PID summary

J. Va'vra

SuperB collaboration meeting in London, 2011

Speakers

Barrel FDIRC

- Jerry Va'vra: "Update on FDIRC prototype"
- Christophe Beigbeder: "Barrel electronics status"
- Jerry Va'vra: "Comment on charge sharing with H-8500"
- Eugeniy Kravchenko: "Investigation of PMT ageing in Novosibirsk"
- Gabriele Simi: "Initial experience with PMT+electronics test setup in Padova"

• Forward PID

- no talk presented this time
- TDR assignments

FDIRC: Definitions of names

(For newcomers)

Photon camera optics:



FDIRC camera mechanics:



FBLOCK and New Wedge

J. Va'vra

- Polishing of the new Wedge is finished. It is being delivered to SLAC.
- FBLOCK polishing will be finished by the end of September. Then it will go to the plating company to produce two mirror surfaces. We will get it sometimes in October.
- The shape of the new optical pieces will be measured with a digital arm owned by the alignment group at SLAC.

FBLOCK after machining its shape:



FBLOCK on x-y polishing table:



Fbox and its support in CRT

Massimo Benettoni, Nicola Mazziotta, and technicians from Padova & Bari



- Fbox and its support was finished in Padova and Bari.
- The parts are at SLAC.

9/15/11

Mechanical trial test of Fbox in CRT

M. McCulloch and J. Va'vra









- Fbox and its support was successfully trial fitted into the CRT stand.
- Right now we working detector holder, electronics shield, air cooling, cable entry.

Test of bar box - wedge gluing



M. McCulloch and J. Va'vra

Gluing fixture:



Trial test of large area gluing:



- Use Epotek 301-2 for this coupling.
- Gluing procedure works well. <u>No bubbles</u>.

Transmission = f(radiation dose) up to ~250krads



- Bottom line: Corning 7980 Fused Silica and RTVs are OK, Epotek-302-1 is the worst.
- Epotek 301-2 OK up to ~250 krads.



Barrel electronics status

Christophe Beigbeder



Front-end board:

- A prototype test board allowing to test 3 diff.
 CFD algorithms
- ASIC-based amplifier
- JV: Do we need an adjustable amp. gain for every channel ?

Motherboard:

- TDC & ADC
- Data packing
- Communication interface
- SCAT chip



Front-end board prototype:

Motherboard:





- Front-end board should be available by the end of this year.
- SCAT chip will be submitted in November.
- Motherboard design will start soon, will be available in 6 months.

Barrel electronics status: communication

Christophe Beigbeder



Problem with Gary's solution:

- Fiber driver are not available, but Gary can provide the artwork to make boards.
- One cannot develop a new electronics outside of SLAC
- LAL engineers do not use XILING chip
- SLAC solution might appear a bit more expensive

Barrel electronics status: communication

Christophe Beigbeder

One possible LAL scheme: Fiber Fiber Compact PCI crate at SLAC: CPU Fiber driver

• Five options for communication protocol:

- 1. LAL: ALTERA chip with a specific firmware developed in Taiwan, and some new software development, "Aurora protocol", Cost: crate, board, PC.
- 2. LAL, etc.: ALTERA chip with two new firmware and two limited software developments, "Fiber channel protocol", Cost: IP, crate, board, PC.
- 3. LAL, Padova: A2818 CAEN board in PC, ALTERA chip with a specific new firmware and PC-based DAQ software developments, "Conet 1 or 2 protocol", Cost: IP, crate, board, PC.
- 4. LAL, Padova: MXI express board in PC, ALTERA chip with new firmware and PC-based DAQ software developments, "Ethernet protocol", Cost: IP, crate, board, PC.

• Whatever the solution, SLAC CRT & scanning setup will be supported !

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Comments on charge sharing with H-8500

J. Va'vra Pad#1 **Burle MCP: charge sharing works** Maximum charge sharing position Pad#2 Single, 100mV/div, 2ns/div 5 6 H-8500: charge sharing does not work Charge-sharing 7 8 (x,y): 39.5, 9.0 Pad#1 Pad#2 M 2 One 1 2505/k IT B Operant 12 2m M 4.0m 25050 A DM 1 -52.0mV

Hamamatsu Multi-anode electrode structure:







Notice a little entrance electrode around each pad boundary. In my opinion, this deflects • photoelectrons away from the pad boundary, which reduces the charge sharing. 9/15/11

1-st FDIRC prototype in the ESA test beam

J. Benitez, D.W.G.S. Leith, G. Mazaheri, B.N. Ratcliff, J. Schwiening, J. Va'vra, L.L. Ruckman, G.S. Varner, NIM A 595 (2008) 104

H-9500 with 3 mm x 12 mm pixels:



- One can see that with the chromatic correction the performance with 3mm x 12mm pixels is superB.
- If we adopt H-9500 with 3mm x 12mm pixels, we would have 64 pixels/tube.

Present FDIRC predicted performance

Doug Roberts, SuperB workshop, Annecy, 2010

1: FDIRC performance simulation by Geant 4 MC.	
Option	$\theta_{\rm e}$ resolution [mrad]
FDIRC with 3 mm x 12 mm pixels with a micro-wedge	8.1
FDIRC with 3 mm x 12 mm pixels & no micro-wedge	8.8
FDIRC with 6 mm x 12 mm pixels with a micro-wedge	9.0
FDIRC with 6 mm x 12 mm pixels & no micro-wedge	9.6
	1: FDIRC performance simulation by Geant 4 MC. Option FDIRC with 3 mm x 12 mm pixels with a micro-wedge FDIRC with 3 mm x 12 mm pixels & no micro-wedge FDIRC with 6 mm x 12 mm pixels with a micro-wedge FDIRC with 6 mm x 12 mm pixels & no micro-wedge

- The most conservative decision, which is a design #4, would give the same performance as the BaBar DIRC (~9.6 mrads for di-muons).
- However, one should point out that FDIRC will correct out the chromatic error by timing, which would reduce the error by 0.5-1 mrads.
- If we reduce the pixel size in y-direction by the charge sharing we gain. <u>The question is how much, and is the improvement worth the effort ?</u>

QE aging of <u>MCP tubes</u> in Novosibirsk

E. Kravchenko (reporting on work of A. Barnyakov: NDIP11, Lyon, 2011)



- **QE aging is caused by ion bombardment of the photocathode.**
- Ion bombardment affects the red region of QE first. 9/15/11 J. Va'vra, PID summary, London

My comment to MCP vs. MaPMT aging

J. Va'vra



MaPMT's photocathode is shielded from ions:



- Hamamatsu took great care to design the dynode structure to prevent ions from hitting the photocathode. Every dynode shields ions, and there are 12 dynodes in the structure.
- MCP structure is vulnerable to this problem, and therefore one has to work hard to invent various tricks (foils, scrubbing, photocathode protection, etc.)
- I would expect that the MaPMT aging is similar to the classical PMT aging, such as what we have observed on tubes in DIRC.
- But it should be checked with H-8500, of course.

9/15/11

Initial experience with PMT+electronics test setup in Padova

Gabriele Simi

1. Present effort



- Test setup with Burle MCP and H-8500
- CAEN waveform digitizer

2. Future possibility

Development "PCIexpress" board with FPGA:



- Xylinx ML605 with 8 optical links
- BLAB3 or French electronics.

Conclusion

- A clear progress on FDIRC prototype thanks to work of people in Padova, Bari and SLAC.
- BLAB3 electronics will be available in January 2012 (the 1-st unit for testing in the SLAC scanning setup in October, 2011).
- LAL electronics will be available in March 2012.
- We are not yet settled on the electronics communication protocol between PC & motherboard.
- Conclusion on the charge sharing with H-8500: it does not work, thus we cannot reduce the pixel size by the charge interpolation. If we want to reach the best test beam θ_c resolution results with the 1-st FDIRC prototype, we would have to go to 3mm x 12mm pixels of H-9500. Thinking....
- We have seen interesting MCP aging results from Novosibirsk.
- A new effort in Padova to understand H-8500 & MCP.