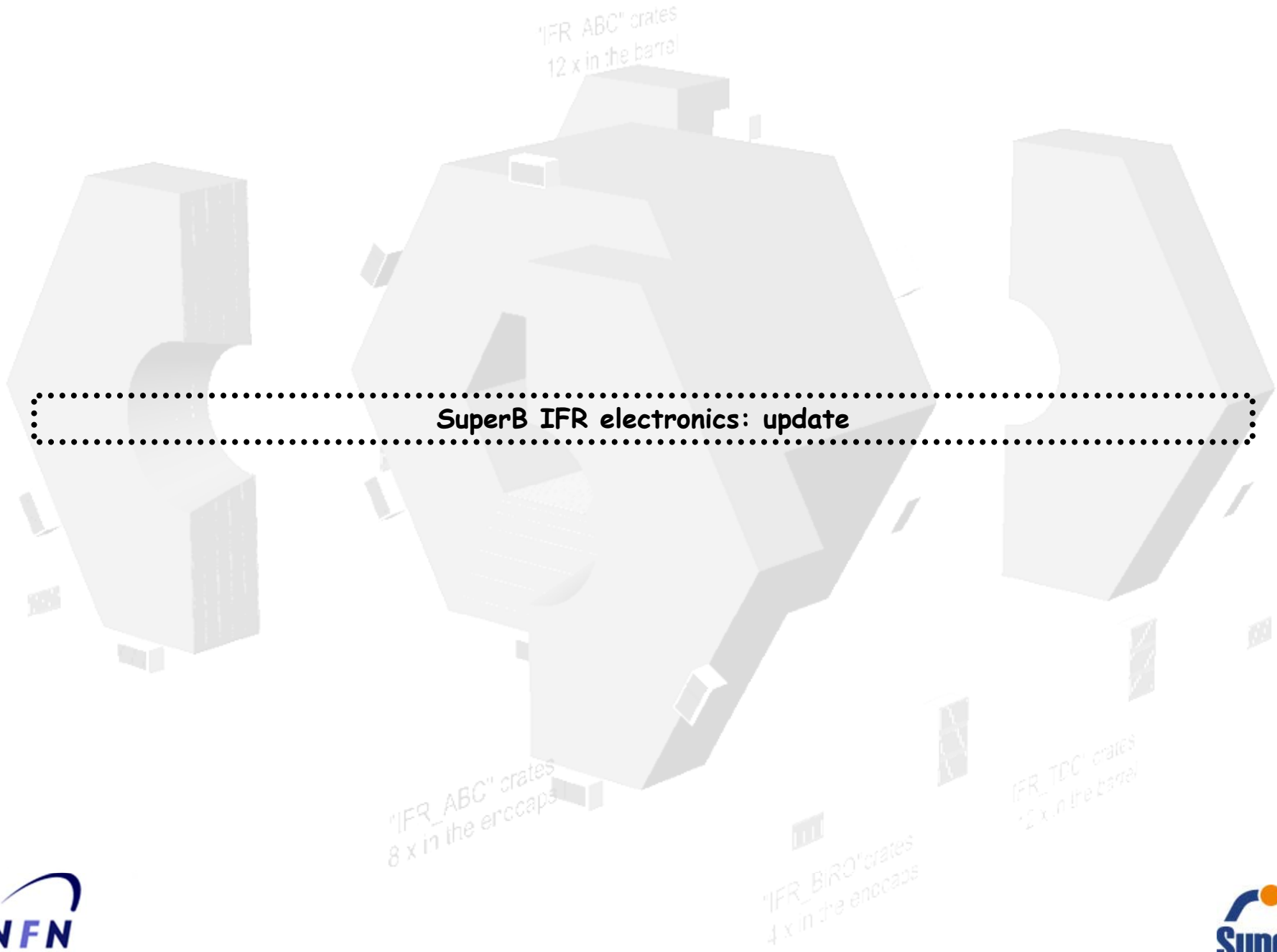


SuperB IFR electronics: update

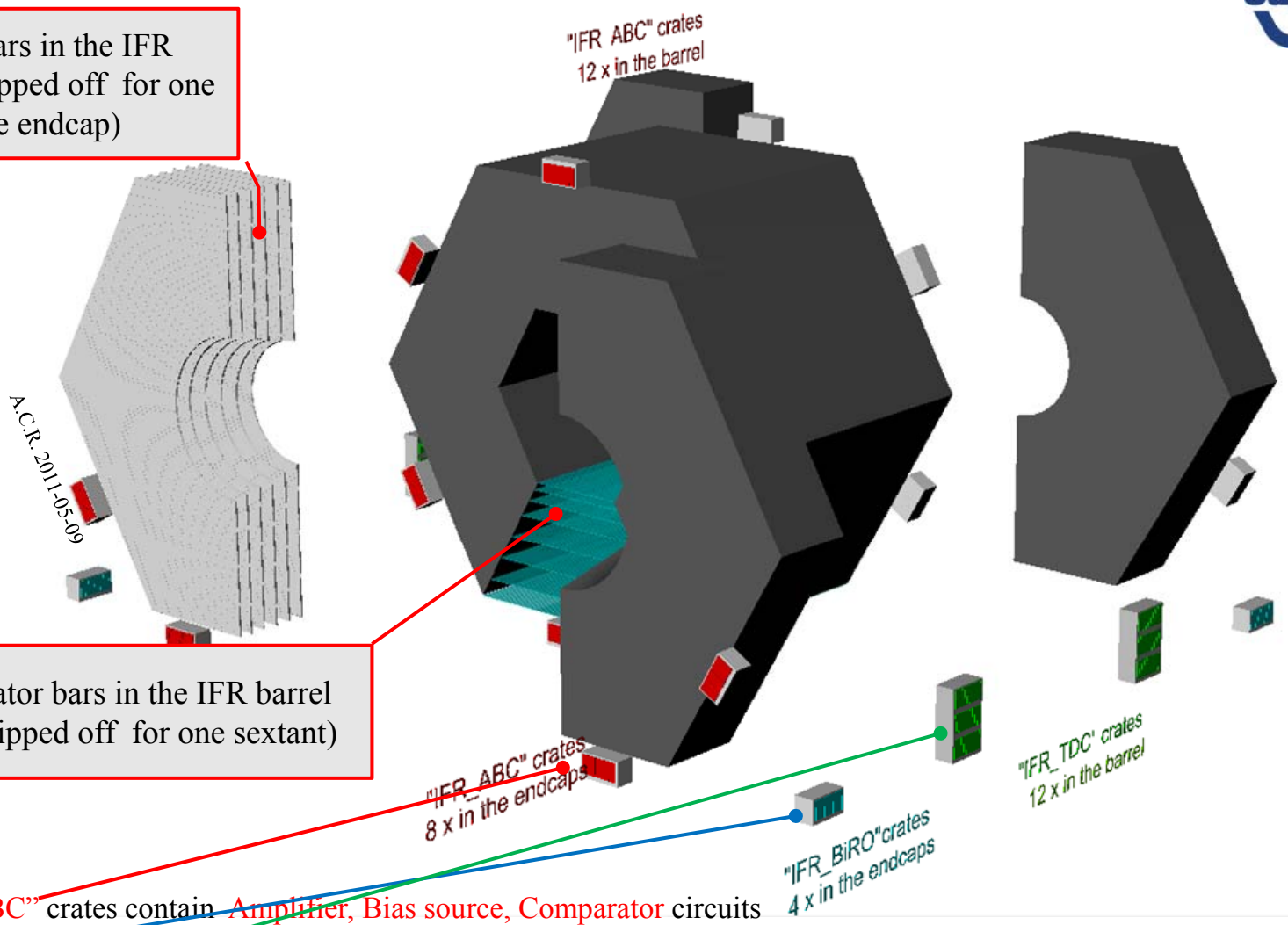
SuperB IFR electronics: update

summary:

- recalling features of the baseline design
- evolving from the baseline design: exploring an all "binary mode" ("BiRO") readout for the IFR
- update:
  - SiPM test in Krakow (W. Kucewicz, Jerzy Barszcz, Mateusz Baszczyk, Piotr Dorosz, Sebastian Glab)
  - developing a compact front end for "BiRO": the "EASIROC" ASIC (by Omega at LAL, Orsay)
  - developing a compact front end for "BiRO": testing FPGAs and design techniques for radiation mitigation
- next milestones:
  - planning irradiation test to get an estimate of the failure rates of a prototype "compact" front end card

SuperB IFR electronics: recalling features of the baseline design

Scintillator bars in the IFR endcap (iron stripped off for one half of the endcap)



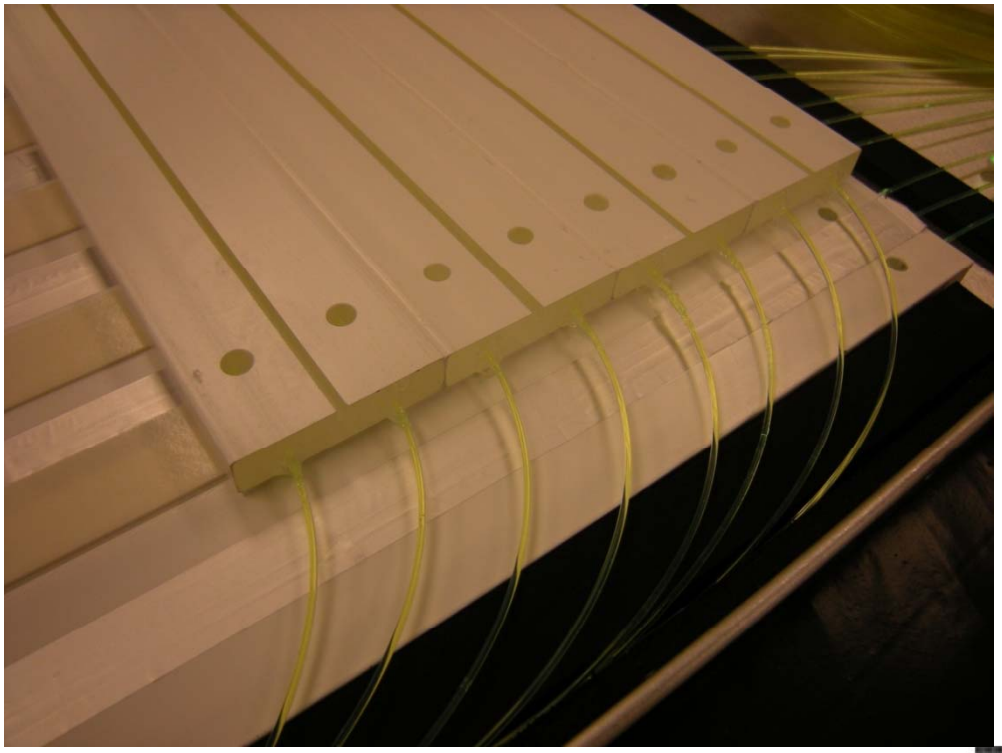
Scintillator bars in the IFR barrel (iron stripped off for one sextant)

Legenda:

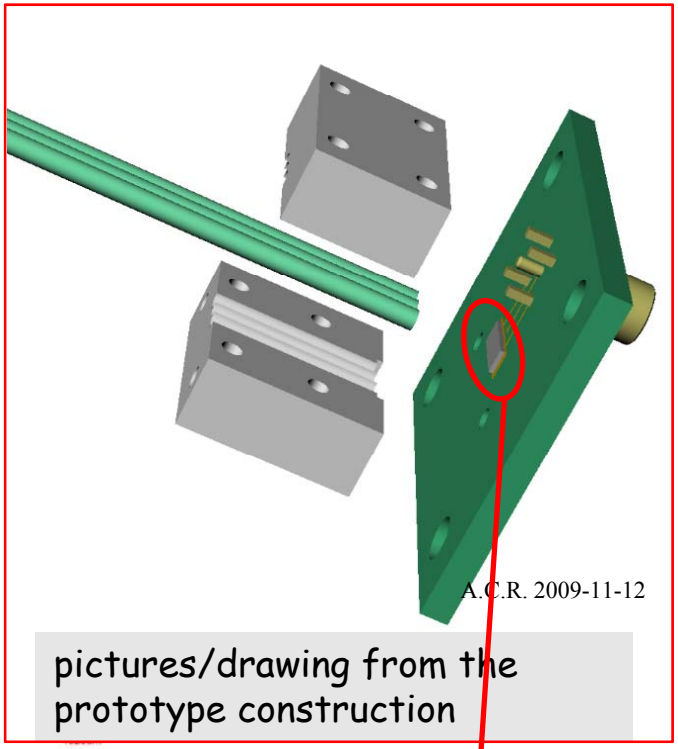
- "IFR_ABC" crates contain Amplifier, Bias source, Comparator circuits
- "IFR_BiRO" crates contain sampling circuits and buffer memories to Read Out the IFR_ABC cards in Binary mode
- "IFR_TDC" crates contain TDC circuits and buffer memories to readout the IFR_ABC cards in timing mode

In the baseline design the splitting of functions was meant to allow the digitizers (TDC ASICs mainly) and latency buffers to be positioned as far as possible away from the high radiation region of the detector and surroundings.

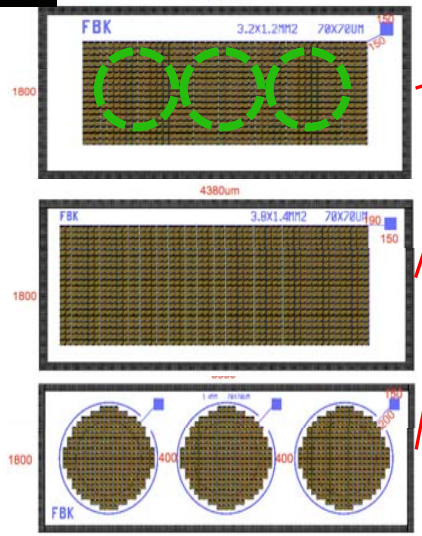
SuperB IFR electronics: recalling features of the baseline design



SuperB IFR : the scintillating bars are equipped with wavelength shifting fibers (3 for each bar in the prototype), which are then coupled to a SiPM device by means of precisely machined plastic supports.



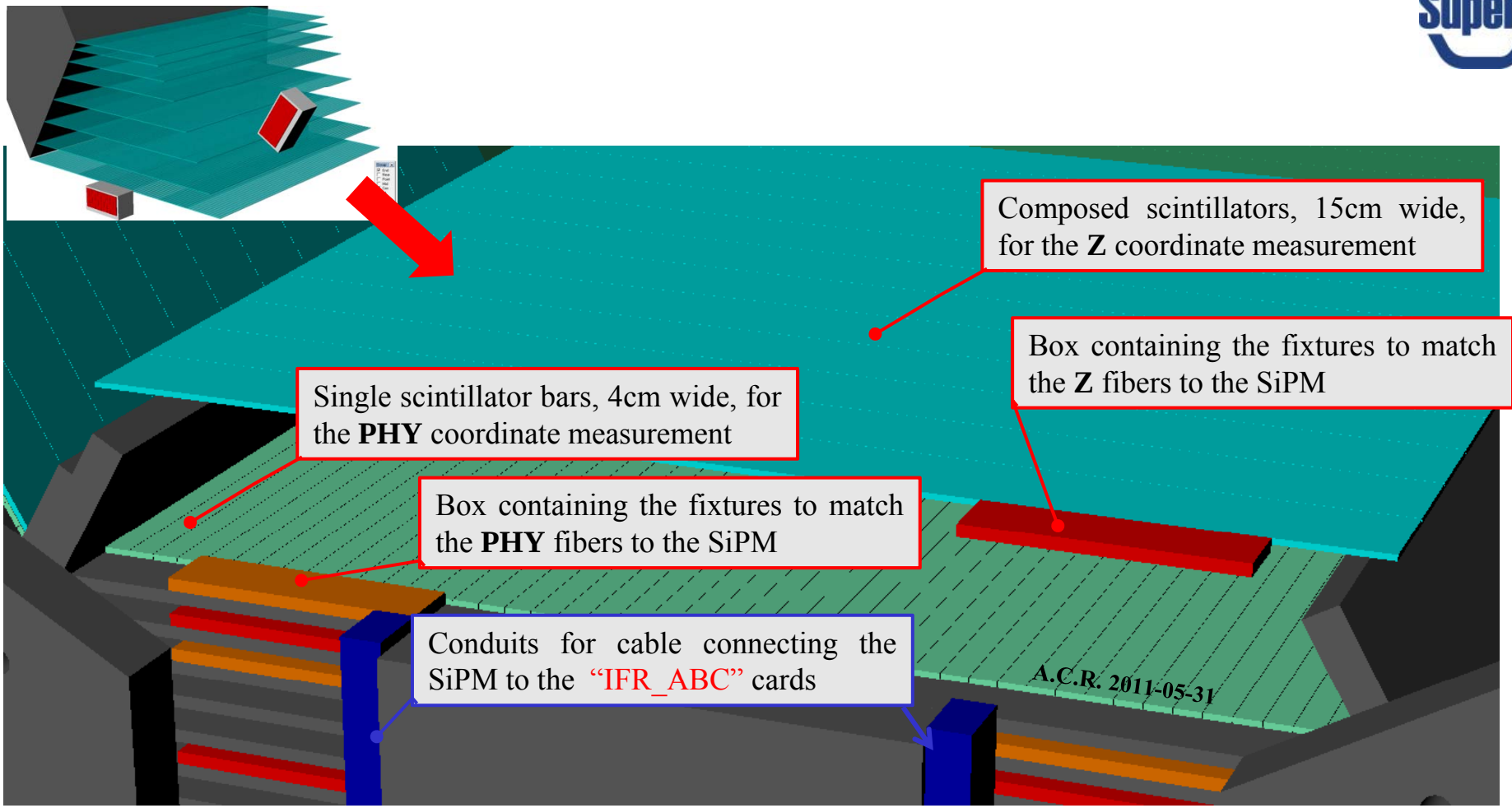
pictures/drawing from the prototype construction



SiPM by FBK, Trento. 70x70um² cell size, n-on-p.

Bonding of the SiPM to the carrier PCB was performed at INFN Perugia thanks to G. Ambrosi, M. Ionica

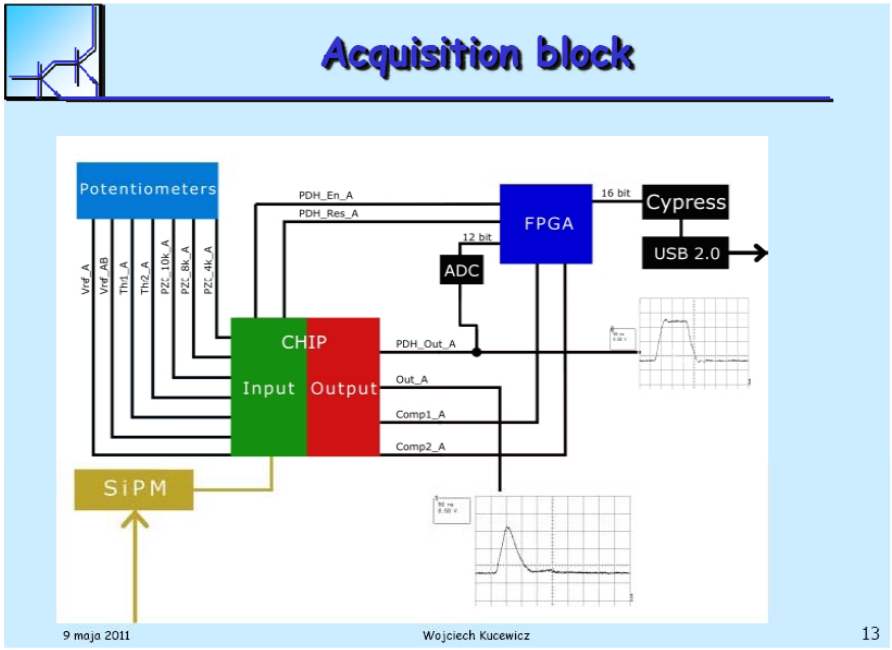
SuperB IFR electronics: exploring an all "binary mode" ("BiRO") readout for the IFR

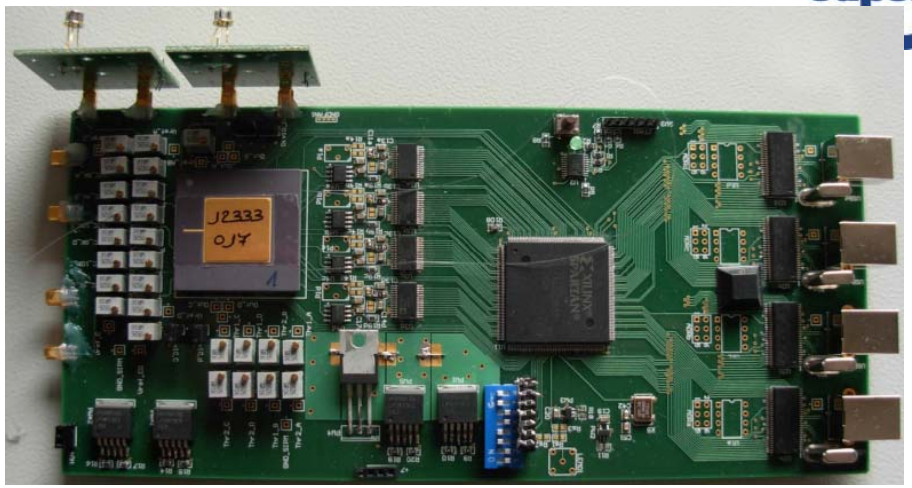


Note: the Z and the PHY layers have been separated in this picture to show them distinct

The actual implementation of the X-Y detector planes is being defined; they will probably result from the union of smaller X-Y modules

SuperB IFR electronics: SiPM test in Krakow





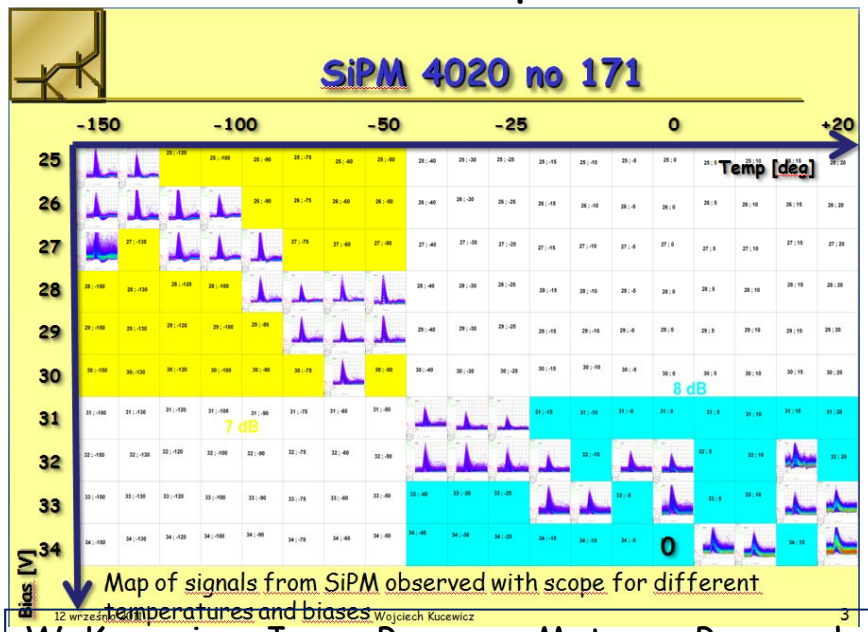
From:
"Silicon Photomultiplier Activity at AGH-University of Science and Technology",
W. Kucewicz, J. Barszcz, S. Głąb, M. Sapor.

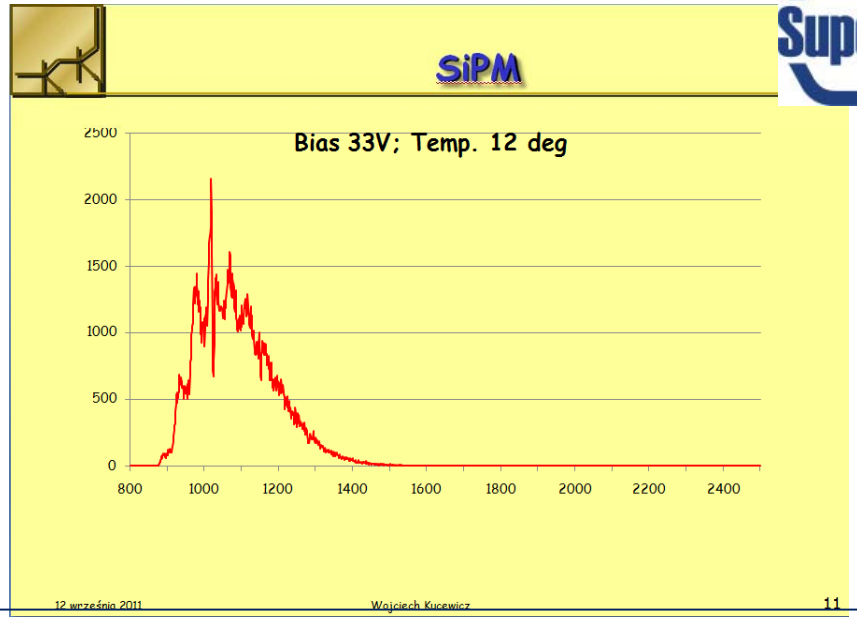
Prof. Kucewicz and his team (Jerzy Barszcz, Mateusz Baszczyk, Piotr Dorosz, Sebastian Glab) have characterized our SiPMs (FBK model 4020) with their test board for ASIC#2.

The preliminary results are presented at this collaboration meeting.

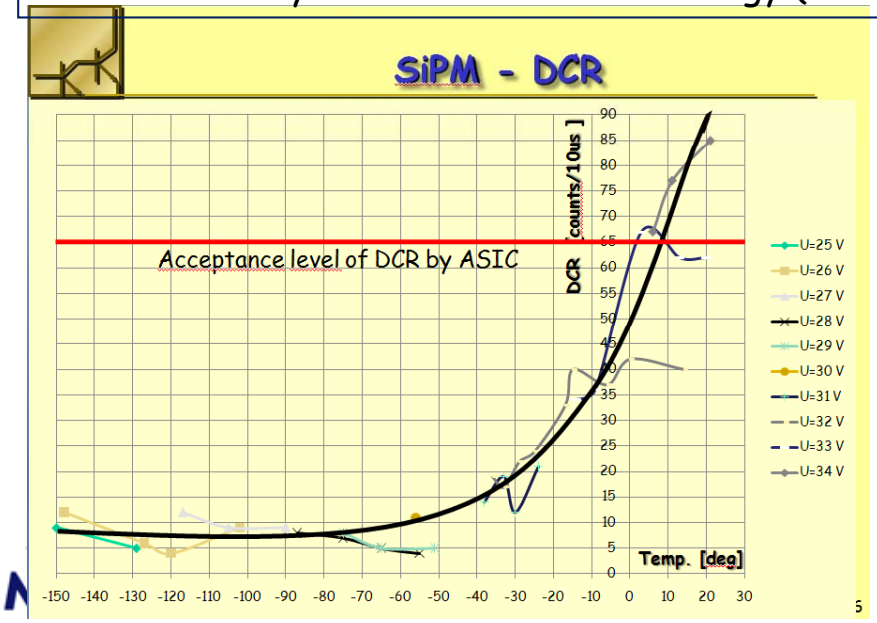
A pool of the test boards could be exploited to built a large scale quality control system for the SiPMs

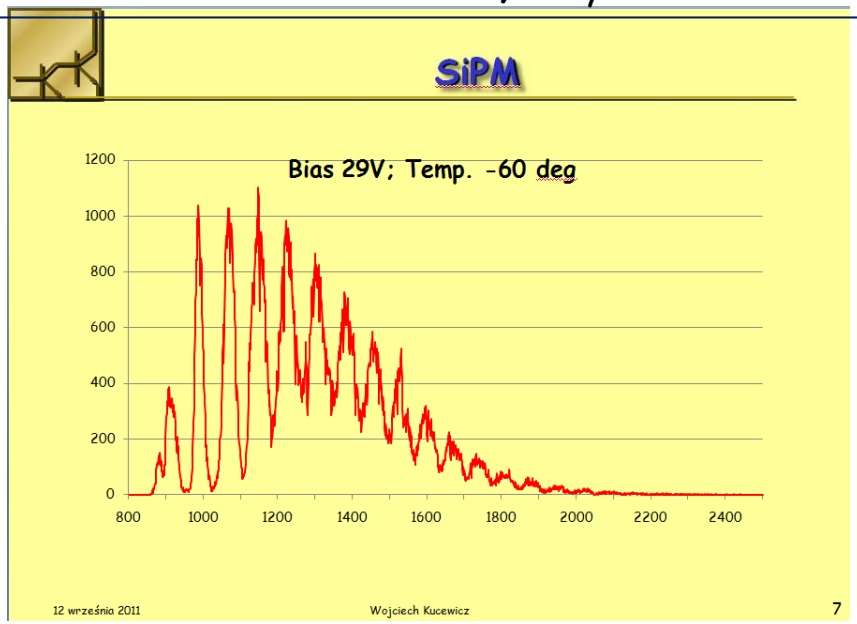
SuperB IFR electronics: SiPM test in Krakow





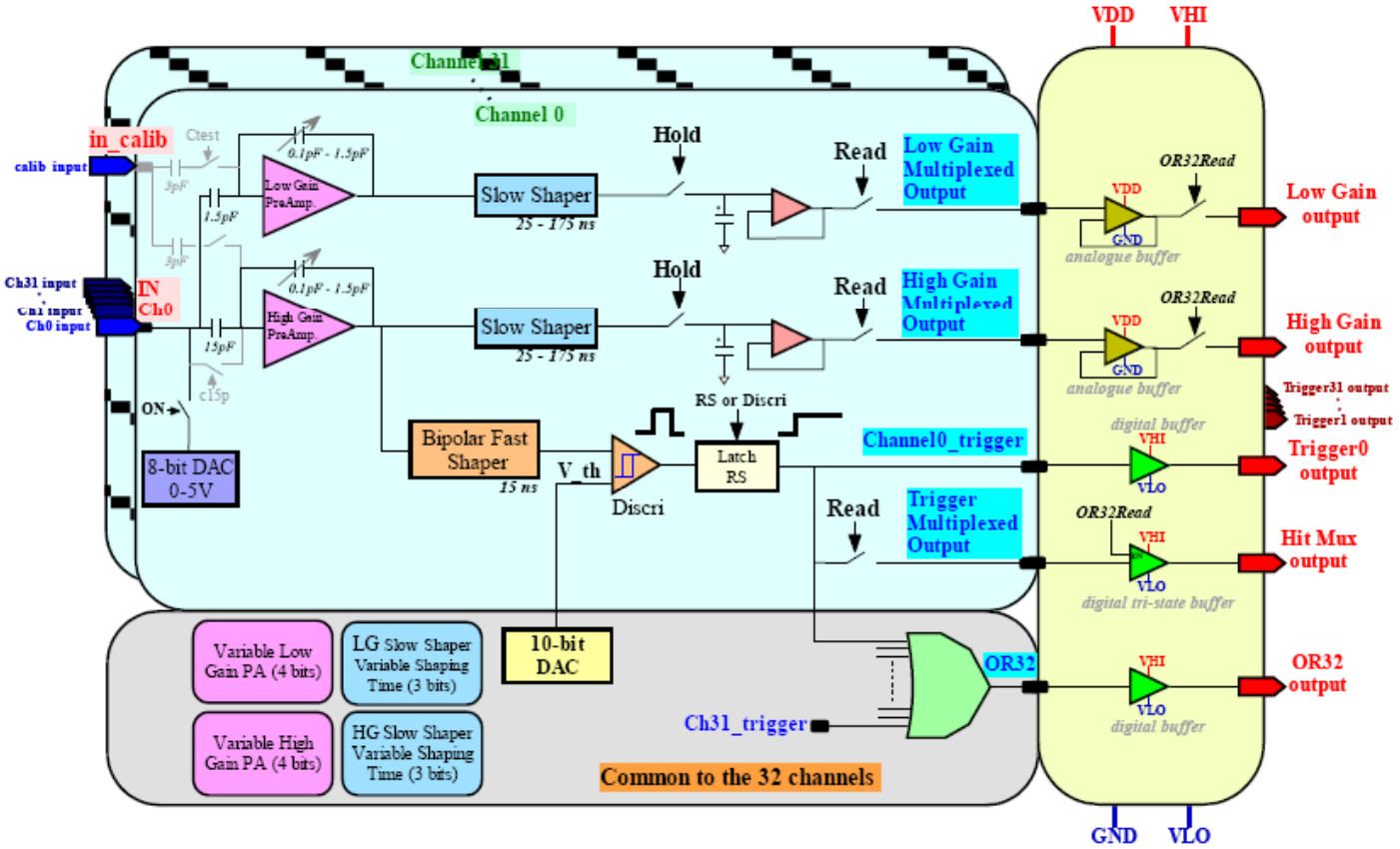
W. Kucewicz, Jerzy Barszcz, Mateusz Baszczyk, Piotr Dorosz, Sebastian Glab
AGH University of Science and Technology (AGH), Krakow: "SiPM from Ferrara", July 2011





SuperB IFR electronics : developing a compact front end for "BiRO": the "EASIROC" ASIC

The "EASIROC" by the OMEGA group of LAL in Orsay is being considered as a candidate ASIC suitable for the front end stage of a "binary mode" readout of the IFR detector



It has an individual trigger output for each of 32 channels plus 32 individual bias setting DACs and a common threshold setting DAC.

The EASIROC was not designed to operate in a high radiation area, BUT the OMEGA group is working at a newer version featuring improved radiation tolerance

USER GUIDE Omega

EASIROC

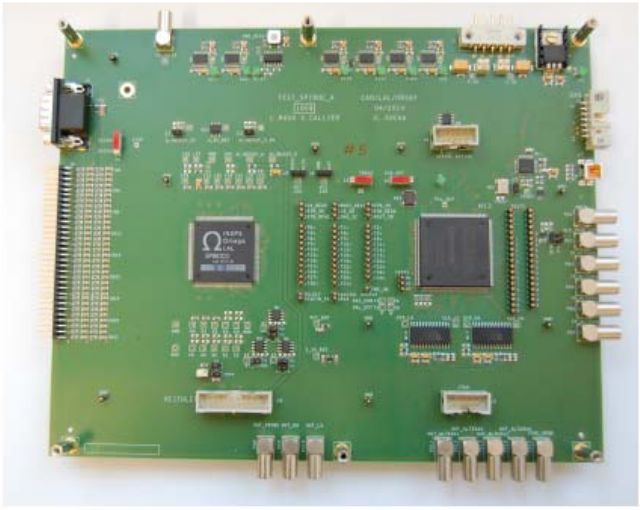
SOFTWARE & TEST BOARD USER GUIDE

Version: 11 April 2011

Abstract

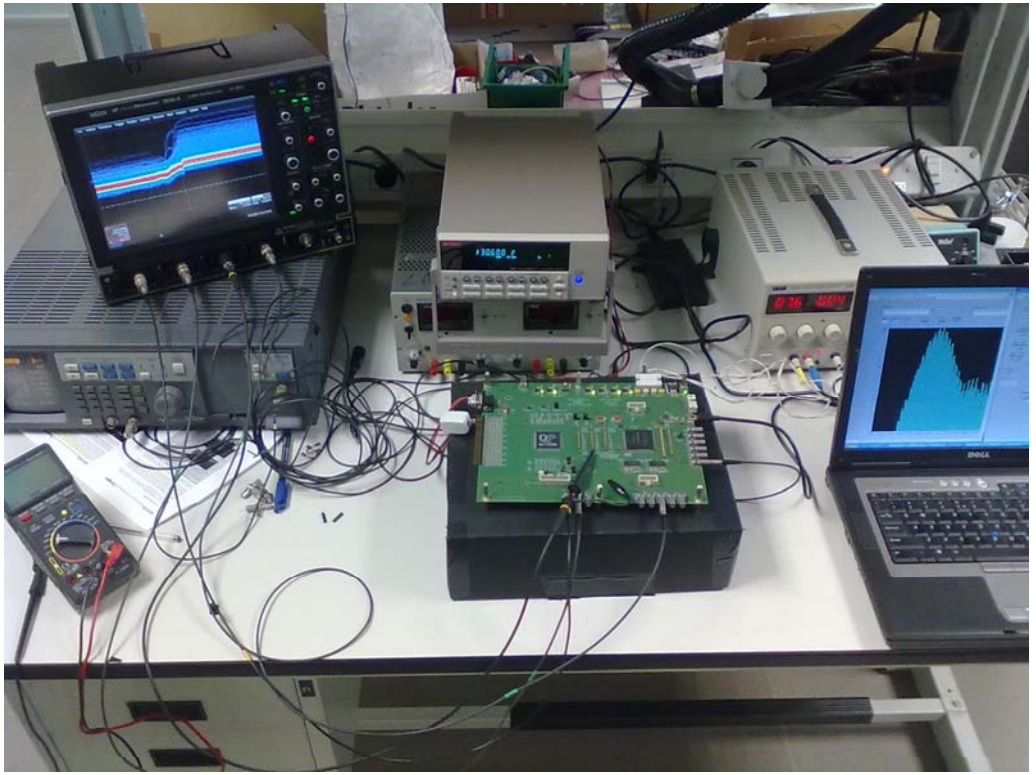
EASIROC (previously SPIROC0), standing for *Extended Analogue Silicon pm Integrated Read Out Chip*, is a 32-channel fully-analogue front end ASIC dedicated to the gain trimming and read-out of SiPM detectors.

This guide explains how to install & use the test board for EASIROC and how to operate with the associated software.



Orsay MicroElectronics Group Associated

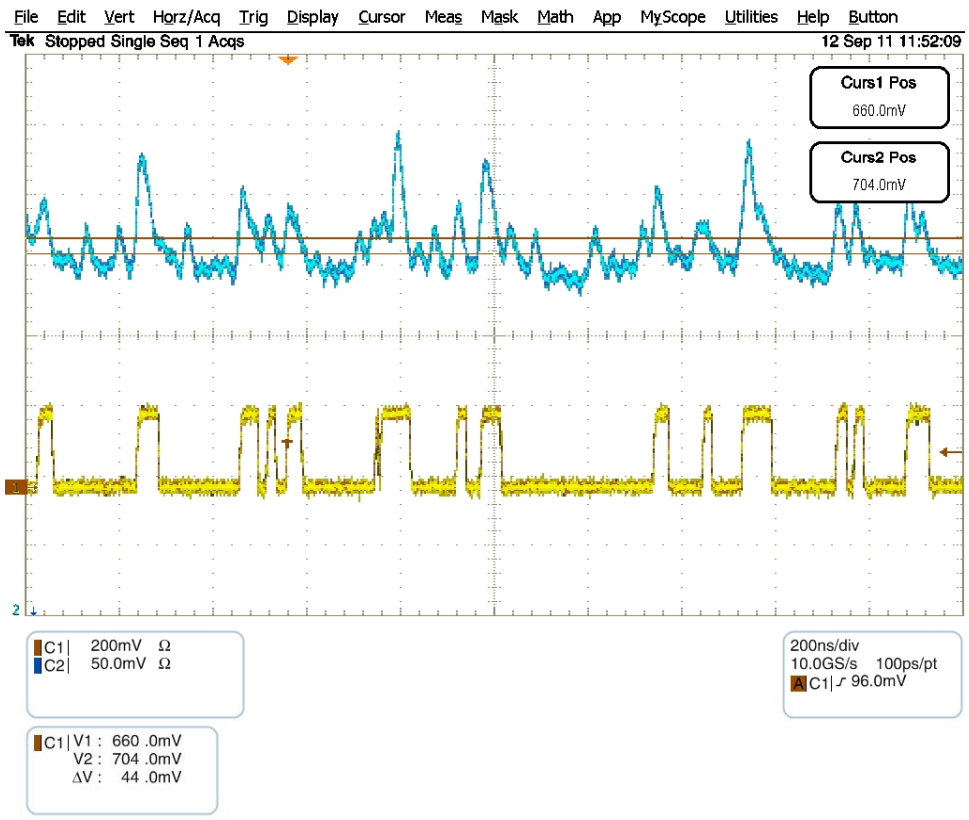
The IFR-Ferrara group has been in touch with Gisèle MARTIN-CHASSARD and Stephane CALLIER of OMEGA who have shown interest in the project and provided us not only plenty of information and support but also a complete hardware and software test system.



SO:
The plan is now to apply an "EASIROC" to a "pizza box" detector prototype and to perform cosmic ray tests to determine the overall efficiency.

Some preliminary test are being carried out to determine the proper operating parameters (bias and threshold) for our FBK SiPMs applied to the EASIROC (acknowledgements to Roberto Malaguti, INFN-Ferrara)

For this test a SiPM #5 of the 4380 type from FBK was connected to channel 4 of the ASIC.
A fiber illuminated by a blue LED was connected to the SiPM. The SiPM support had to be modified to adapt to the different biasing scheme imposed by the ASIC.

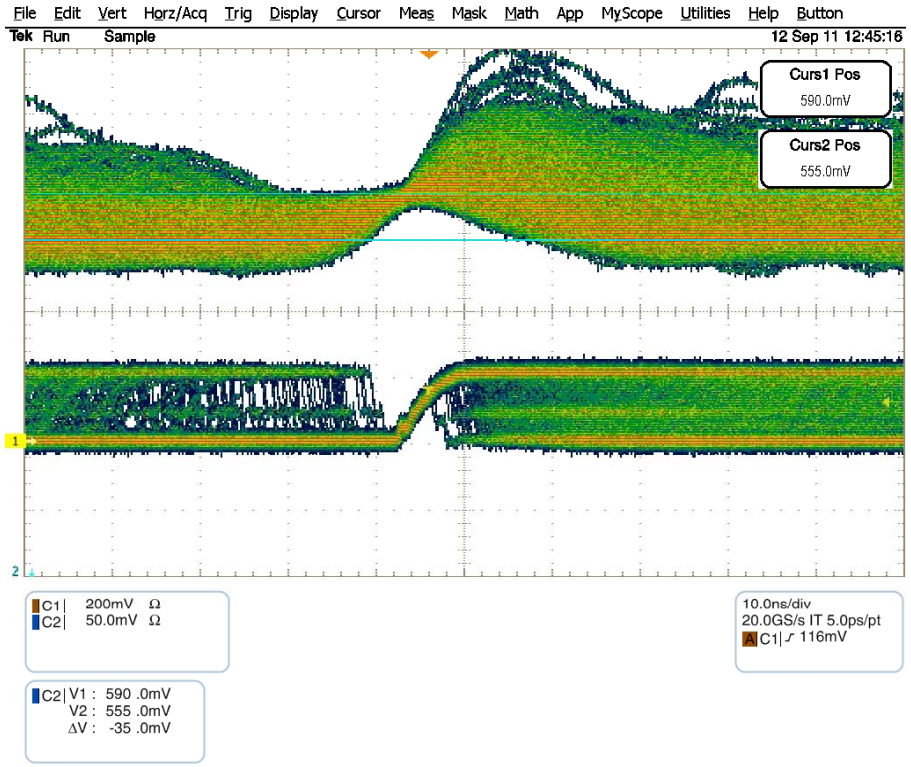


For this test SiPM #5 of the 4380 type from FBK was connected to channel 4 of the ASIC.

The SiPM was biased @ 32.3V and the LED pulser was OFF → what is shown in the waveform is a sample of dark counts

The waveforms reported here represent:
-blue trace: the output of channel 4's internal 15ns fast shaper. This internal signal is observed at the "probe" output of the EASIROC test board (attenuated a factor of 2)
- yellow trace: the output of channel 4 "trigger" comparator

The dark count rate at room temperature is about 12.5MHz if one looks at the blue "spikes" a little less at the "trigger" output with DAC threshold setting of 904 (≈ little above 1 p.e.)



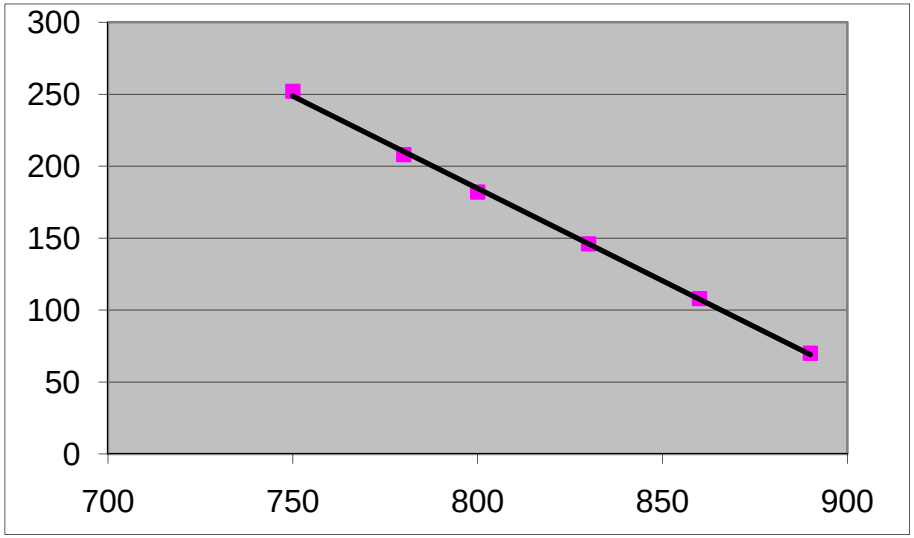
For this test SiPM #5 of the 4380 type from FBK was connected to channel 4 of the ASIC.

The SiPM was biased @ 32.3V and the LED pulser was ON → what is shown are accumulated samples of dark counts + stimulated response

The accumulated waveforms reported here represent:
- top trace: the output of channel 4's internal 15ns fast shaper. This internal signal is observed at the "probe" output of the EASIROC test board (attenuated a factor of 2)
- bottom trace: channel 4 's "trigger" output

We estimated that the output of the internal fast shaper has a sensitivity of about 36 mV per p.e.

The test allowed us to calibrate the threshold DAC setting in terms of p.e. (about 30 counts per p.e.).

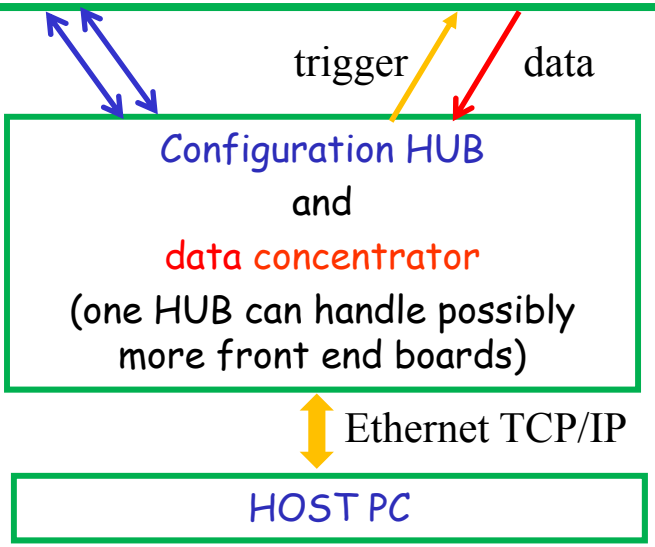


SO:
The plan is now to apply an "EASIROC" to a "pizza box" detector prototype and to perform cosmic ray tests to determine the overall efficiency.

Next steps:

• design a board (which would also be used for radiation tolerance test) hosting:

- one EASIROC
- EASIROC power supply with latchup detection / protection
- flash based FPGA for EASIROC configuration & data processing; the FPGA would be connected by LVDS links (electrical / optical ?) to a:



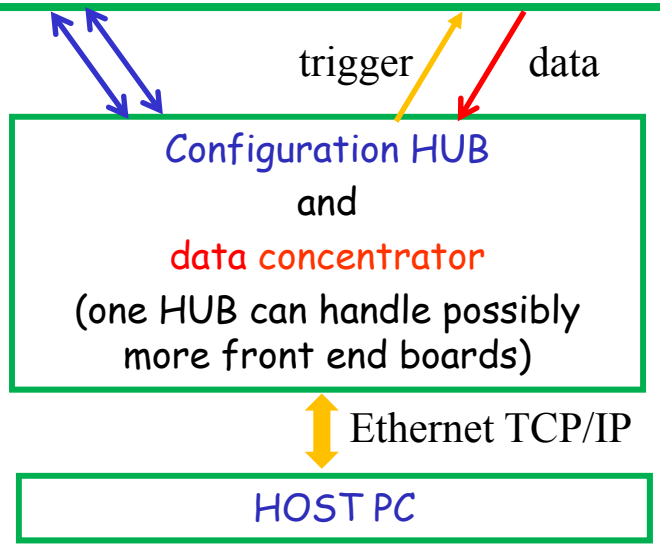
SuperB IFR electronics : developing a compact front end for "BiRO": the "EASIROC" ASIC

SO:
The plan is now to apply an "EASIROC" to a "pizza box" detector prototype and to perform cosmic ray tests to determine the overall efficiency.

Next steps:

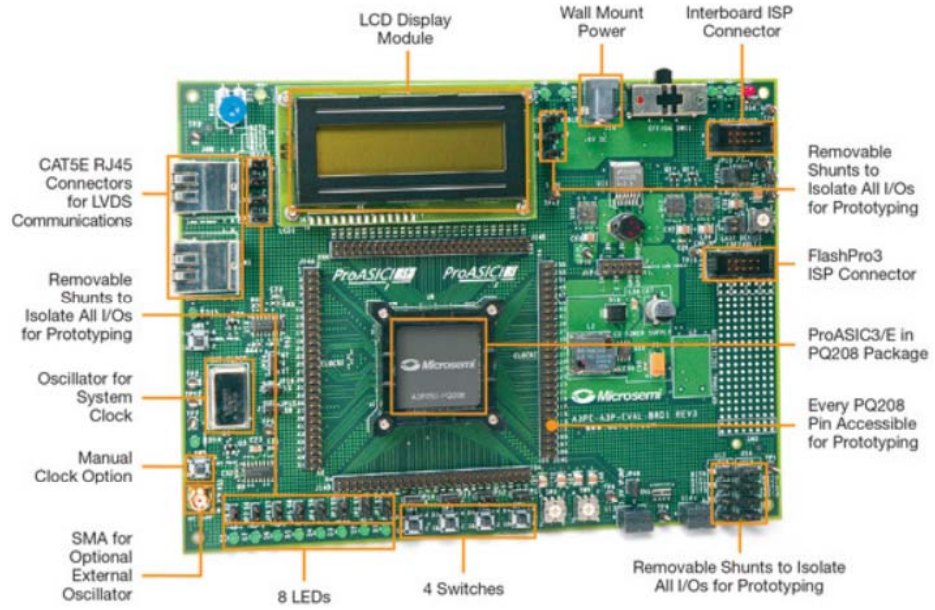
• design a board (which would also be used for radiation tolerance test) hosting:

- one EASIROC
- EASIROC power supply with latchup detection / protection
- flash based FPGA for EASIROC configuration & data processing; the FPGA would be connected by LVDS links (electrical / optical ?) to a:

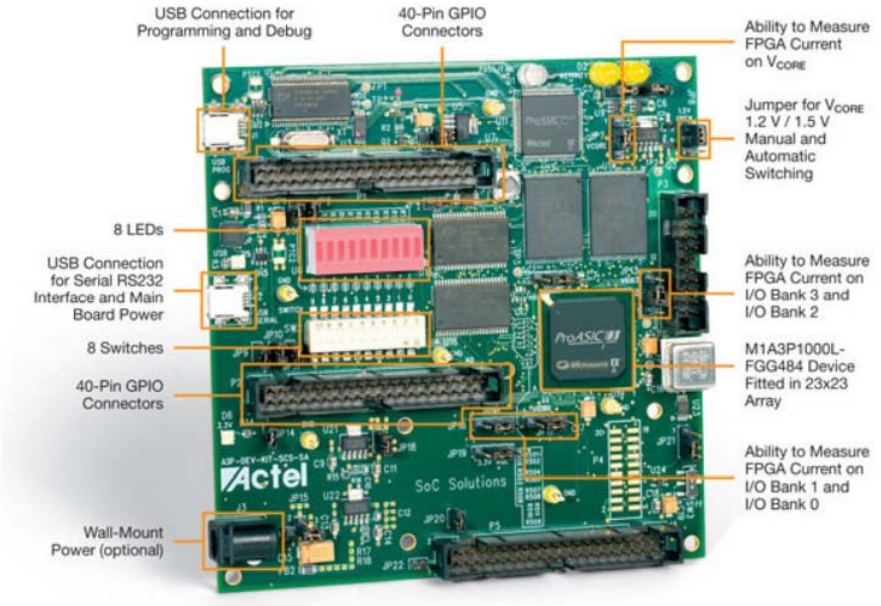


SuperB IFR electronics : testing FPGAs and design techniques for radiation mitigation

Two development cards based on ACTEL ProASIC devices have been procured:

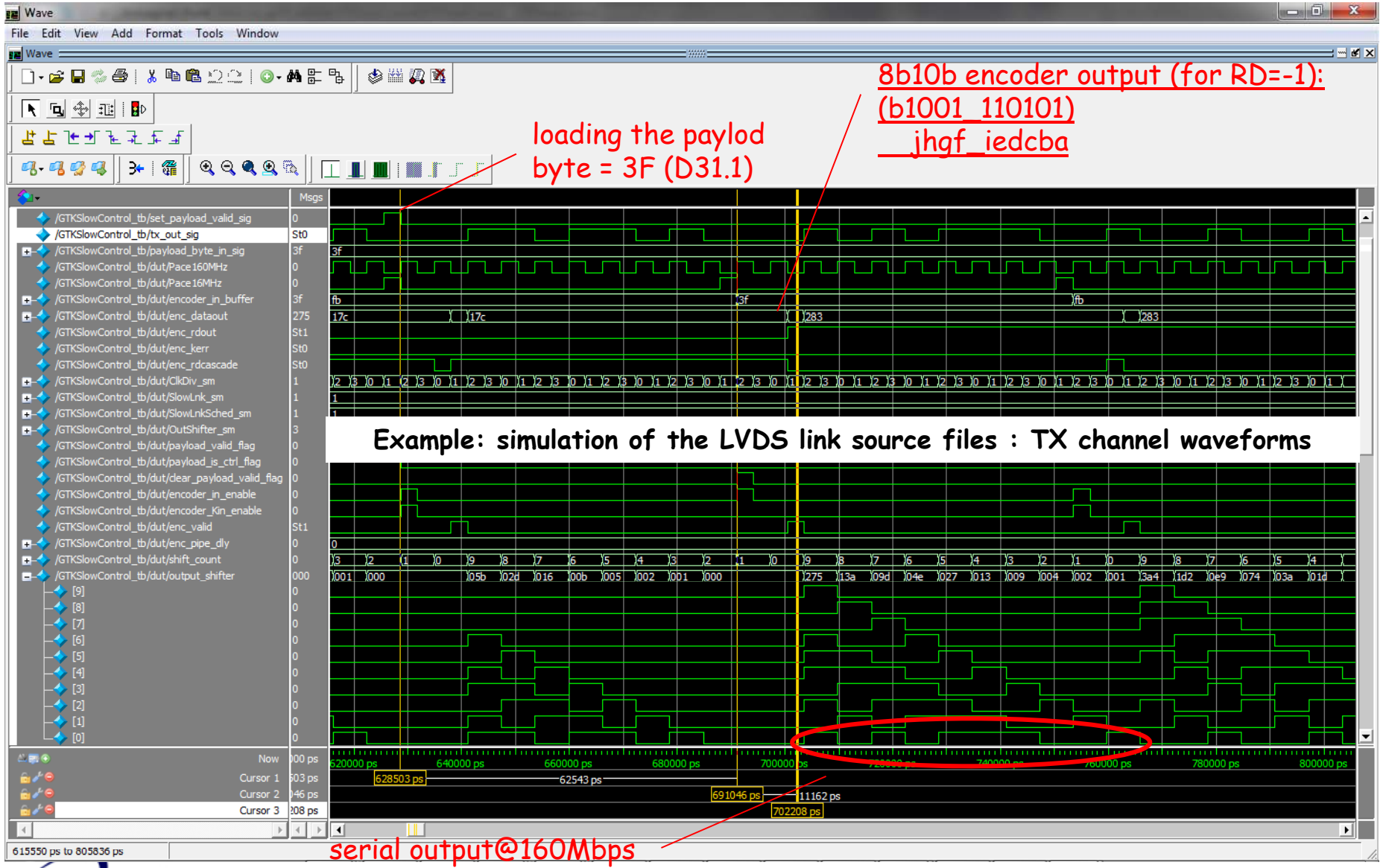


Evaluation board with an A3PE1500-PQ208 FPGA

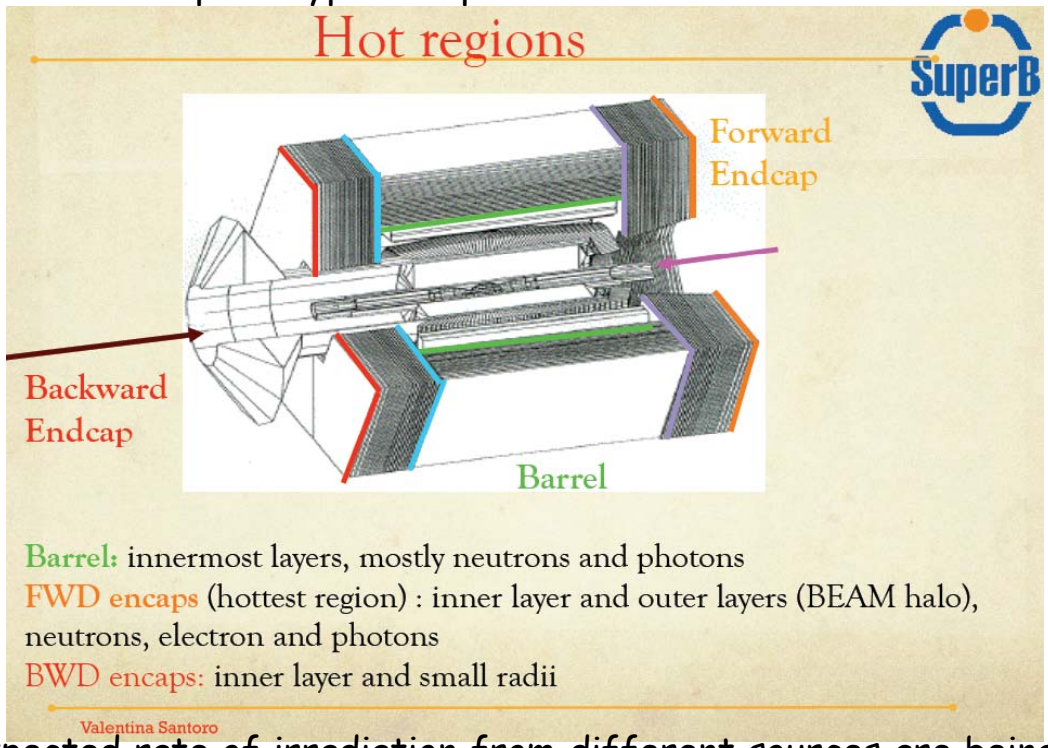


Development board with an M1A3P1000L-FGG484 device

and work has started to get acquainted with the Libero development system and the resources offered by the ACTEL device.
As a first excercise we are implementing:
- the EASIROC configurator unit and its local storage controller, interfaced to the HUB via a high speed link exploiting the LVDS pins of the proASIC 3 devices (thesis work of Lorenzo De Santis)
- the serial stream will be 8b/10b encoded to achieve a DC balanced signal that could be sent through a fiber link and to have some inherent protection against error induced by noise or single events


Wave
File Edit View Add Format Tools Window
loading the paylod
byte = 3F (D31.1)
8b10b encoder output (for RD=-1):
(b1001_110101)
jhgf_iedcba
Example: simulation of the LVDS link source files : TX channel waveforms
serial output@160Mbps

SuperB IFR electronics : planning irradiation test to get an estimate of the failure rates of a prototype "compact" front end card



Reliable data on expected rate of irradiation from different sources are being produced lately
→ we can now plan irradiation tests at the proper facilities in order to evaluated the rate of:
-Single Event Latchup (is the ASIC affected ?)
-Single Event Upsets (how often will the DACs in the ASIC need to be refreshed ?)
(how often a local parameter table in the FPGA will be corrupted by radiation? HAMMING CODING SHOULD HELP)
- Rate of Functional Interruptions (TRM techniques in FPGA state machine design SHOULD HELP HERE)

THE OUTCOME OF THESE TEST WILL DETERMINE WHETHER THE FRONT END ELECTRONICS COULD EVENTUALLY BE LOCATED "INSIDE THE IRON"