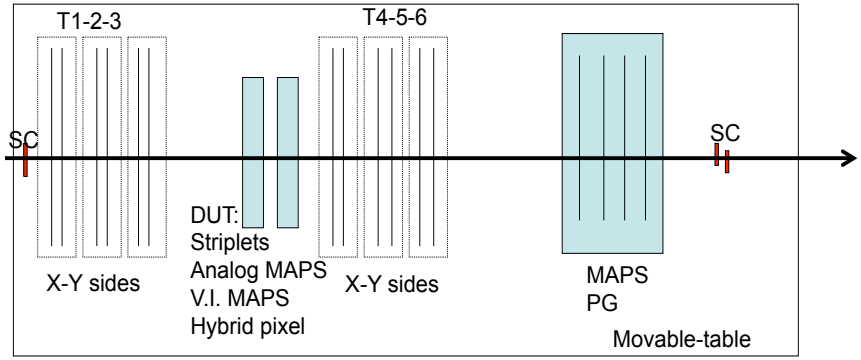
SVT (I)

Testbeam @CERN starting next week

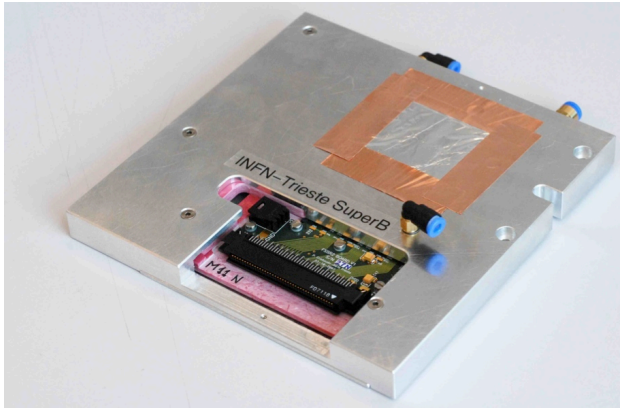
- Most of the SVT group working hard over the summer to get things ready
  - Thanks to S. Bettarini for the organization
- Several pixel structures and striplets on test



New flexibility implemented in DAQ system (Bologna) to test all the different DUT's

Analysis team (Pi+BO+MI) is getting the new code ready

5 new telescope modules with FSSR2 readout built in Trieste to a have a 3+3 telescope configuration.



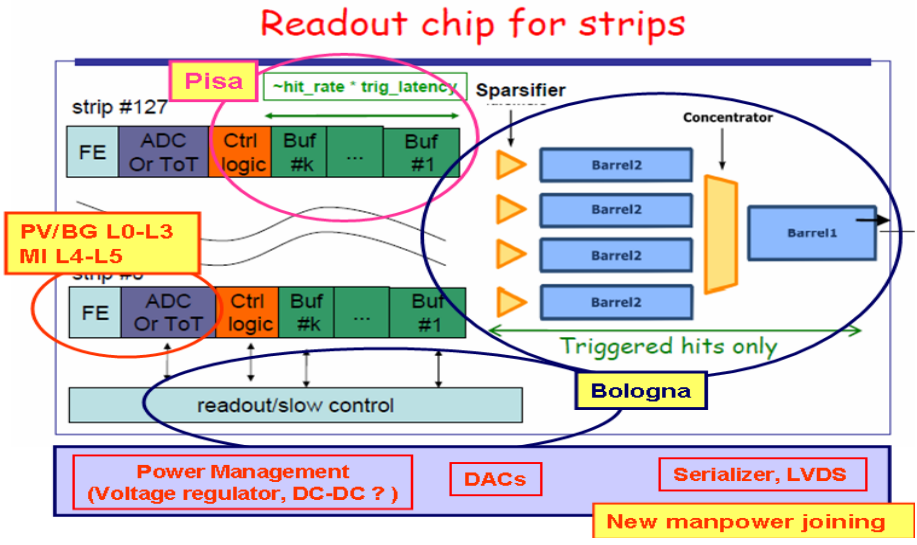
More robust movable table (Torino)

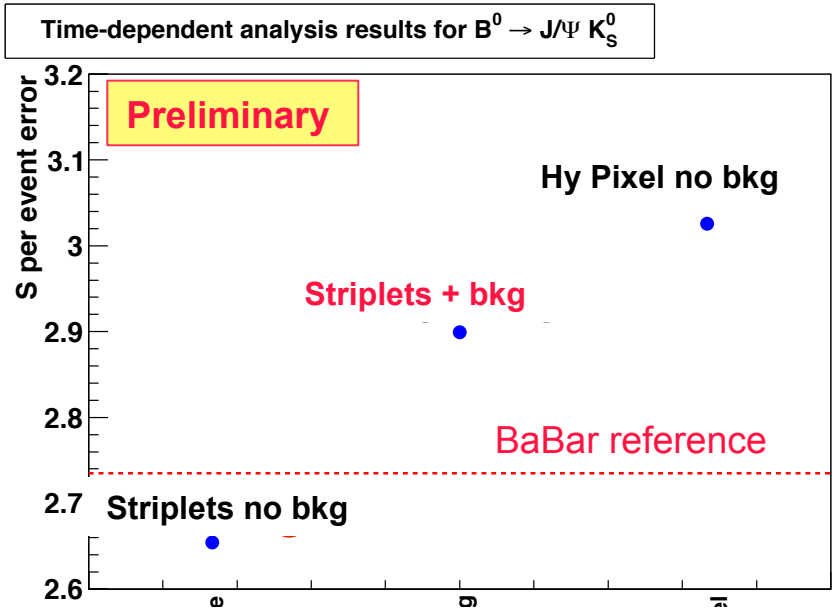
SVT (II)

- Progress on Baseline configuration (Striplets L0+L1-L5 design)

Readout chips for striplets/strip:

- detailed plan for chip development by Italian groups presented to INFN.
  - Develop fast (L0-L3) and slow (L4-5) channels & adapt readout architecture used for pixel.
    - Full VHDL simulation for TDR.
    - Prototypes chips in 2012 & 2013
    - Production run in 2014





First preliminary results on striplets performance in high background with Fastsim

- Hits from background pairs added to signal for time dependent analysis.
  - Still safety factor not included on back rates.
- Checks on fundamental quantities still to be done and and several technical problems need to be fixed to perform systematic studies.

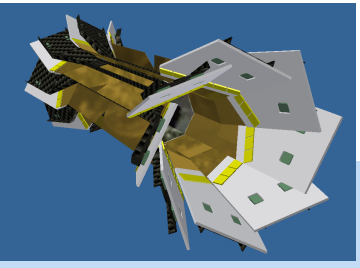
SVT (II)

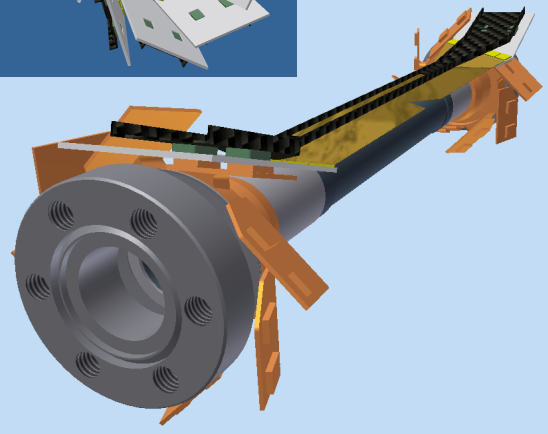
Background simulation:

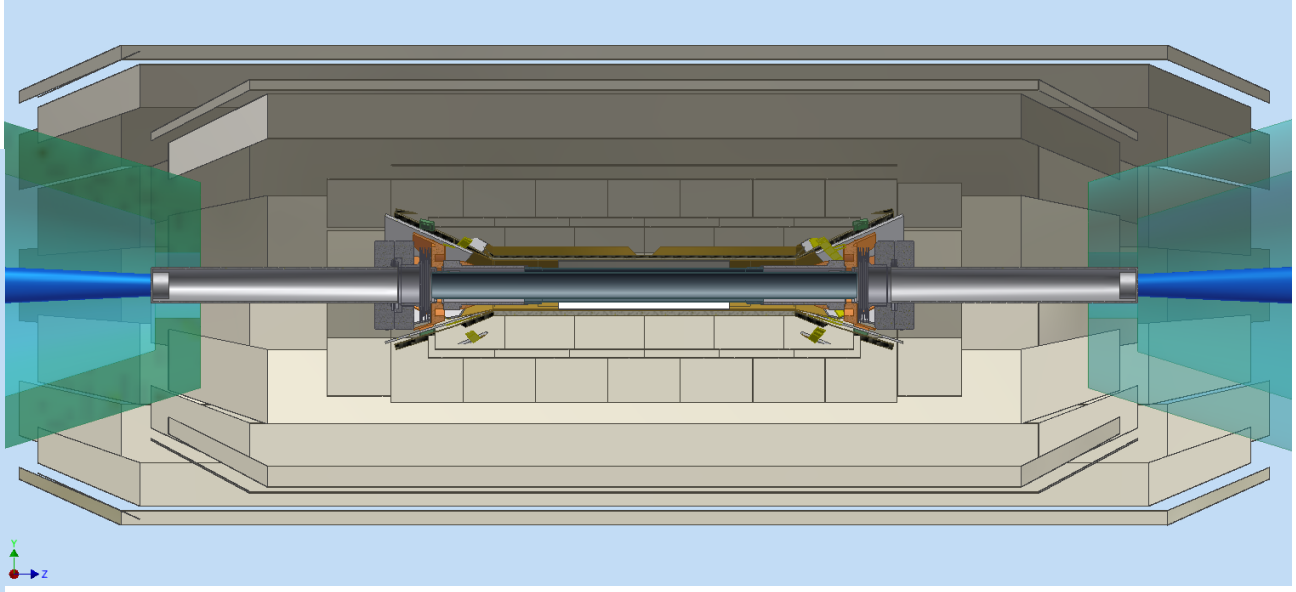
- Strip detail implemented in Bruno for a more accurate rate calculation
- Very useful contribution from Trieste group to cross check results and get more solid background estimates!
- Distributions of cluster multiplicity and energy deposited/strip will be provided as input for readout chip simulation

Layer	RO PitchZ (or +45°) μm	Cenci Rate Z or +45° (MHz / cm^2)	Rate Z or +45° (MHz / cm^2)	RO Pitch ϕ (or -45°) μm	Cenci Rate ϕ or -45° (MHz / cm^2)	Rate ϕ or -45° (MHz / cm^2)
0	50	29.9	24.3	50	23.3	24.3
1	100	0.7	0.93	50	1.5	1.61
2	100	0.35	0.4	55	0.72	0.73
3	100	0.097	0.12	55	0.19	0.19
4	210	0.0076	0.0036	100	0.012	0.007
5	210	0.0041	0.0024	100	0.006	0.005

Mechanics: Layer0 design with striplets revised and L1-L5 module design started







SVT-TDR subchapters & editors

1. Vertex Detector Overview (12) – G. Rizzo
2. Backgrounds (4) – R. Cenci
3. Detector Performance Studies (6) – N. Neri
4. Silicon Sensors (8) – L. Bosisio
5. Fanout Circuits (8) – L. Vitale
6. Electronics Readout (28)
    1. Readout Chips (10) – V. Re
    2. Hybrid Design (10) – M. Citterio
    3. Data Transmission (8)– M. Citterio
    4. Power Supplies (1??) -???

    SVT DAQ (M. Villa) will be in the ETD section
7. Mechanical Support & Assembly (14) – S. Bettarini/F. Bosi
8. Layer0 pixel upgrade options (10) – G. Rizzo/L. Ratti/ + others
9. Services, Utilities (2) -??

- Chapter editors produced a first draft of detailed outline
- The first estimate of pages is too high: TOT ~ 92!
- We should try to end up with ~60-70 pages max.

SVT Parallels

11:00->*12:30* **Parallel 1 - SVT** (Convener: Giuliana Rizzo (*PI*)) (Francis Bancroft Bldg - room 240 (FB))

Description:

EVO Details:
http://evo.caltech.edu/evoNext/koala.jnlp?meeting=eBele2vtv9aaavIvauIB The web password is superb

People can connect via the EVO phone bridge, using an appropriate number from
http://evo.caltech.edu/evoGate/telephone.jsp and the following codes:
Phone Bridge ID: 10 9383 Phone Bridge Password: 5939

11:00	Introduction (10')	Giuliana Rizzo (*PI*)
11:10	Pixel & Strip FE Electronics Update (20')	Valerio Re (*PV*)
11:30	Update on activities in Bologna (20')	Filippo Maria Giorgi (*BO*)
11:50	Striplets performance in high background conditions (20')	Nicola Neri (*MI*)

14:00->*16:30* **Parallel 2 - SVT** (Mostly devoted to Mechanics discussion - room 240

14:00	Update on activities in UK (20')	Fergus Wilson (*RAL*)
14:20	SVT Mechanics (20')	Filippo Bosi (*PI*)
14:40	Technical Discussion on SVT Mechanics (50')	

16:00->*17:30* **Parallel 3 - SVT** (Convener: Giuliana Rizzo (*PI*)) (Francis Bancroft Bldg - room 240 (FB 240))

16:00	Update on HDI design and periphel electronics (20')	Mauro Citterio (*MI*)
16:20	Update on activities in Trieste (phone) (20')	Carlo Stella (*TS*)
16:40	Update on background simulation (phone) (20')	Riccardo Cenci (*PI*)