Control and readout in the 4D-MPET detector: preliminary results and inputs for the discussion

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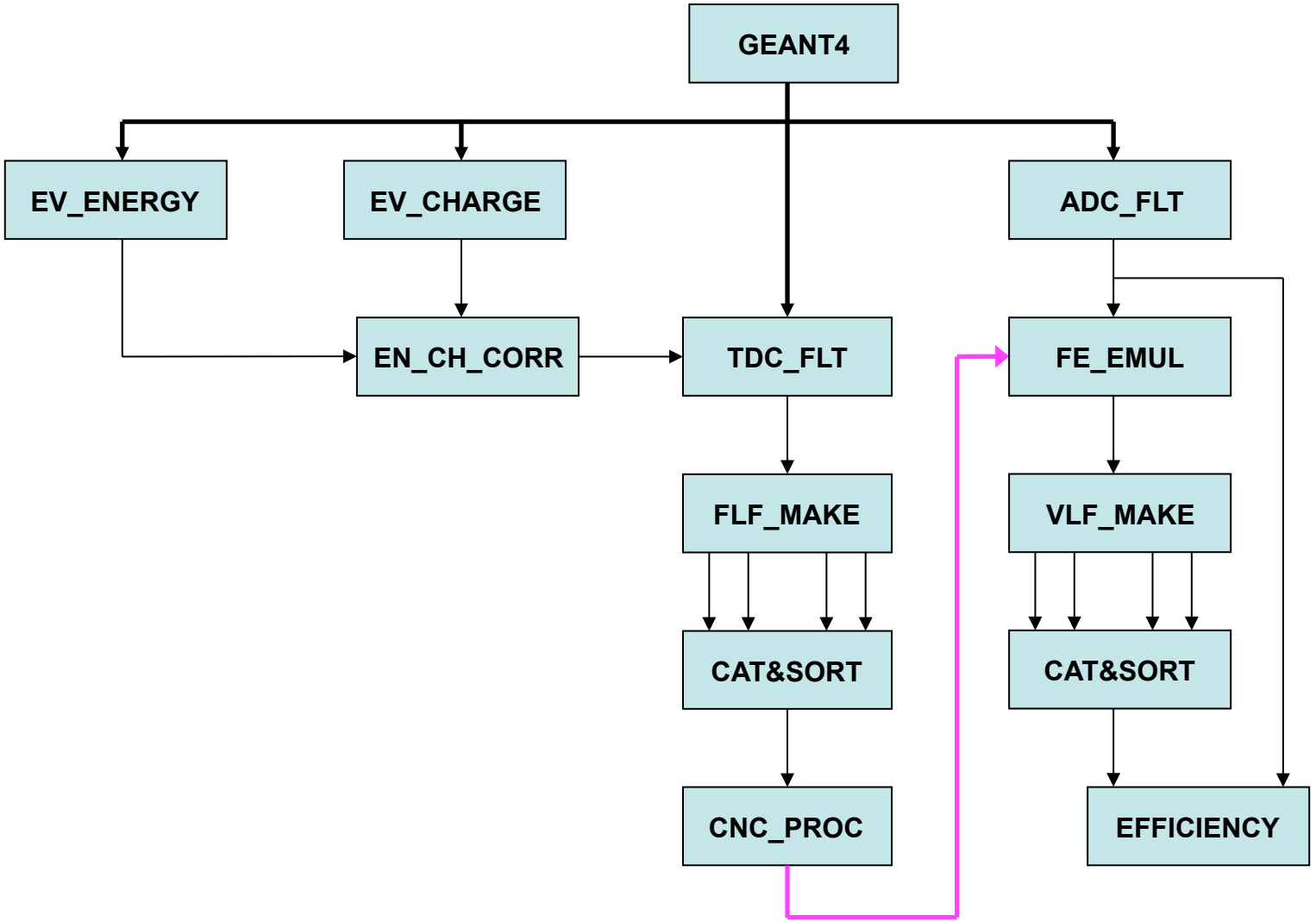
Outline

1. GEANT4 simulations & DAQ architecture
2. VHDL modeling of components of the 4D-MPET control and readout systems and FPGA emulation
3. Some architectural issues

GEANT4 simulations

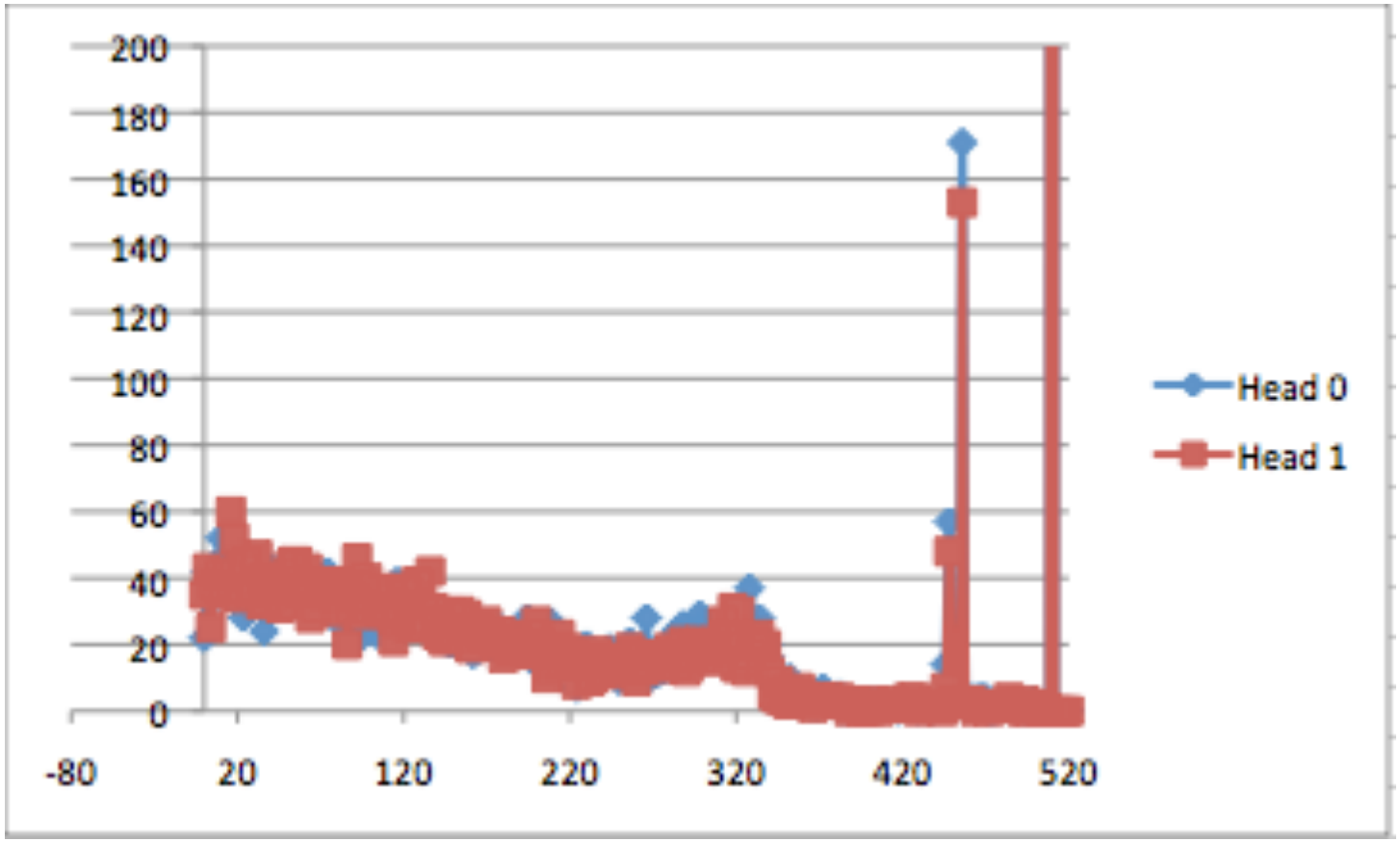
- Data from GEANT4 simulation can be used to characterize and compare algorithms, protocols and hardware solutions:
  - thresholds on TDC data
  - frame size and link speed
  - size of data buffers in FE ASIC (if required)
  - …
- PERL scripts are ideal to perform analysis and processing of data embedded in text files

PERL Data Flow



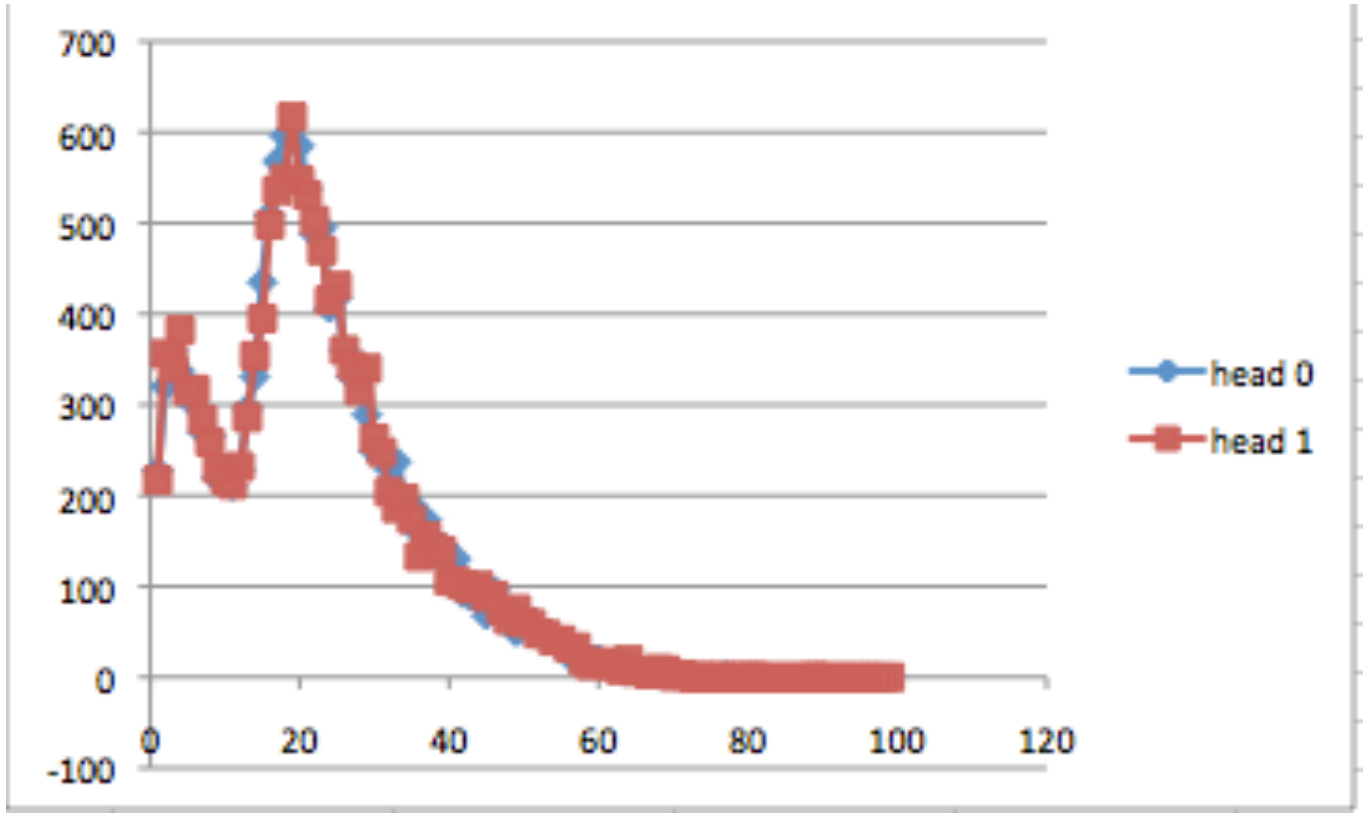
Energy distribution

event_energy.pl -> distribution of the energy



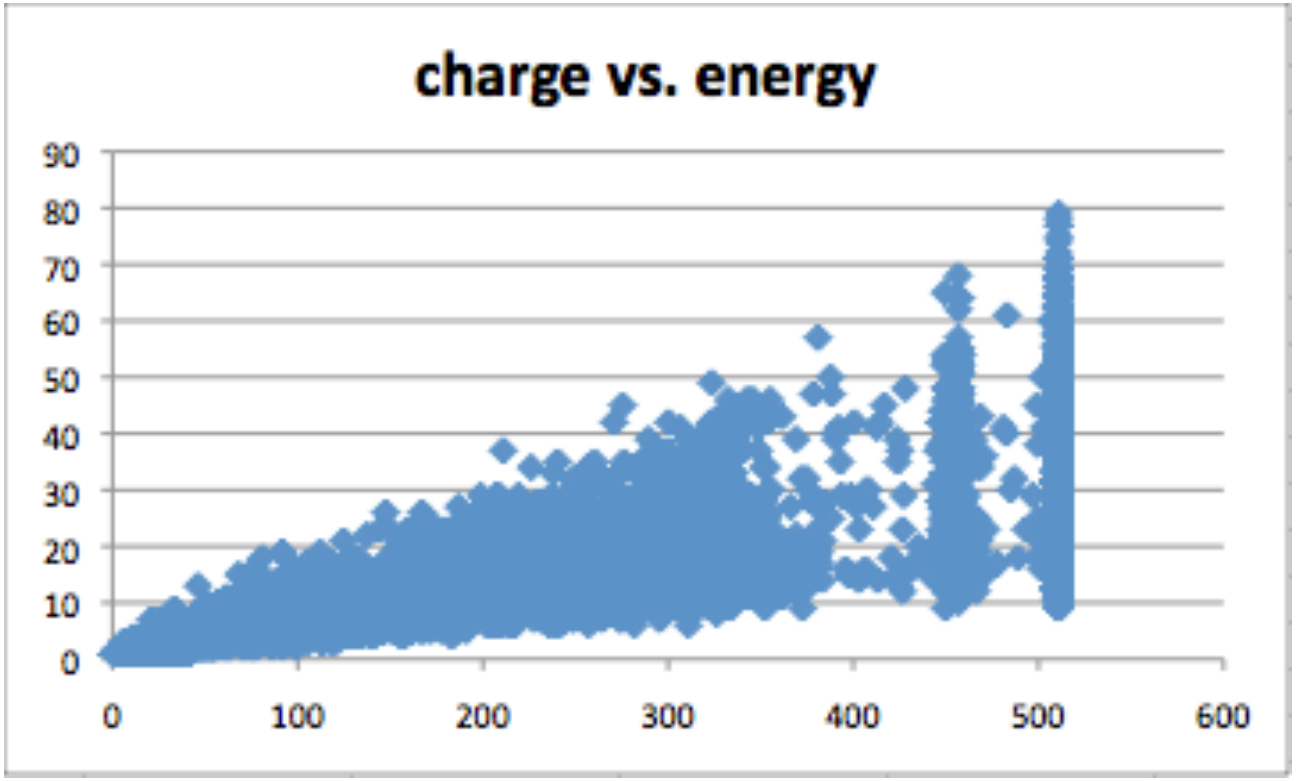
Charge distribution

event_charge_m.pl -> distribution of the max charge released in the pixels in each event (window = 20ns)



Energy/Charge correlation

en_ch_corr.pl -> correlation between the max charge released in the pixels in each event and the energy



FLF generation (1)

- **perl tdc_flt.pl tdc_hits_in tdc_hits_out tdc_win hit_n**

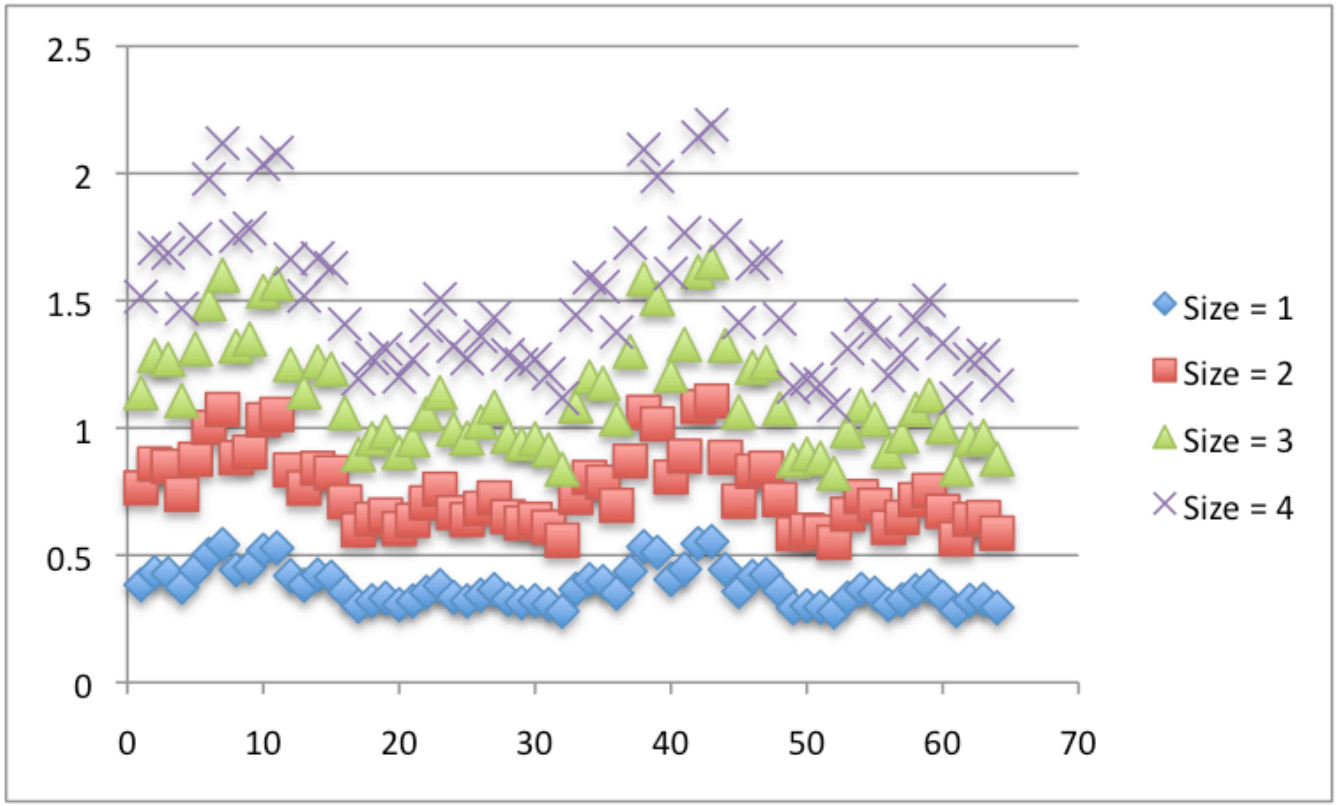
  Only pixels with at least hit_n hits within tdc_win since the first one generate data
- **perl fe_flt.pl hits_tdc_out**

  For each FE ASIC, Time Stamp (TS) and Fine Timing (FT) of accepted hits are evaluated as input data of the coincidence processor
- **perl make_flf.pl frame_size**

  For each FE ASIC, FLFs are generated and required bandwidth and transmission efficiency are evaluated

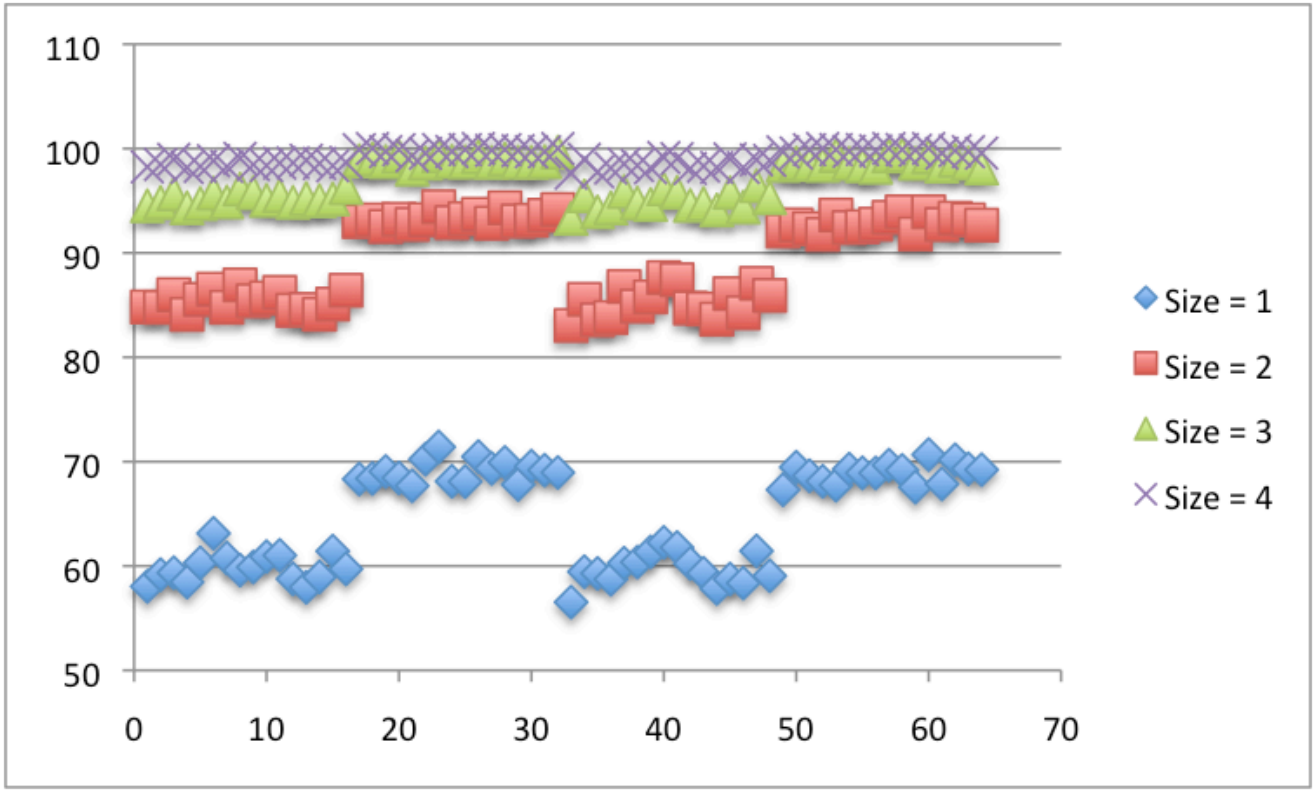
FLF generation (2)

Bandwidth occupancy (%) vs. frame size



FLF generation (3)

Transmission Efficiency (%) vs. frame size



FE ASIC emulation (PERL)

Hit data

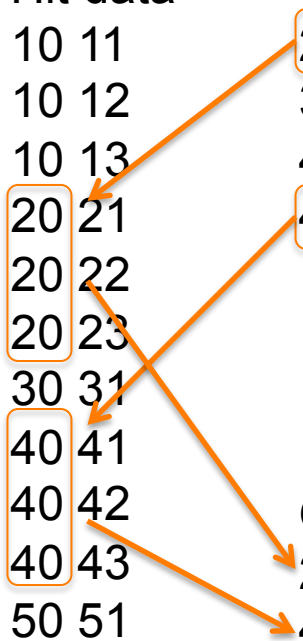
10 11
10 12
10 13
20 21
20 22
20 23
30 31
40 41
40 42
40 43
50 51
60 61
60 62
60 63
60 64

Coincidence data

25
32
41
45

Output data

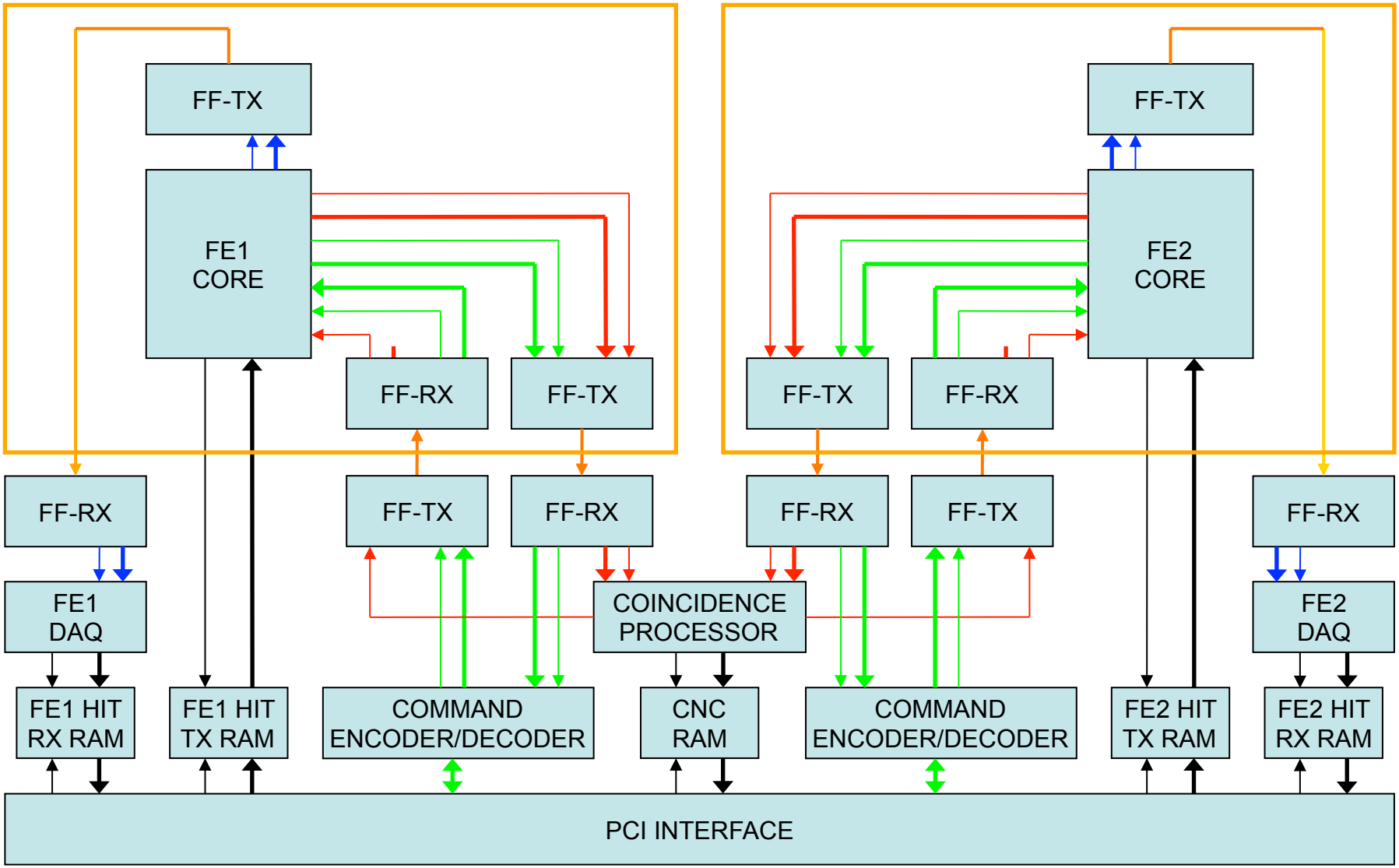
20 21 22 23
40 41 42 43



Logfile

hit read -> data @ 10 (11)
time = 1 0
time = 2 0
time = 3 0
time = 4 0
time = 5 0
time = 6 0
time = 7 0
time = 8 0
time = 9 0
time = 10 0
push 11 into data(10)
cnc read -> 25
hit read -> data @ 10 (12)
push 12 into data(10)
hit read -> data @ 10 (13)
push 13 into data(10)
hit read -> data @ 20 (21)
…

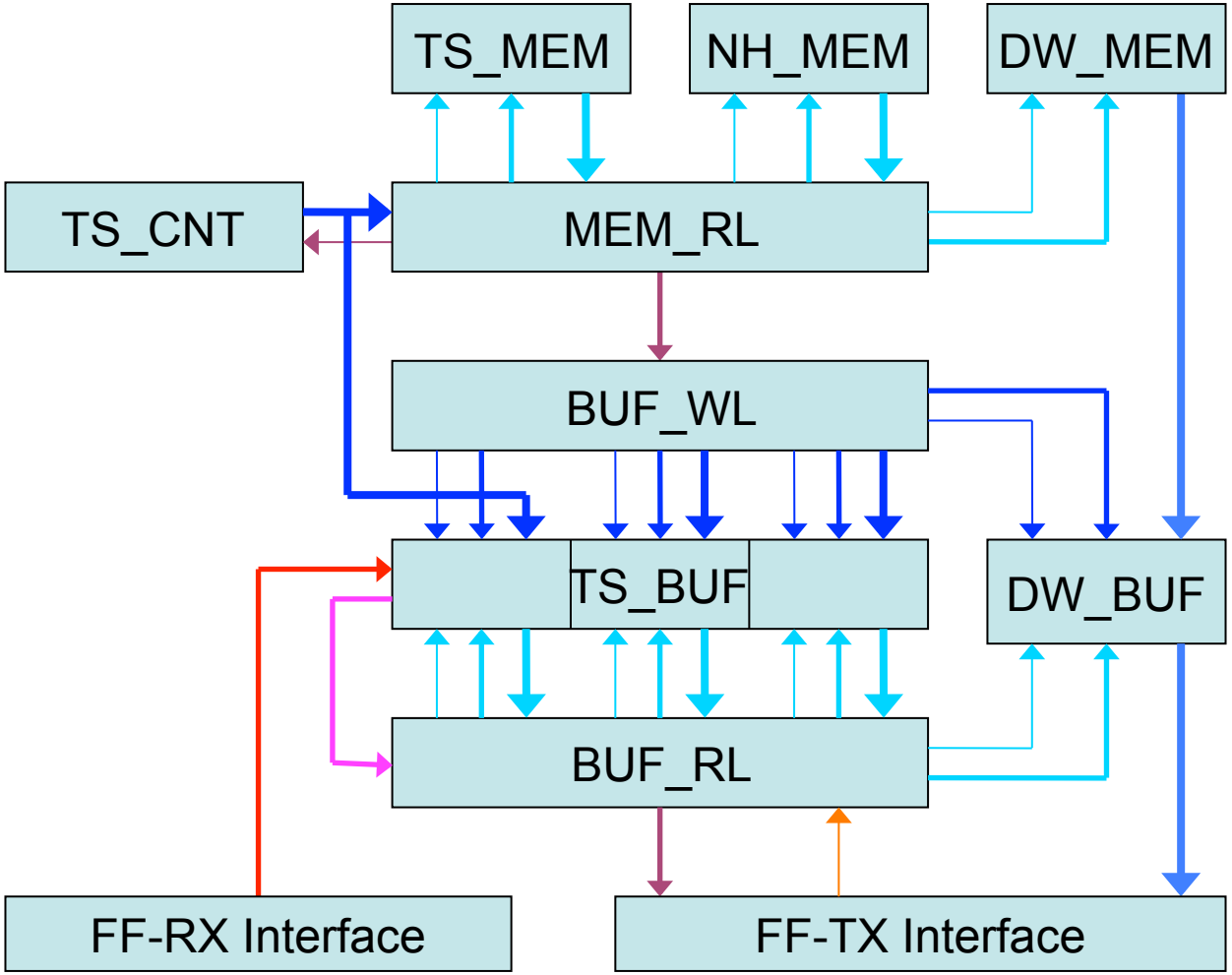
4D-MPET emulator (1/2)



4D-MPET emulator (2/2)

- FE configuration is defined in the GUI and downloaded into FE registers through the command encoder and the TTC down-link (green lines)
- Data generated in read accesses to FE registers are transmitted to the command decoder through the TTC up-link (green lines)
- The Run Controller embedded in the FE emulator reads the HIT TX RAM and starts the generation of hit data in the TDC (channel and fine timing) and in the FE (channel and charge)
- Trigger information are transmitted to the conincidence processor through the TTC up-link (red lines)
- The coincidence processor evaluates the coincidence condition between data generated by two FE circuits and generates a trigger that is transmitted to the FE circuits through the TTC-downlink (red lines)
- When a trigger is received in a FE circuit, raw data are transmitted to the DAQ system through the DAQ up-link (blue lines)

FE core modeling (1/4)



FE core modeling (2/4)

- Data RAMs
  - TS_RAM -> time stamps with raw data to be transmitted
  - NH_RAM -> number of hits for each time stamp
  - DW_RAM -> hit data (data words)
- Memory Read Logic (MEM_RL)
  - When the TS counter output (TS_CNT) is equal to the current output of the TS_RAM:
    - NH data words are downloaded from the DW_RAM
    - The data valid line is kept high and the TS counter is disabled for NH clock cycles

FE core modeling (3/4)

- Buffer Write Logic (BUF_WL)
  - When the data valid goes high the TS counter data word are loaded into DW_BUF (if there are free locations)
  - When the last data word has been loaded the following data are loaded into TS_BUF
    - Time stamp of the clock cycle when the data valid became high
    - Starting address (S_PNT) in the DW_BUF
    - End address (E_PNT) in the DW_BUF
- Buffer Read Logic (BUF_RL)
  - rdaddr is the address of the TS_BUF current location
  - If TS (rdaddr) = TS_CNT – latency => rdaddr++
  - If TS (rdaddr) = TS_CNT => hit data are downloaded from the HIT RAM from the address E_PNT to the address S_PNT (data_valid high)

FE core modeling (4/4)

TS_RAM

TS1	S_PNT1	E_PNT1
TS2	S_PNT2	E_PNT2
TS3	S_PNT3	E_PNT3
TS4	S_PNT4	E_PNT4

HIT_RAM

S_PNT1	Hit_1_1
	Hit_1_2
	Hit_1_3
S_PNT2	Hit_2_1
	Hit_2_2
S_PNT3	Hit_3_1
	Hit_3_2
	Hit_3_3
	Hit_3_4
S_PNT4	Hit_4_1

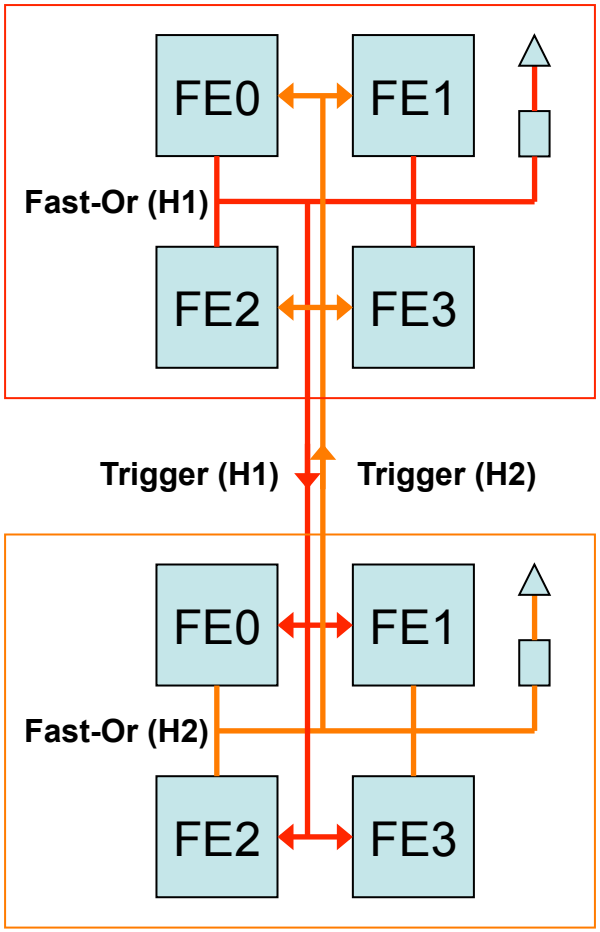
Some architectural issues

- Coincidence
  - Where and how?
  - Three approaches considered:
    - “Wired-Or”
    - Coincidence Processor
    - 2-Step Coincidence
- On-Chip Buffering
  - Level 1 buffers in the FE ASICs required?
- Module Controller
  - Data merge on the head on a digital data concentrator ASIC possible/useful?

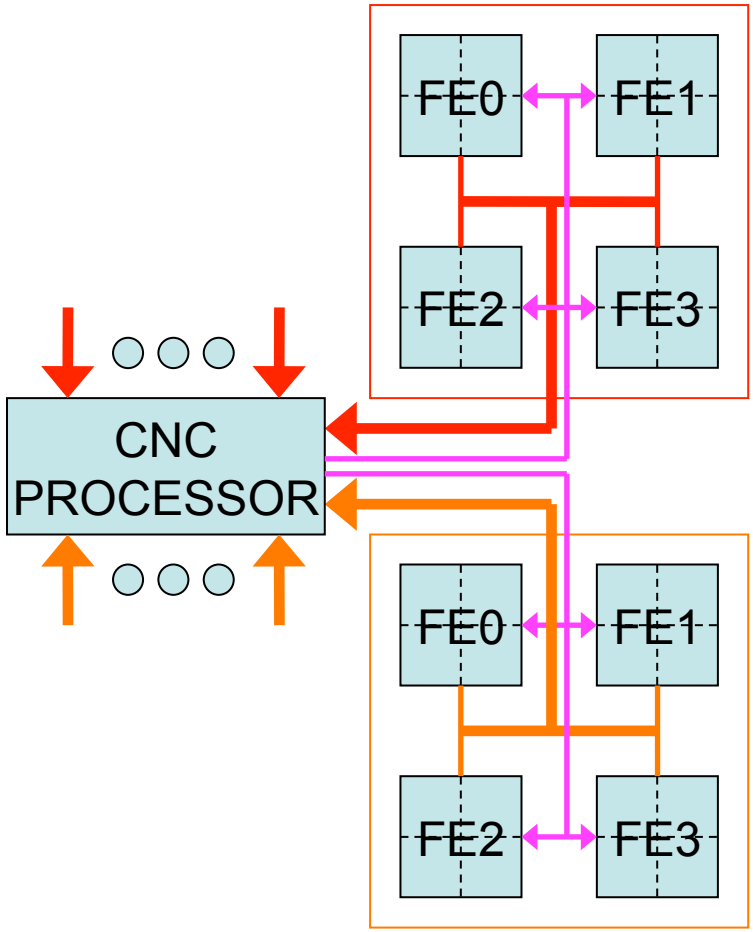
Coincidence (1/5)

- “Wired-Or” approach (BASIC32)
  - On-chip fast-or of pulses associated to detected hits is performed
  - Wired-or of fast-or signals is performed in each head and transmitted to the other head
  - Coincidence is evaluated on chip by using local wired-or and wired-or from the other head
- “Coincidence Processor” (CP) approach:
  - Timing information are transmitted from each FE to the CP (if required, spatial information can be attached to timing information)
  - Coincidence is evaluated in the CP
  - Coincidence trigger is transmitted to FE to start the transmission of the “raw” data
- “2-Step Coincidence” approach:
  - Timing information from both sides are used in each head to implement a Level-1 coincidence (correlation) algorithm for data rate reduction
  - Data-Rate reduction will allow the transmission of all the FE data to the “off-line” Level-2 coincidence processor and to the DAQ system

Coincidence (2/5)

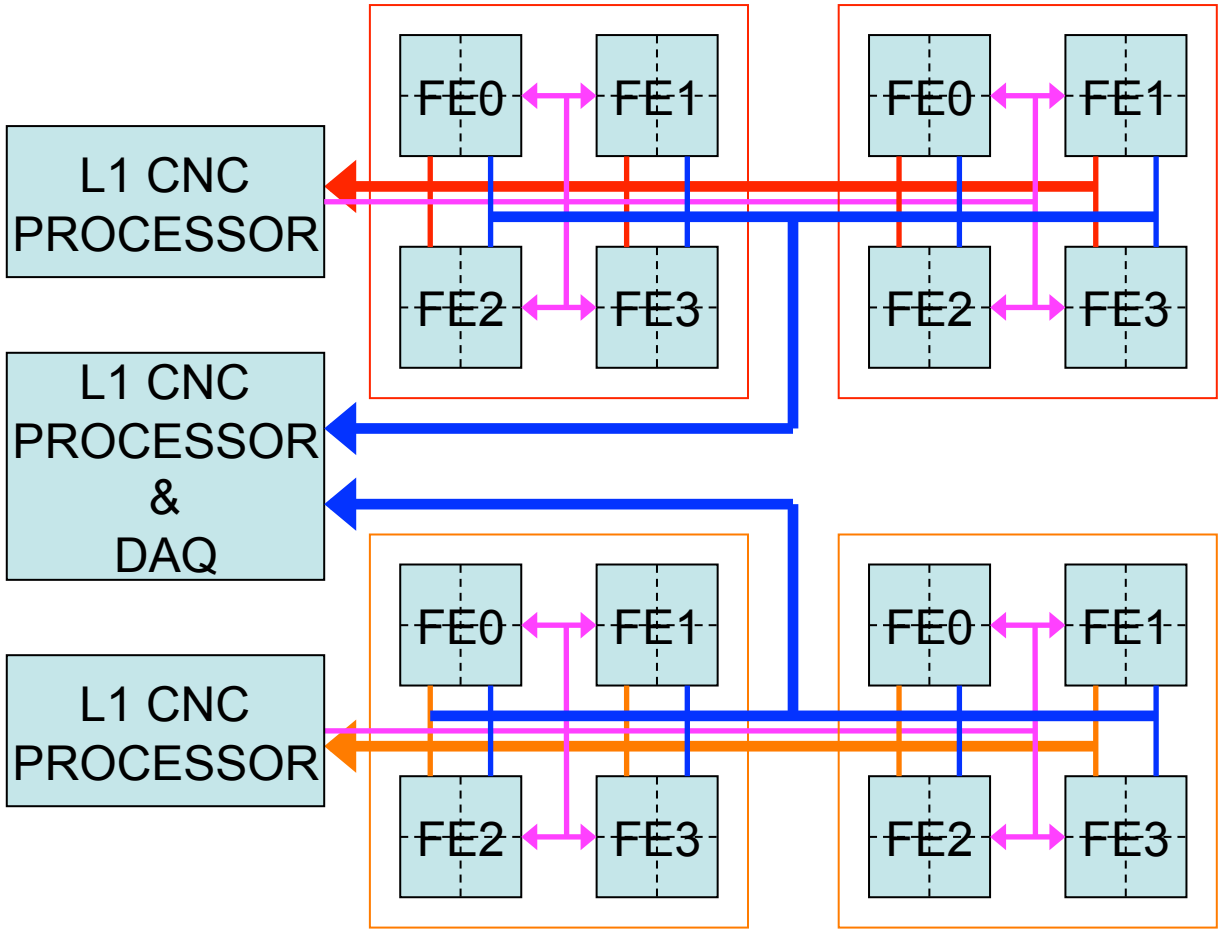


“Wired-Or” approach



“Coincidence Processor” approach

Coincidence (3/5)



“2-Step Coincidence” approach

Coincidence (4/5)

- Advantages of the CP approach:
  - High resolution is allowed in the coincidence algorithm
    - timing information are evaluated locally (e.g.: in the TDC), serialized and transmitted as frames
    - There is no influence of physical links (e.g.: length) on the timing information received in the CP
  - More sophisticated coincidence algorithms can be implemented (e.g.: taking into account spatial information as head, FE, pixel)
  - The system is intrinsically scalable in view of the development of more complex structures

Coincidence (5/5)

- Advantages of the 2-Step approach:

?

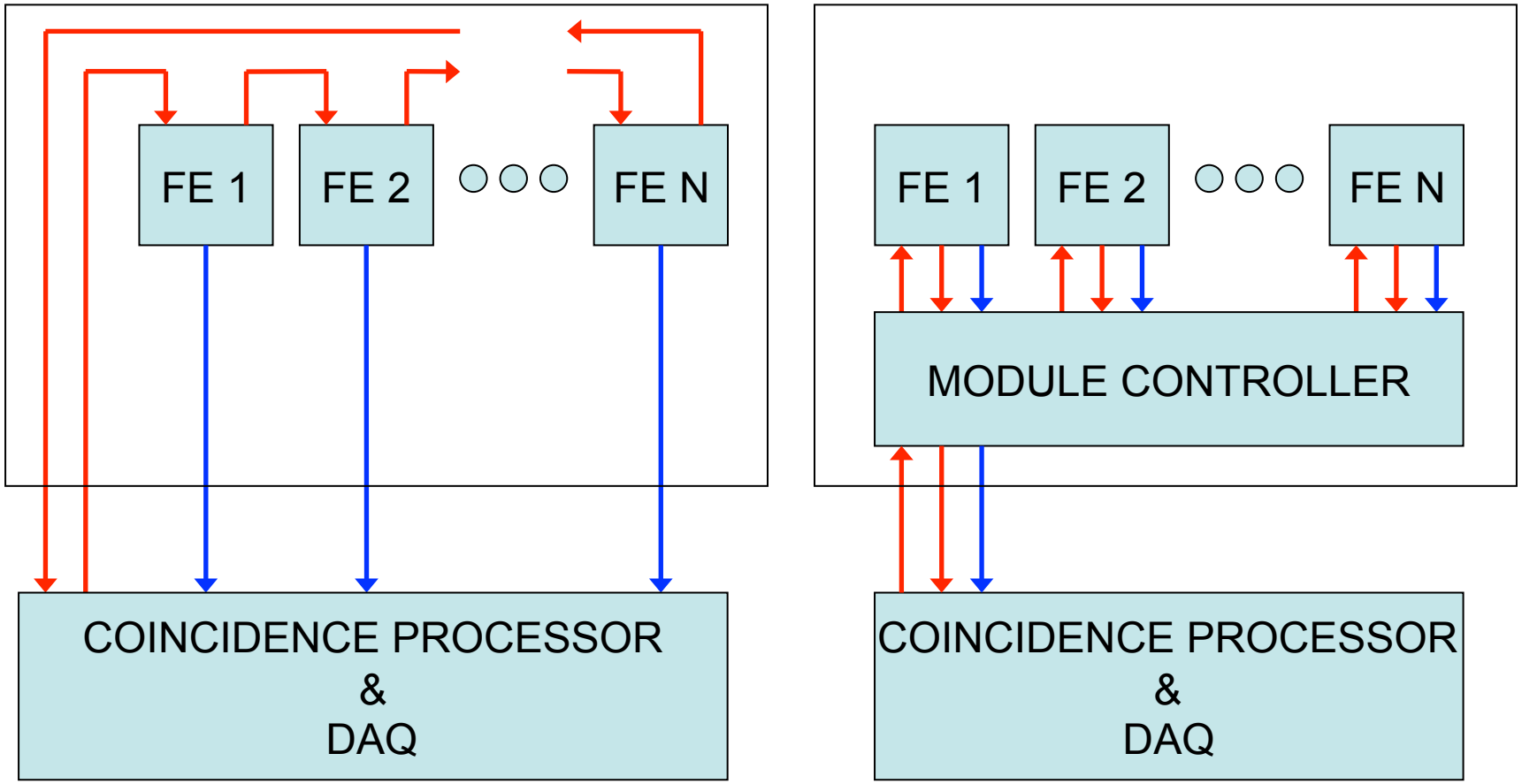
On-Chip Buffering

- Data Rate and latency in coincidence evaluation and transmission could force to use on-chip buffers
- This is not a great issue (common approach in FE ASICs for HEP): buffers and buffer readout logic are fully digital modules
- Buffer size (and need) to be evaluated through high level simulations (Guido, Richard, Francesco)

Module Controller (1/2)

- A Module Controller ASIC could be developed to:
  - merge data streams from FE ASICs into one data stream to Coincidence Processor and DAQ
  - distribute Timing, Trigger and Control (TTC) signals (“Star” architecture)
- Advantages
  - Reduced number of optical links
  - Possible “relaxed” specifications on link speed from FE ASICs
  - No need of a redundant ring architecture for the distribution of TTC signals
  - Possible implementation of an On-Head Level 1 Coincidence Processing
- High level simulations (Guido, Richard, Francesco) required to estimate data rates from FE ASICs and required number of readout links

Module Controller (2/2)



Conclusions

- Many issues still to be discussed
- System architecture to be defined as soon as possible (according to simulation results) before finalizing any chip design
- Modularity and scalability wherever it is possible in view of future developments