

MLR1: CMOS MAPS technology validation for ALICE ITS3

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Summary. — The second ALICE Inner Tracking System upgrade project (ITS3), to be completed during LHC Long Shutdown 3 (LS3, 2026-2028), will dramatically reduce the Inner Barrel (IB) detectors' material budget and thus improve the ITS tracking capabilities (detection efficiency and track resolution). For this purpose, the ITS3 project envisions replacing the current ITS2 IB with 6 flexible, truly cylindrical half-layers, supported only by a carbon foam frame and cooled down by an air system. The ITS3 will be made of CMOS Monolithic Active Pixel Sensors (MAPS) produced with a 65 nm technology. This innovative project has required a remarkable effort in terms of R&D, going from the design to the testing of small devices. In this contribution studies on the first small test device submission (MLR1) will be presented. Those studies have been carried out with the goal to compare different silicon chip manufacturing processes, doping profiles, front-end configurations, and generally validate 65 nm technology for the ITS3 CMOS MAPS.

1. – Introduction

During the LHC Long Shutdown 2 (LS2, 2019-2022), ALICE sub-detectors underwent an upgrade [1]. In particular, the ALICE Inner Tracking System (ITS) was upgraded to its second (and current) version, ITS2, based on ALPIDE chips. ALPIDEs make use of CMOS Monolithic Active Pixel Sensors (MAPS), built with the 180 nm technology and integrated readout circuitry. ALICE ITS2 consists of 7 layers of silicon detectors, structured in staves extending along the beam axis [1] and covering a radial distance from the interaction point of 22 mm up to 395 mm. The 3 innermost ITS2 layers are collectively known as Inner Barrel (IB), whereas the remaining 4 are known as Outer Barrel (OB). The ITS2 has successfully limited the detectors' material budget to 0.36% X_0 per layer (X_0 being a radiation length) for IB and 1.10% X_0 per layer for OB, contributing to a better pointing resolution and overall superior tracking performance even at low transverse momenta p_T . The smaller distance between IB and the interaction point (22 mm compared to 39 mm of ITS1) and the higher granularity of state-of-the-art ALPIDE chips have also played a role in this improvement, allowing studies on shorter-lived particles.

Moreover, ITS2 can sustain data flow for interaction rates up to 1 MHz in pp collisions and 50 kHz in Pb-Pb [1].

In the ITS3 upgrade project, the 3 IB layers will be replaced with 6 flexible, truly cylindrical silicon half-layers, made of stitched sensors (fig. 1). The new ITS3 chips will be built with the TPSCo 65 nm technology. An important advantage of the upgraded ITS is that ITS3 layers can be held in place by carbon foam spacers, hence reducing the needed material budget compared to the present ITS2 stave structure [1, 2]. Moreover, it is expected that by keeping the ITS3 power consumption below 40 mW/cm², the ITS2 water cooling system can be replaced by air cooling, thus contributing to a reduced material budget. IB layers will be closer to the interaction point, with an inner radius of 19 mm, and the material budget for the future ITS3 is expected to be thinned down to 0.07% X₀ per layer, excluding the carbon fiber foam spacers (0.09% on average). According to simulation results, ITS3 tracking performance will improve with respect to ITS2 [2, 3]. For reference, tab. I summarises the main differences between ITS2 and ITS3.

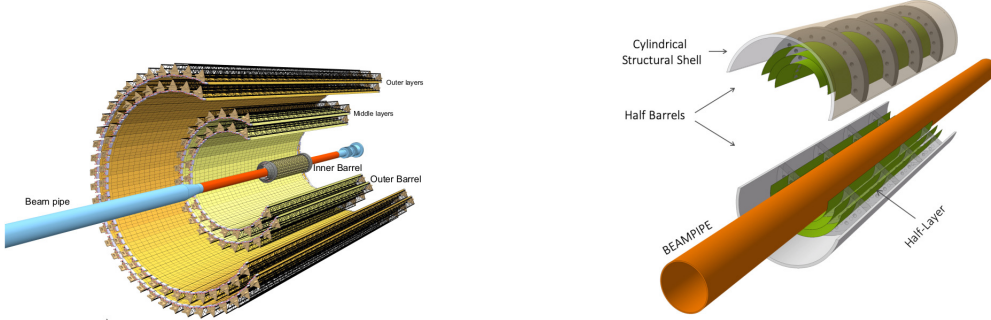


Fig. 1. – Current ITS2 layout [1] (left) vs ITS3 project [2] (right).

	ITS2	ITS3
Technology	MAPS 180 nm	MAPS 65 nm
L0 radius	22 mm	19 mm
Material budget per layer	0.36% X ₀	0.07% X ₀
Pixel size	27 $\mu\text{m} \times 29 \mu\text{m}$	20 $\mu\text{m} \times 22.5 \mu\text{m}$
Pseudo-rapidity coverage	$ \eta \leq 1.3$	$ \eta \leq 2.5$
Cooling system	Water	Air

TABLE I. – Summary of ITS2 vs ITS3 Inner Barrel features [1, 3].

The upgrade to ITS3 involves several R&D milestones, one of which is the validation of the TPSCo 65 nm CMOS MAPS technology for ALICE ITS3 and investigation of its feasibility with respect to the ITS3 goals [3]. Small test devices from the Multi-Layer Reticle 1 (MLR1) submission were studied until late 2023 to fulfill this task: Analog and Digital Pixel Test Structures (APTS and DPTS), and Circuit Exploratoire 65 nm (CE65). In the following sections, at first, an overview of 65 nm technology and MLR1 devices will be given. Secondly, we will discuss the results obtained on APTS and DPTS test measurements, both from laboratory and beam setups, in which the chips' charge

collection efficiency, detection efficiency and spatial resolution were investigated.

2. – Overview of 65 nm technology validation tests

The choice of 65 nm technology for the upcoming ITS3 MAPS was motivated by its higher density of circuits and larger diameter of silicon wafers. In fact, silicon wafers with diameter of 300 mm can be produced with the 65 nm technology for stitching, allowing for the production of sensor with a length of 27 cm [3]. However, adapting this technology to physics measurements at ALICE with the future ITS3 sensors requires assessment and validation of the new chips' performances in terms of - among others - charge collection efficiency, detection efficiency, spatial resolution and radiation hardness. Being closer to the interaction point, the ITS3 is expected to deal with a radiation load larger by about 70% than ITS2, up to an estimated $10 \text{ kGy TID} + 10^{13} \text{ 1 MeV n}_{eq} \text{ cm}^{-2} \text{ NIEL}$ [2].

MLR1 chips, submitted in 2021, were among the first test structures designed for that purpose. They included 55 different models of small test devices, consisting in $1.5 \text{ mm} \times 1.5 \text{ mm}$ pixel matrices of different dimensions, pixel pitches, and designs. In particular, three different pixel designs have been developed (fig. 2), all with different doping profiles and depletion region shapes. In *standard* design (currently used in ITS2 ALPIDE chips, fig. 2(a)), the pixel is not fully depleted and the depletion region has an approximately spherical shape around the n-well collection diode. The *modified* design (fig. 2(b)) features an additional low dose n-type implant below the MOS and collection diodes, with a diffuse planar depletion region. Similarly, in *modified with gap* design (fig. 2(c)) there is a $2.50 \mu\text{m}$ wide ($1.25 \mu\text{m}$ per pixel edge) gap in the n-type implant, strengthening the electric field near pixel edges [3, 4]. Moreover, 4 different doping profiles, or splits (split 1 to 4), and 4 geometries of collection diodes (reference, larger n-well, smaller p-well, finger-shaped p-well) have been tested and compared [5].

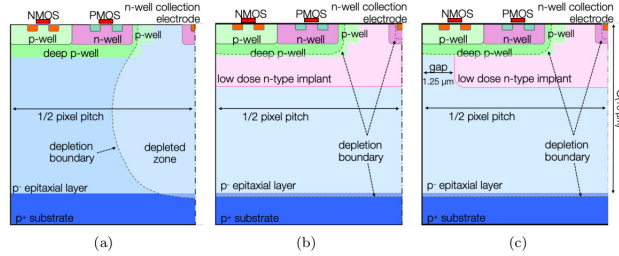


Fig. 2. – Three different designs of small test device pixel for the ITS3 R&D: *standard* (a), *modified* (b) and *modified with gap* (c) [5].

Small test devices fall into 3 families, differing mainly in pixel matrix dimensions and readout electronics: Analog and Digital Pixel Test Structures (APTS and DPTS) and Circuit Exploratoire 65 nm (CE65) [3] (fig. 3).

- **Analog Pixel Test Structures (APTS):** small 6×6 pixel matrices with direct analog readout, where only the innermost 4×4 sub-matrix is actively readout to avoid edge effects on the outermost pixels. Pixels vary in pitch, from 10 to $25 \mu\text{m}$, and design, as shown in fig. 2. Output buffer is either a simple source-follower, as in the APTS-SF chips, or includes an additional unity gain operational amplifier for enhanced time resolution, as in the APTS-OA model [3, 5].

- **Digital Pixel Test Structures (DPTS):** small 32×32 pixel matrices with digital readout, including an amplifier, a differential discriminator and a Current Mode Logic (CML) output. Pixels have a $15 \mu\text{m}$ pitch and *modified with gap* design. Information about signal position within the matrix are time-encoded in the time distance and duration of two output pulses, while the signal amplitude is time-encoded in Time-over-Threshold [3, 6].
- **Circuit Exploratoire 65 nm (CE65):** there are 4 variants of CE65, three of which are 64×32 matrices of $15 \mu\text{m}$ pixels and the fourth is a 48×32 matrix of $25 \mu\text{m}$ pixel. CE65 devices are divided in three sub-matrices, of which two have an amplifier output buffer (one is AC- and the other is DC-coupled) and the third has a simple DC source-follower output buffer. The sub-matrices signals are collected by a rolling shutter readout [3].

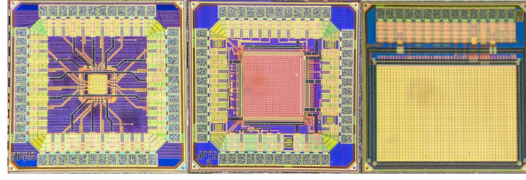


Fig. 3. – Pictures of MLR1 test device categories: APTS (left), DPTS (center) and CE65 (right) [3].

3. – Small scale device test results: APTS and DPTS

Test measurements on APTS and DPTS small scale devices yielded significant results regarding the efficiency and spatial resolution achievable with the 65 nm technology, even beyond the goals set for ITS3 sensors, *i.e.* 99% detection efficiency and $5 \mu\text{m}$ resolution [2, 3]. Tests were carried out with radioactive source and charged particle beams, on devices of different pixel designs and pitches. Radiation hardness of 65 nm devices was also investigated, in order to evaluate the impact of (non-)ionizing radiation on chip performances at varying TID and NIEL levels. To that purpose, devices were irradiated with X-rays at CERN and neutrons at JSI Ljubljana.

Laboratory tests and results. In the laboratory setup, Devices Under Tests (DUT) were exposed to X-ray ^{55}Fe sources, to acquire and compare the resulting readout signal spectra. In fig. 4 the spectra acquired on APTS-SF devices (*standard* and *modified with gap*) with different pitches and NIEL levels are shown. The spectra are expected to be dominated by the 5.9 keV line of ^{55}Fe (Mn- K_α), which is referred to as calibration peak. From its position and FWHM, input capacitance and energy resolution could be evaluated too. Another less intense line can be found at 6.5 keV (Mn- K_β). However, in fig. 4 we see that *standard* design spectra exhibit a broad peak at low signals, due to charge sharing effects. Charge sharing becomes less and less relevant in *modified* and *modified with gap* designs, where most charges are collected by a single pixel and the calibration peak is predominant. In the same figure, robustness under different NIEL levels was investigated on a $15 \mu\text{m}$ pitch *modified with gap* chip at irradiation levels from

0 up to 10^{16} 1 MeV n_{eq} cm^{-2} NIEL. Non-ionizing radiation could cause damage to the pixel crystal lattice and thus inhibit its charge collecting capabilities. On the other hand, ionizing radiations are expected to have a detectable impact on the in-pixel front-end circuitry and noise, but not on charge collection efficiency. This is why only NIEL levels have been varied for APTS devices, that were used mainly to study the in-pixel charge collection process [3].

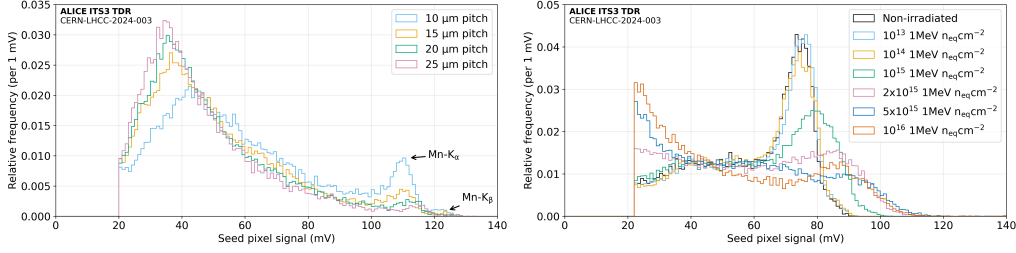


Fig. 4. – APTS-SF ^{55}Fe X-spectra comparison: *standard* pixel design, varying pitch (left) and *modified with gap* pixel design, 15 μm pitch, varying NIEL levels (right).

Input capacitance values were shown to be very small, down to 2 fF, while energy resolution varies between 5% and 10% [5]. Finally, in fig. 4 we see that up to 10^{14} 1 MeV n_{eq} cm^{-2} NIEL (1 order of magnitude larger than the ITS3 radiation hardness requirement), in *modified with gap* design the charge is mainly collected by one single pixel, pointing out a good charge collection efficiency of the chip.

Beam tests. In beam test setup, the DUTs were exposed to high-momentum charged particle beams to evaluate their detection efficiency and spatial resolution. For each DUT, particle tracks were reconstructed with the help of 6 collinear ALPIDE chips. Another APTS or DPTS device was used as a trigger in APTS and DPTS test beam, respectively, and scintillators provided an additional trigger in DPTS test beam setup. The DUT was aligned to the rest of the setup and cooled down to a temperature $T = 15^\circ\text{C}$ (for APTS tests) or 20°C (for DPTS).

Detection efficiency and spatial resolution were estimated from particle track: efficiency was defined as the ratio of tracks with an associated signal in the DUT over the total number of tracks, whereas spatial resolution was obtained from the standard deviation of track-to-cluster distance distribution.

In fig. 5 the results of the efficiency and spatial resolution measurements from DPTS test beams are shown. Both NIEL and TID levels were varied, and we observe that the detection efficiency holds above 99% up to 10^{14} 1 MeV n_{eq} cm^{-2} NIEL, with excellent performances at the expected ITS3 working conditions ($10 \text{ kGy TID} + 10^{13}$ 1 MeV n_{eq} cm^{-2} NIEL). Spatial resolution also holds slightly below the ITS3 goal ($5 \mu\text{m}$) and it is consistent with the expected resolution of $4.33 \mu\text{m}$ (pixel pitch/ $\sqrt{12}$) at $10 \text{ kGy TID} + 10^{13}$ 1 MeV n_{eq} cm^{-2} NIEL.

4. – Conclusions

Laboratory and test beam measurements have been performed on Analog and Digital Pixel Test Structures from MLR1 chip submission, to validate the 65 nm technology for ITS3 and assess the feasibility of ITS3 performance goals. Test measurements included

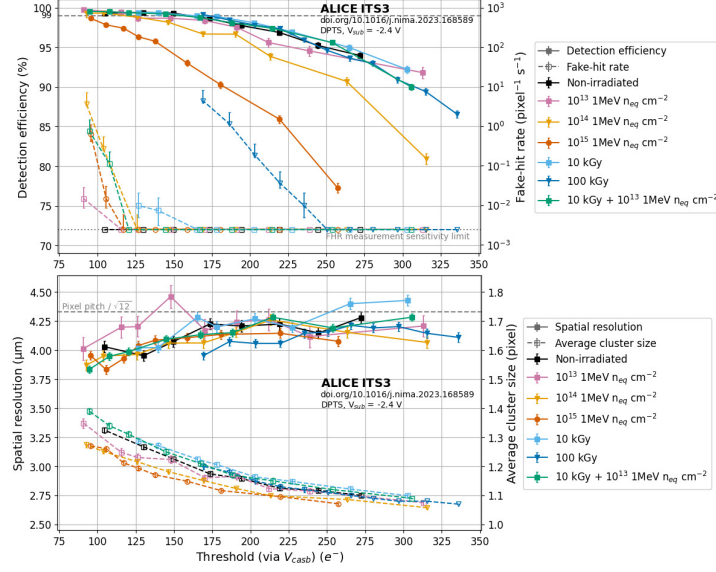


Fig. 5. – DPTS efficiency *vs* (top) and resolution (bottom) *vs* NIEL+TID irradiation levels.

X-ray spectra acquisition from a ^{55}Fe source in laboratory and exposing the DUTs to high-momentum charged particle beams, at different TID or NIEL irradiation levels. Laboratory tests have yielded low input capacitance values (down to 2 fF) and shown that the addition of a low dose n-type implant on the pixel epitaxial layer (particularly with gaps at pixel edges) improves charge collection efficiency. Test beam measurements pointed out that detection efficiency and spatial resolution meet the ITS3 performance goals even up to 10^{14} 1 MeV n_{eq} cm^{-2} NIEL irradiation levels, well beyond the expected ITS3 working conditions. Furthermore, in DPTS test beam measurements with different front-end configurations, detection efficiencies above 99% were achieved with a power consumption around 16 mW/cm^2 , fully in line with the goals for ITS3 air cooling [3].

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