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Preliminary results on monolithic CMOS sensors with gain layer in 110 nm technology for the ALICE 3 experiment

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In recent years, monolithic active pixel sensors (MAPS) have emerged as valid alternatives to hybrid detectors in the design of next generation high-performance silicon vertex and tracking detectors for high-energy physics (HEP) experiments and other fields of research like medical imaging and space applications. This option is among the technologies taken into account for the Time Of Flight detector of the ALICE 3 experiment for the LHC Run 5.
One of the main features of MAPS is that they can be implemented cost-effectively using a commercial CMOS process without the need for an expensive interconnection. In this context, Fully Depleted Monolithic Active Pixel Sensors (FD-MAPS) represent a state-of-the-art detector technology, as they have the advantage of collecting charges by drift, enabling a fast and uniform response over the pixel matrix. The ARCADIA project, in particular, is developing FD-MAPS with an innovative sensor design, which exploits backside bias voltage to fully deplete the sensor and to improve the charge collection efficiency and the timing performances.
Recent developments have addressed the possibility of introducing a gain layer in MAPS. Thanks to the signal multiplication, a higher signal to noise ratio can be reached, translating into a lower power consumption with respect to standard MAPS without gain. This peculiarity makes these devices very attractive for space applications, where low power consumption is strongly desired.
This work illustrates the first characterization results on the monolithic CMOS sensors with additional gain layer, based on a standard 110 nm CMOS technology developed in collaboration with LFoundry for the third run of the ARCADIA project. Laboratory measurements will be presented, together with preliminary results from a test beam conducted at PS, CERN. To conclude, the future perspectives and the next steps in the ongoing R&D will be pointed out.

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