

Preliminary results on monolithic CMOS sensors with gain layer in 110 nm technology for the ALICE 3 experiment

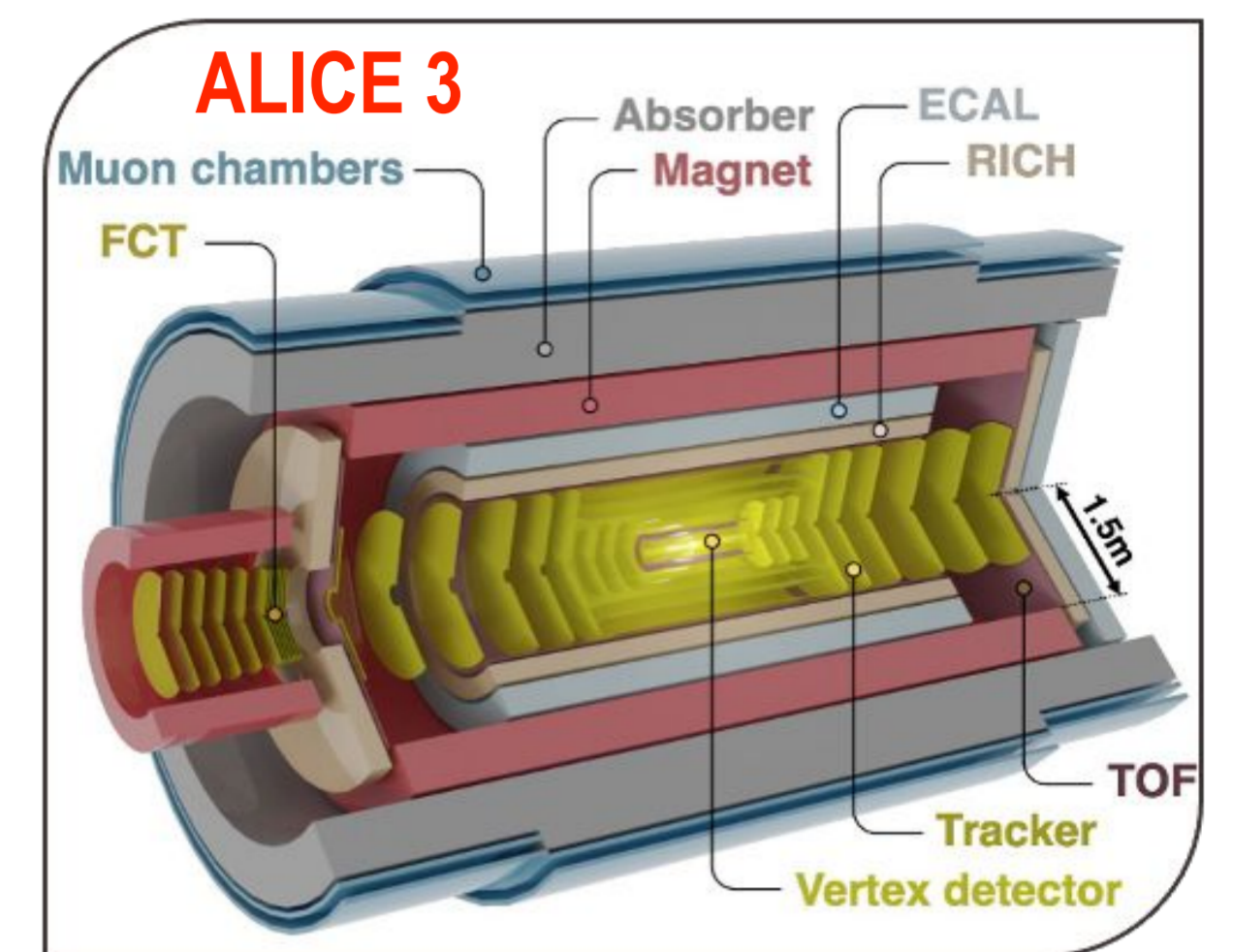
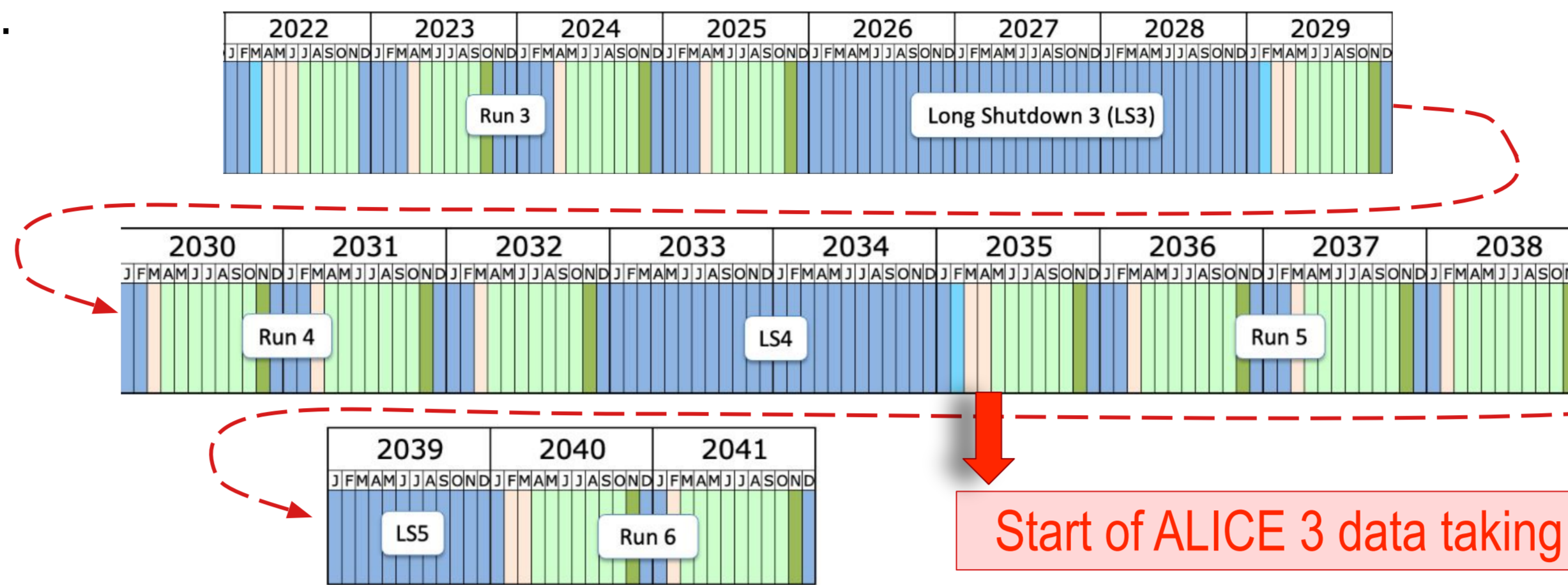
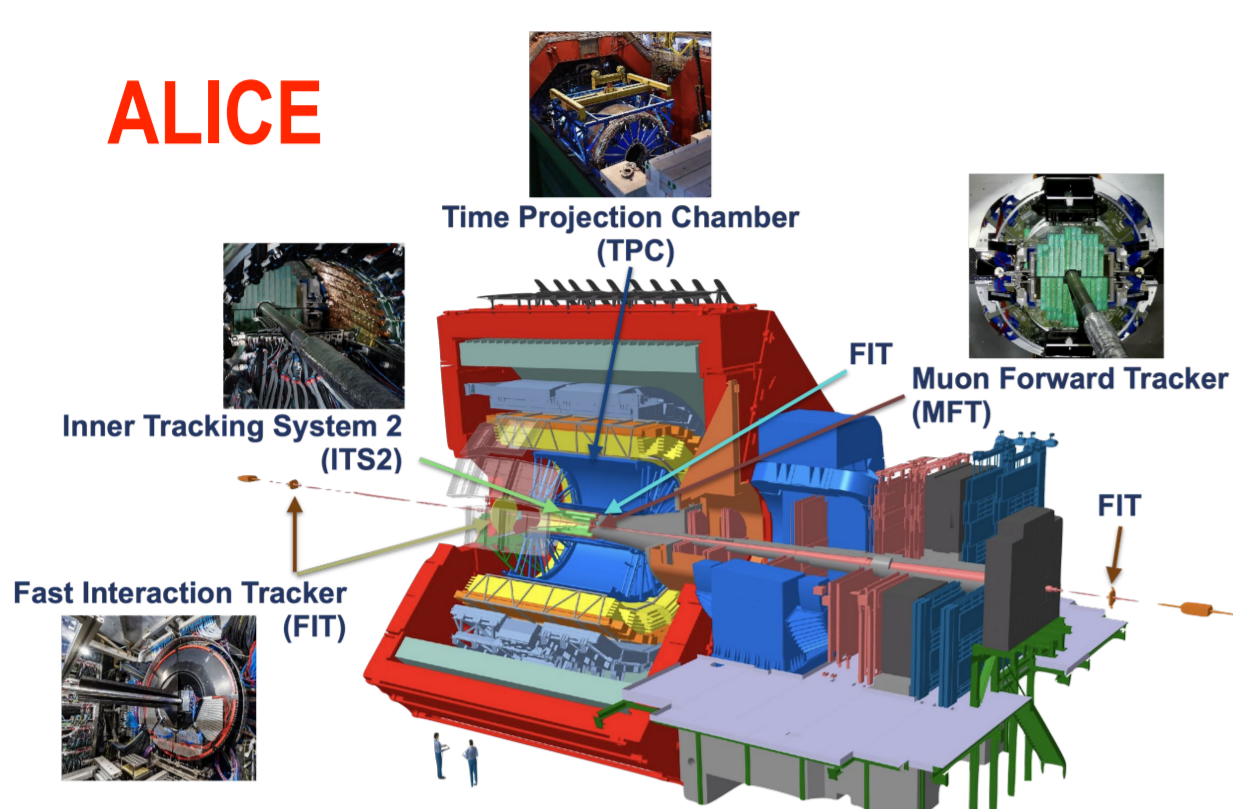


Chiara Ferrero*
on behalf of the ALICE and ARCADIA collaborations
*Politecnico di Torino and INFN Sez. di Torino



Context and motivation: the ALICE 3 upgrade

▶ **Monolithic Active Pixel Sensors (MAPS)** based on the CMOS Imaging Sensor (CIS) technology are used in ultra-light large tracking systems of various high-energy physics (HEP) experiments like **ALICE (A Large Ion Collider Experiment)** at the CERN LHC. They are considered for many future HEP applications, in particular for **ALICE 3**, the next-generation heavy-ion physics experiment proposed for the LHC Run 5 and 6.



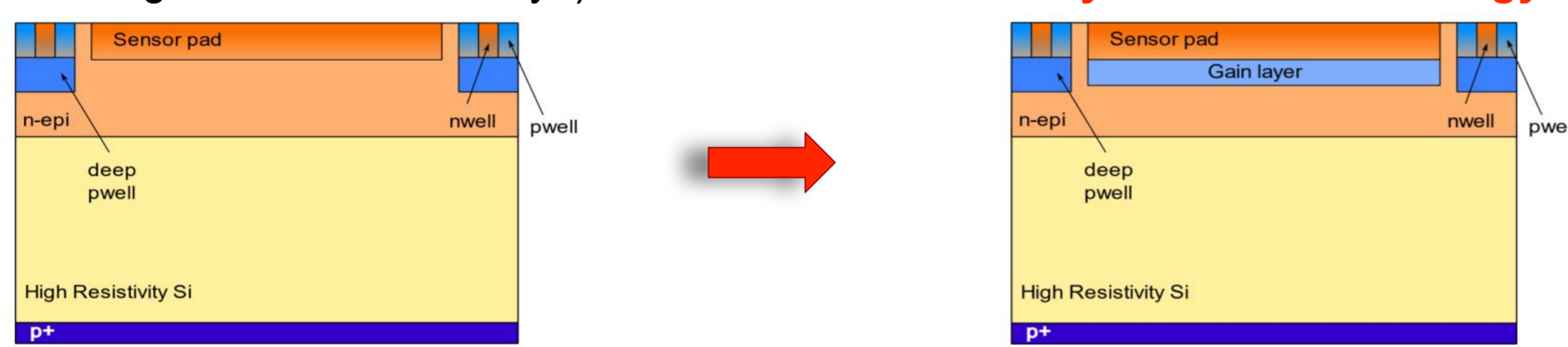
▶ **ALICE 3 TOF detector:** dedicated to Time Of Flight measurements. The required time resolution of **20 ps** will provide accurate particle identification information. Other TOF requirements: material budget 1-3% X_0 per layer, power consumption limit: 50 mW/cm²

The sensor concept

▶ Different silicon-based technologies are under study for the ALICE 3 timing layer: LGAD, SPAD or MAPS with gain. Timing with silicon sensors:

$$\sigma_t^2 = \sigma_{\text{Time Walk}}^2 + \sigma_{\text{Landau Noise}}^2 + \sigma_{\text{Distortion}}^2 + \sigma_{\text{Jitter}}^2 + \sigma_{\text{TDC}}^2$$

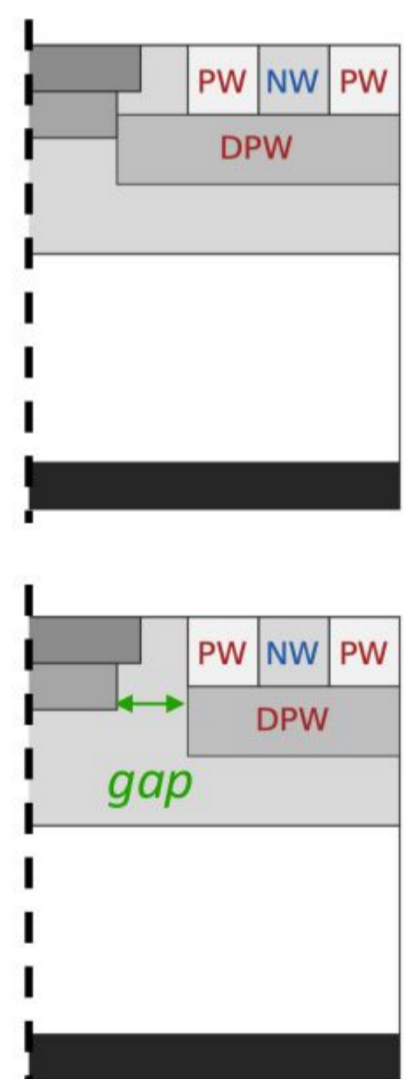
Structures developed by the **ARCADIA (Advanced Readout CMOS Architectures with Depleted Integrated sensor Arrays)** collaboration: **LFoundry 110 CIS technology**



Arcadia pad sensor

Arcadia pad sensor with gain

▶ Additional p-gain implant below the n+ collecting electrode to improve the time performance
▶ Different sensor layouts to test the charge collection properties at borders: **A1** and **A2**

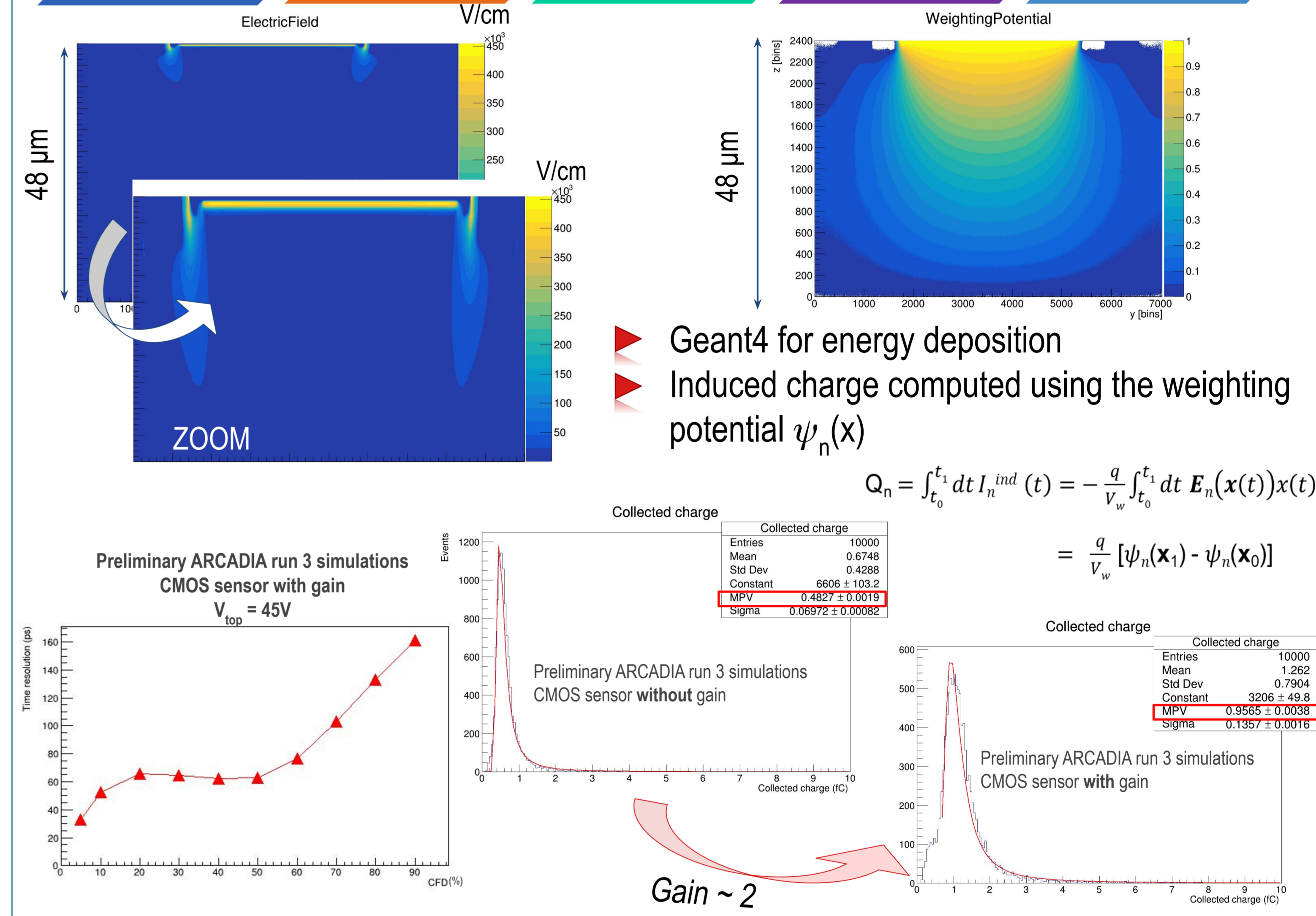
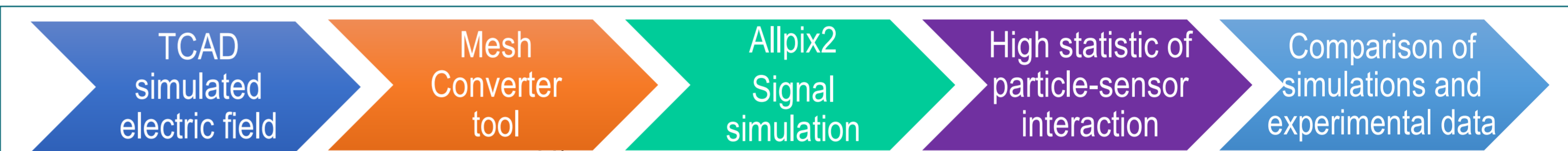


Layout A1

Layout A2

- no space between deep-p-well and p-gain
- charges from the borders are multiplied: extended collection volume more uniform multiplication
- "standard LGAD" termination implants
- charges collected at borders are NOT multiplied: direct path to the p-gain/n+ region more uniform time response

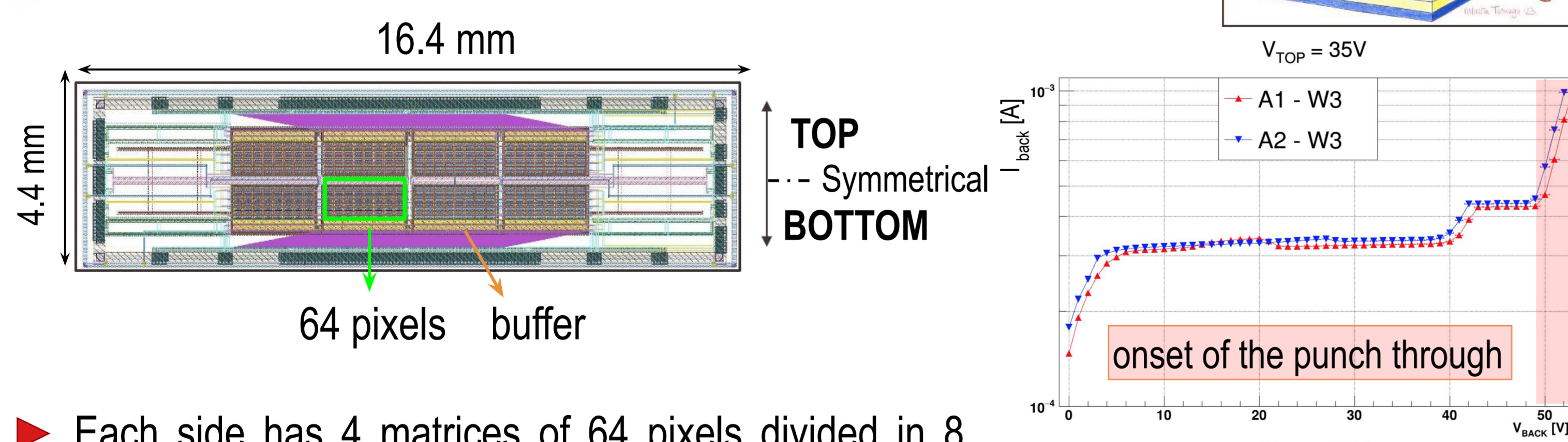
TCAD and Monte Carlo simulations



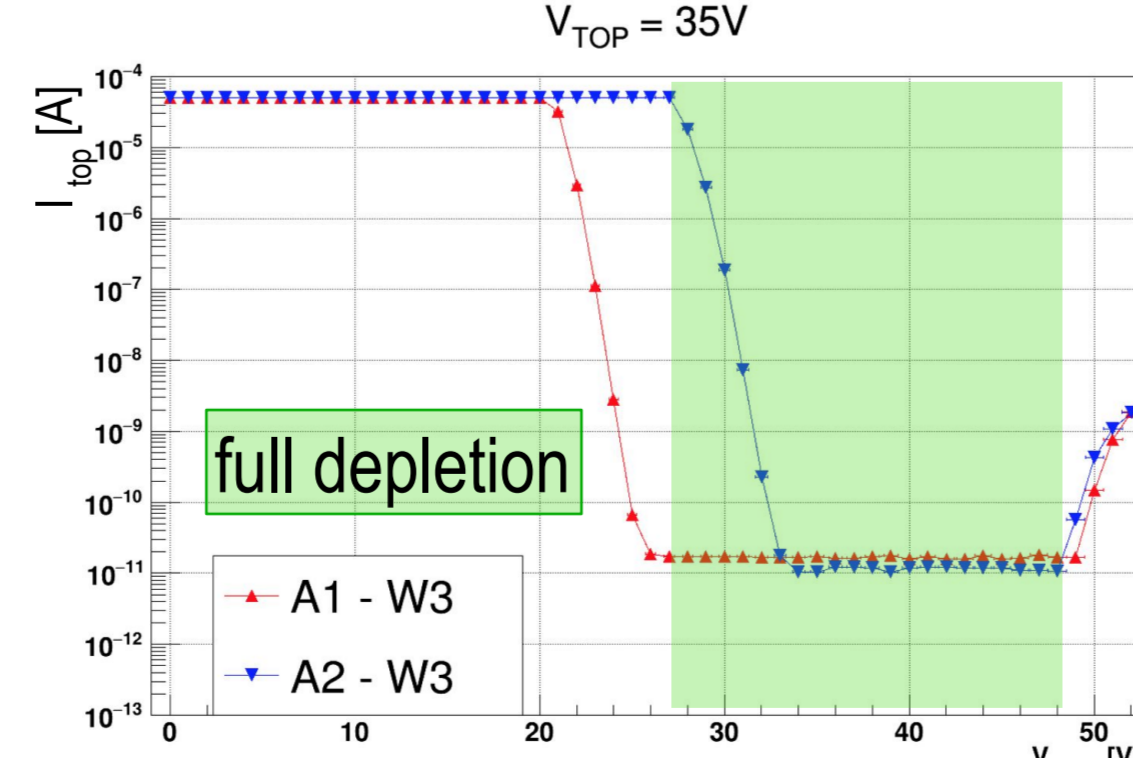
MadPix : a Monolithic CMOS Avalanche Detector PIXelated

First prototype with integrated electronics and gain layer

- ▶ Active thickness: 48 μm
- ▶ V_{back} allows full depletion (-25 V \div -40 V) \rightarrow drift field in the substrate
- ▶ V_{top} (30 V \div 50 V) \rightarrow defines the gain



- ▶ Each side has 4 matrices of 64 pixels divided in 8 rows and 8 columns
- ▶ Pixels size: 100 μm x 250 μm
- ▶ Maximum applicable backside voltage limited by punch-through current (power consumption increases exponentially above a certain threshold)

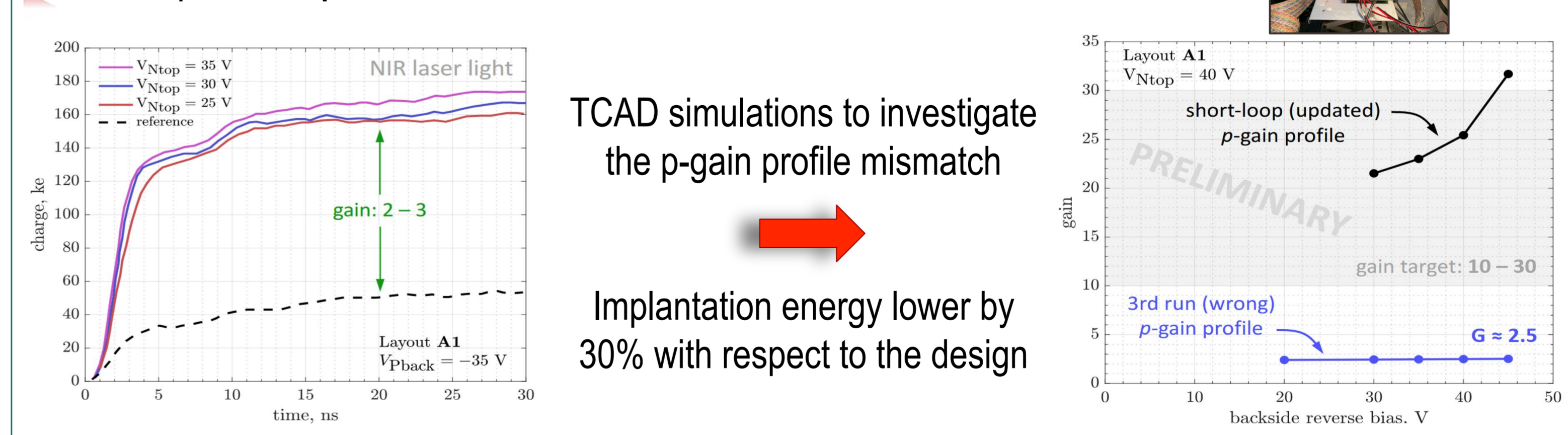


Future plans: test beam and laboratory measurements

- ▶ Validation of **MadPix + LIROC** (front-end ASIC designed to discriminate SiPM signals) + **picoTDC** (resolution of 3 – 12 ps) \rightarrow acquisition of 4 analog outputs
- ▶ Validation of **MadPix + picoTDC** to acquire 4 discriminated outputs
- ▶ Electrical and optical characterization of the **monolithic devices with higher gain** and test beam to evaluate the timing resolution (foreseen in July 2024)

Laboratory measurements

- ▶ Optical characterization of passive structures at University of Trento
- ▶ IR laser from the back of the sensor simulating the passage of a MIP
- ▶ laser spot \sim 20 μm



In-beam measurements

Proton Synchrotron - CERN, October 2023
p/ π beam with momentum 10 GeV/c
setup in collaboration with INFN Bologna
MadPix read out via 3 oscilloscope channels

