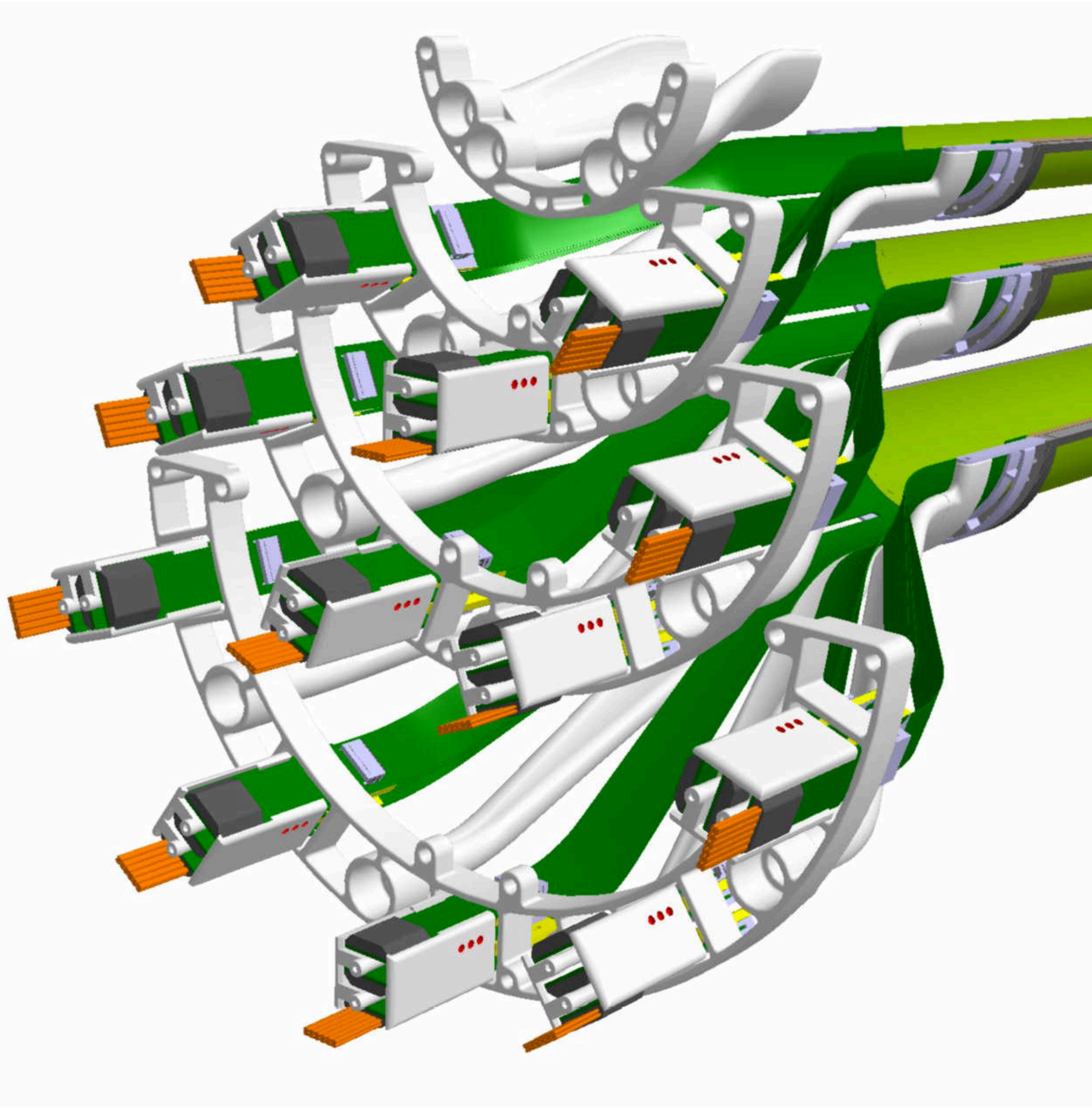
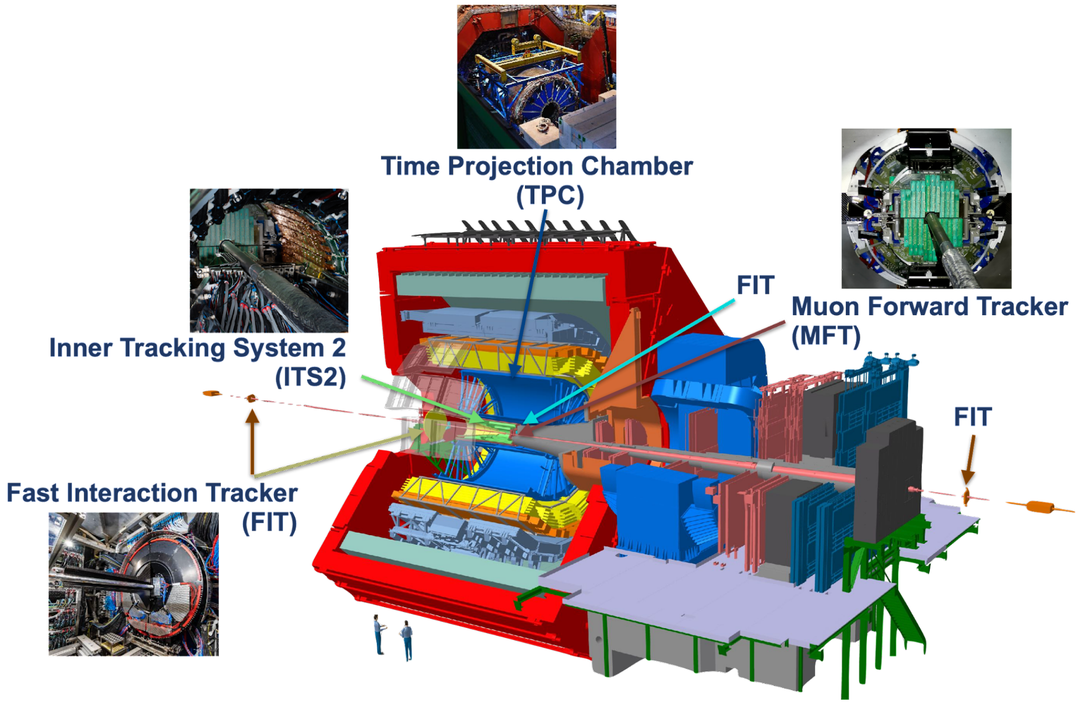
The ALICE ITS3 upgrade project

Latest results on monolithic pixel sensors test structures realized in the 65 nm technology

U. Savino on behalf of ALICE



ALICE Inner Tracking System (ITS)



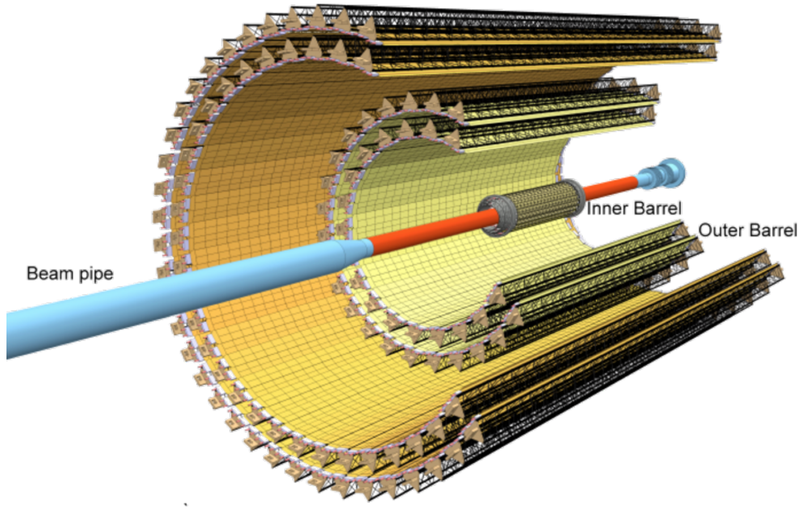
- properties of the **quark-gluon plasma** produced in **heavy-ion collisions**
- low momentum (≲1 GeV/c) particle reconstruction

ITS2 **first large-area** (~10 m^2) **silicon tracker** → MAPS

ALPIDE chip: TowerJazz **180 nm CMOS** imaging process

Main characteristics:

- **7 layers** of MAPS (3 inner - 4 outer barrel)
- close to interaction point (**23 mm**)
- improved single point **resolution** (pixel ~ 29×27 μm^2)
- low material budget: **0.35% X_0/X**
- **fast readout**:
  - Pb-Pb collisions at 50 kHz (ITS1: 1 kHz)
  - p-p at 400 kHz

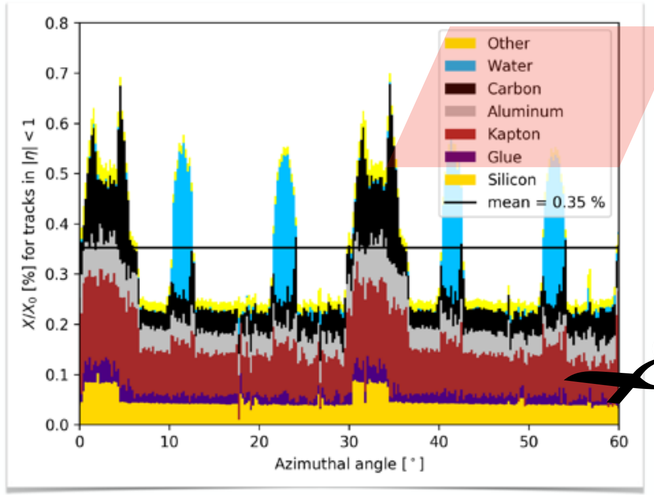


ITS3 - truly cylindrical wafer-scale MAPS

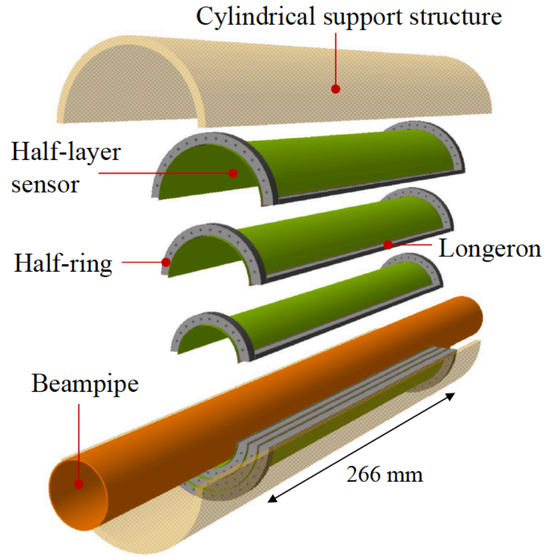
Layout:
3 layers → replace ITS2 Inner Barrel
- beam pipe inner radius (to 16 mm with 500 µm thickness)

Technology:
- **65 nm CMOS** from TPSCo:
  - 300 mm **wafer-scale chips**, fabricated using **stitching**
- thinned down to **50 µm**
  - flexible (bent to target radii)
- mechanically held by carbon foam ribs with low density and high thermal conductivity

Benefits:
- extremely low material budget: **0.07% X_0**
- homogeneous material distribution



to 0.07% X_0/X



Road map

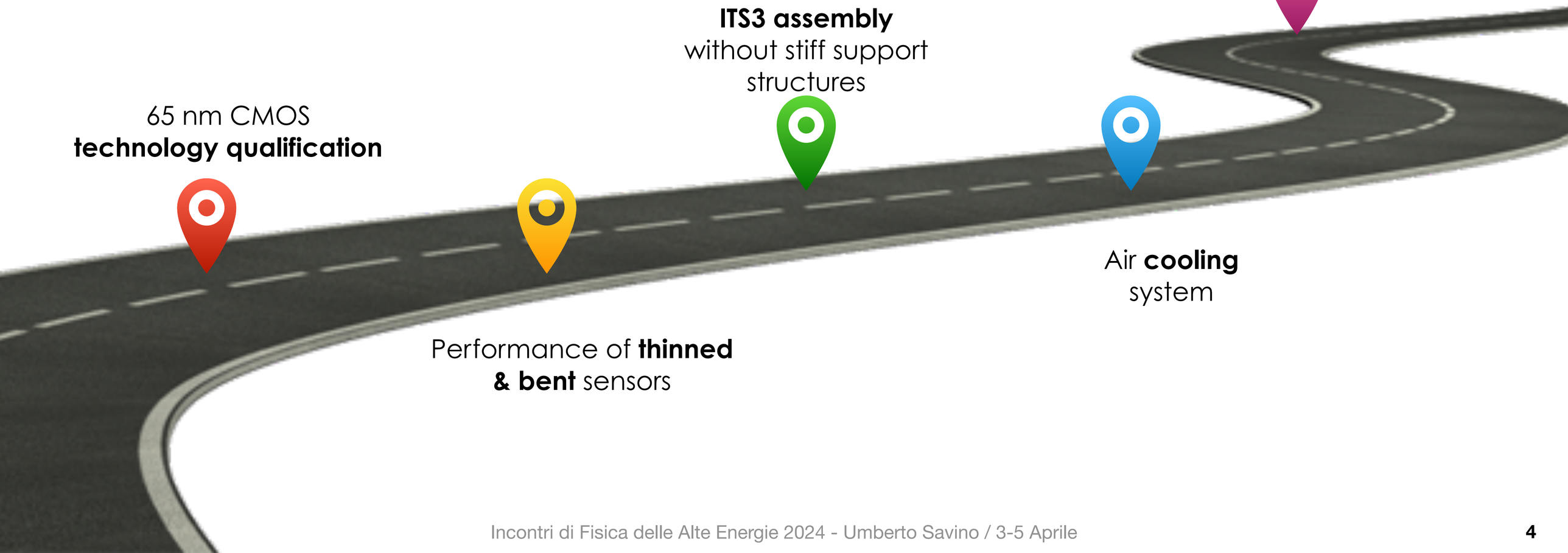
65 nm CMOS
technology qualification

Performance of **thinned & bent** sensors

ITS3 assembly
without stiff support structures

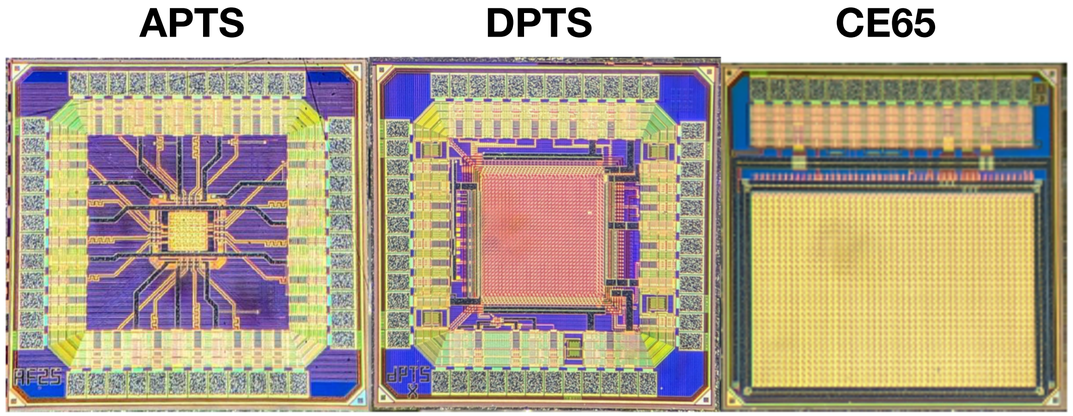
Air **cooling** system

Stitched wafer scale sensor
performance (yield and specifications)



65 nm CMOS technology validation

MLR1 submission - APTS, DPTS, CE65

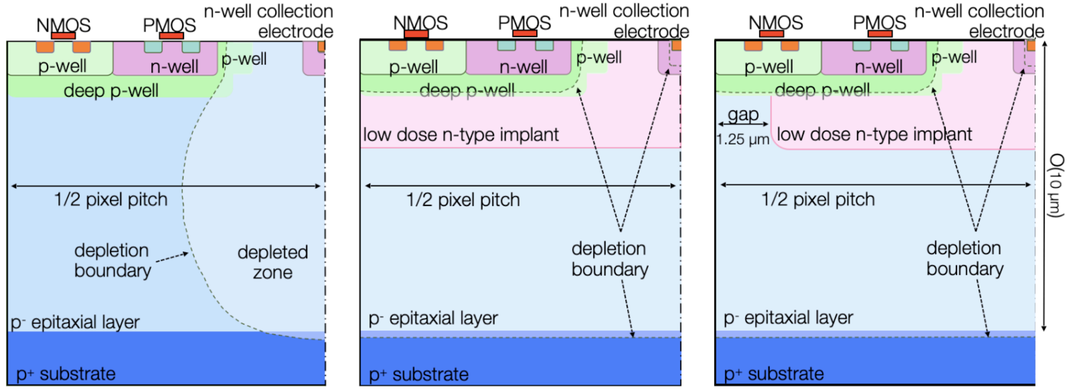


Four test structures

- Analog (APTS - 4x4 px) direct analog readout
  - OpAmp buffer for enhanced time resolution
  - SF buffer for stable readout
- Digital (DPTS - 32x32 px) digital asynchronous readout
- Circuit Exploratoire (CE65 - 64x32 px) rolling shutter analog readout

Three sensor variants

- standard: ALPIDE-like
- modified: low dose n-type implant
- modified with gap: low dose n-implant with lateral gap



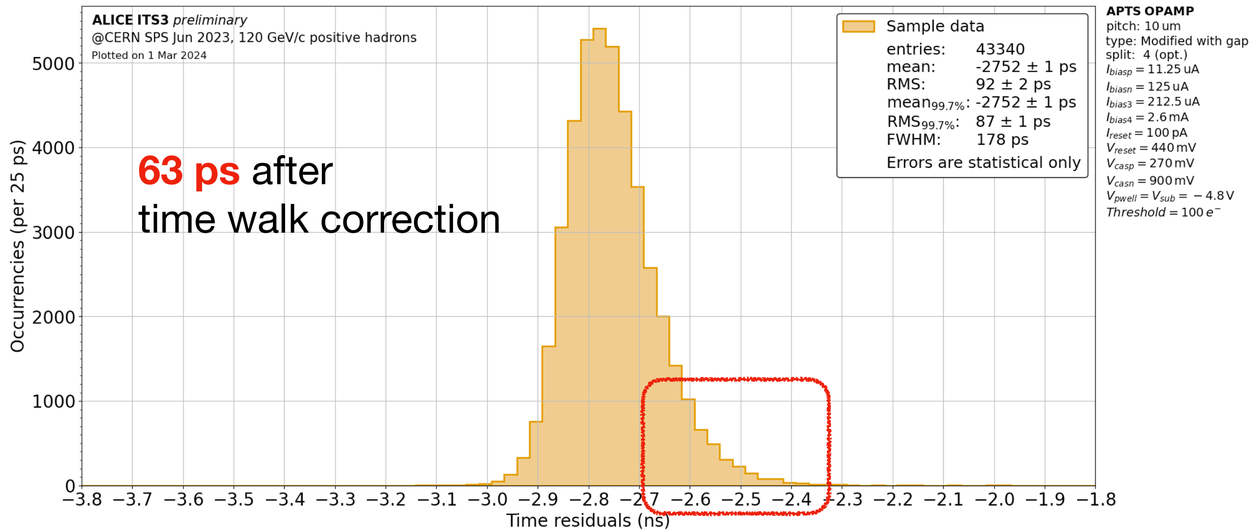
MAIN results of MLR1 test structures in poster session:
MLR1: 65 nm CMOS MAPS technology validation for ALICE ITS3 - (Alessandro Sturniolo)

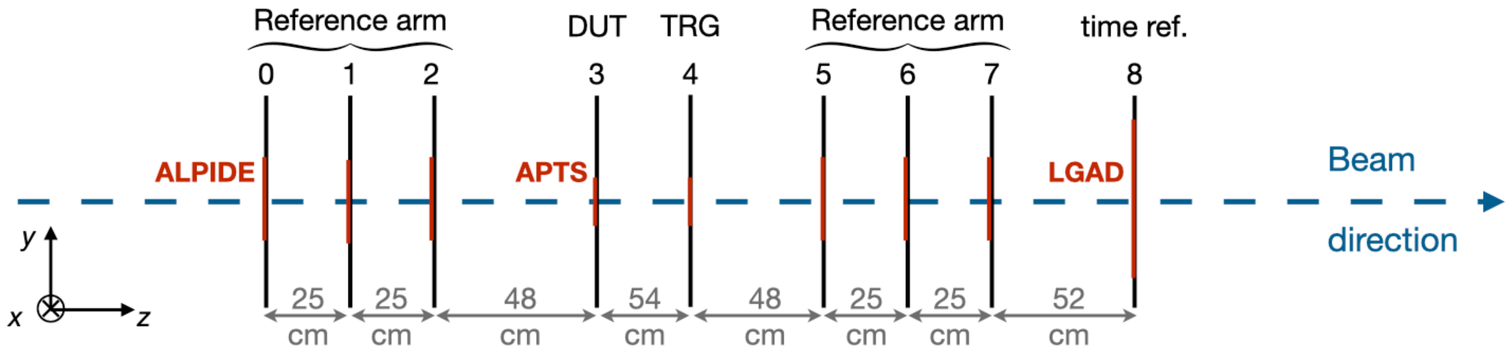
APTS OA - time resolution

Test beam

- SPS (CERN) positive hadrons 120 GeV/c
- time reference → FBK fast LGAD (30 ps)
- APTS-SF trigger (15 µm pitch)
- APTS-OA modified with gap (10 µm pitch) with inner pixels read out with a scope (40GS/s x 4 & 13 GHz)

Result: 63 ps time resolution and **above 99%** efficiency at V_sub = -4.8 V





Performance of thinned and bent sensors

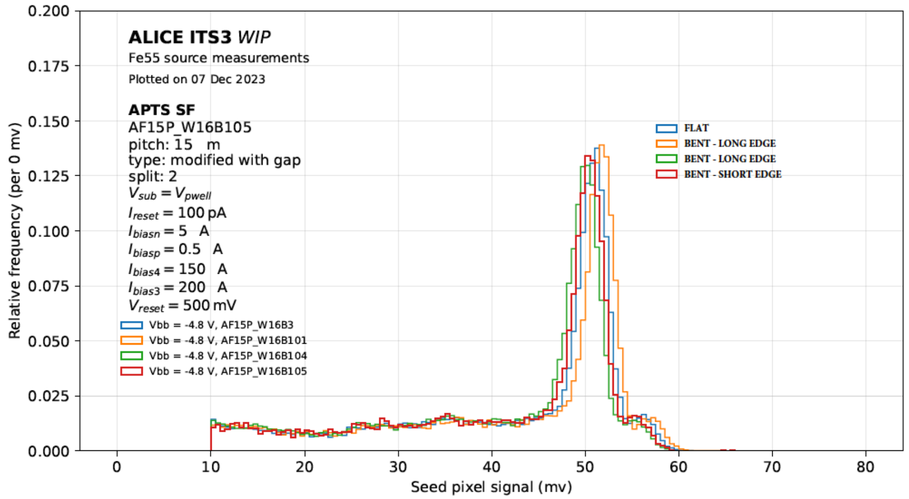
Test on ALPIDE sensors

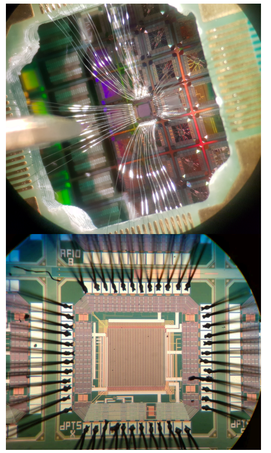
Procedure

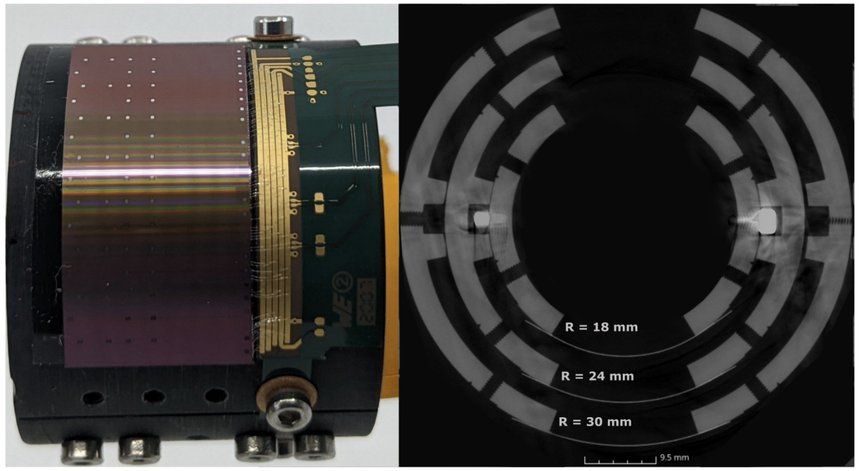
- number of no responsive pixels
- pixel threshold
- noise
- fake hit rate

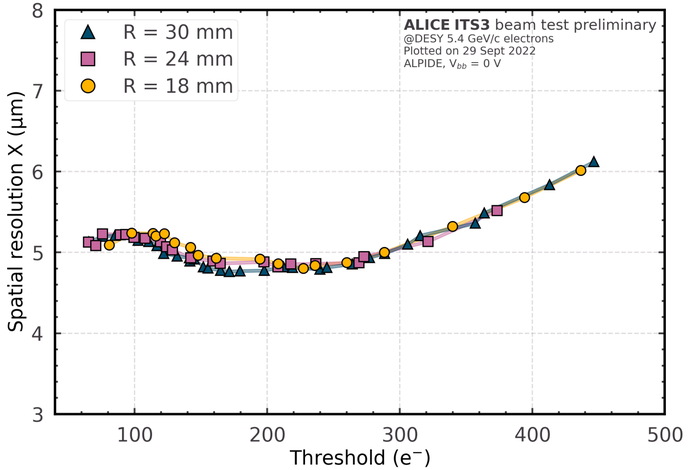
performance unchanged after bending

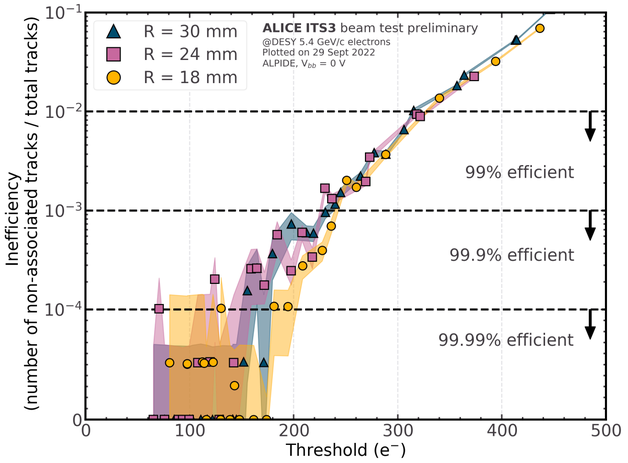
results from bent MLR1 structures → WIP







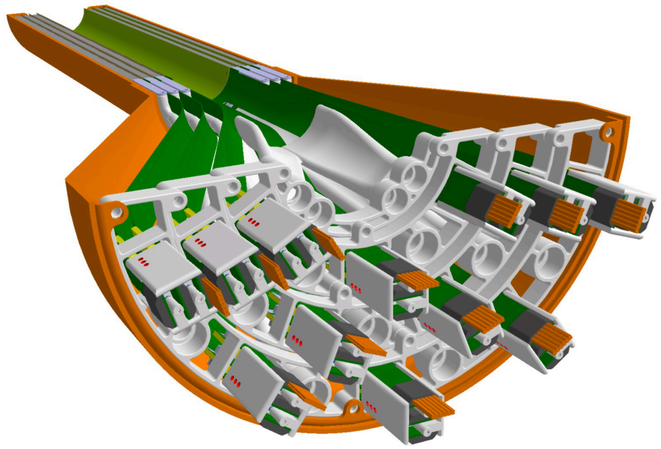


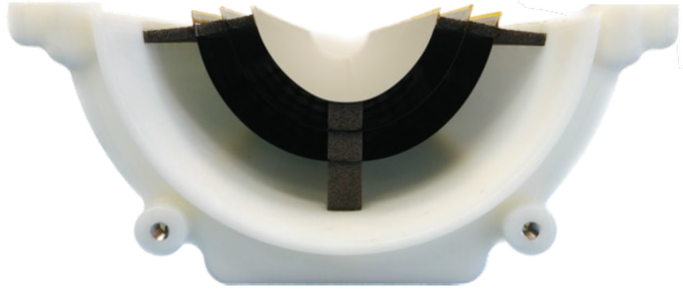


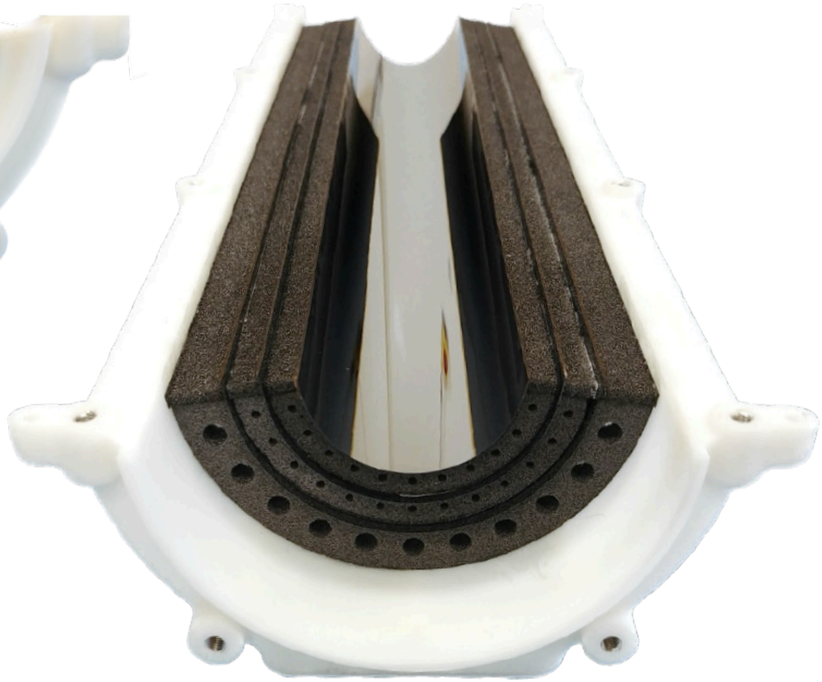
ITS3 assembly

Without using stiff support

- Engineer model 1 has proven integration scheme & cooling scheme







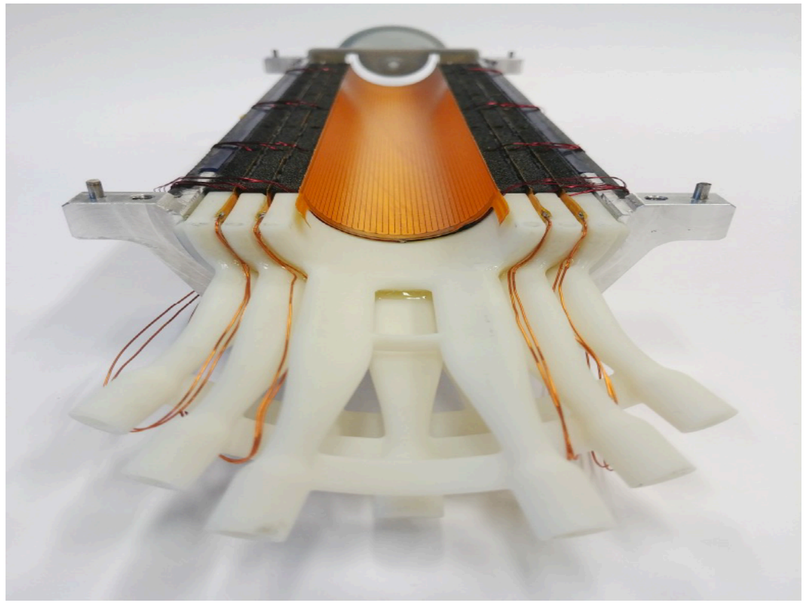
Half detector

- wafer-scale bent MAPS
- carbon foam spacers

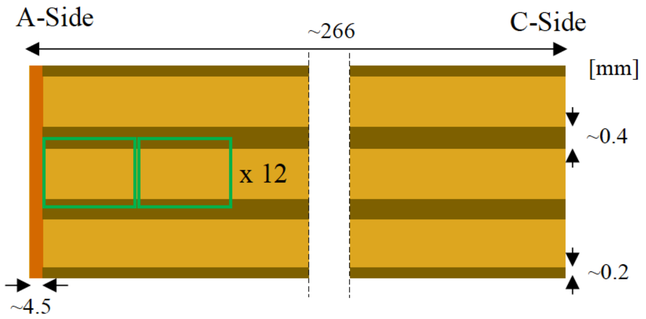
Rigid support with good **thermal properties**

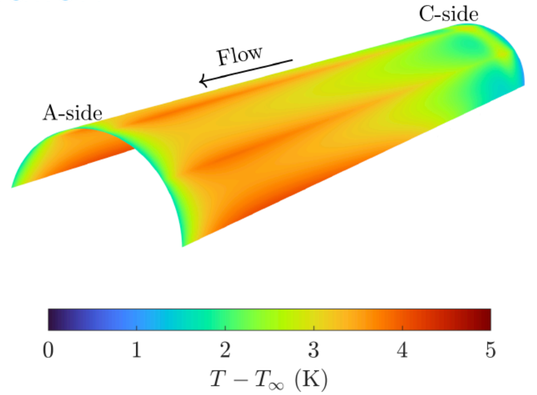
Air cooling

- **Cooling characteristics**:
  - employ **air**
  - speed: 8 m/s
  - power dissipation 40 mW/cm^2
  - temperature gradient < 5 K
  - 1 μm vibration

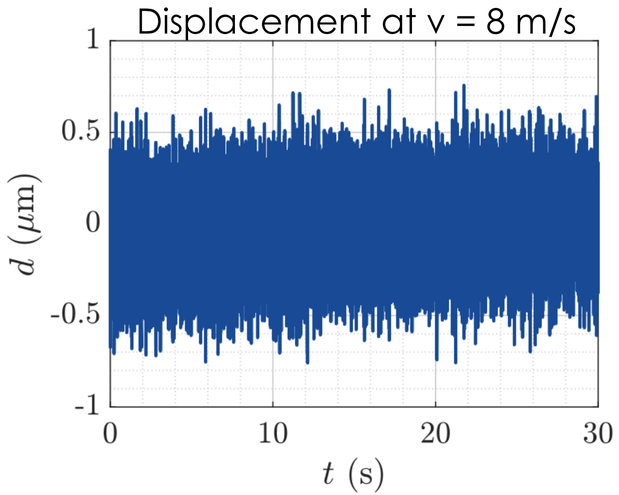


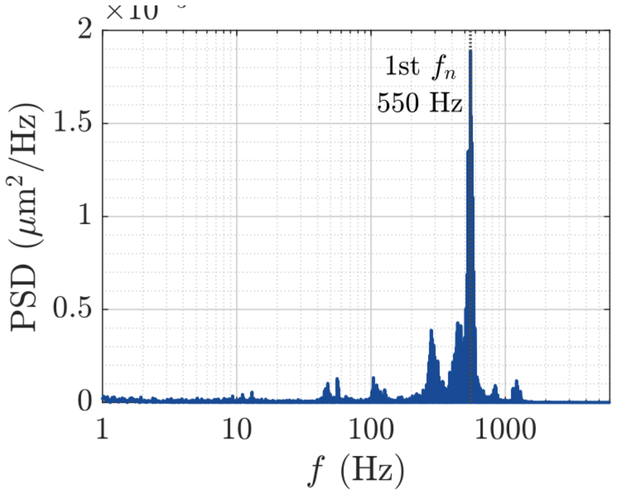
Temperature variation from simulation





Aeroelastic test





Stitched wafer scale sensors

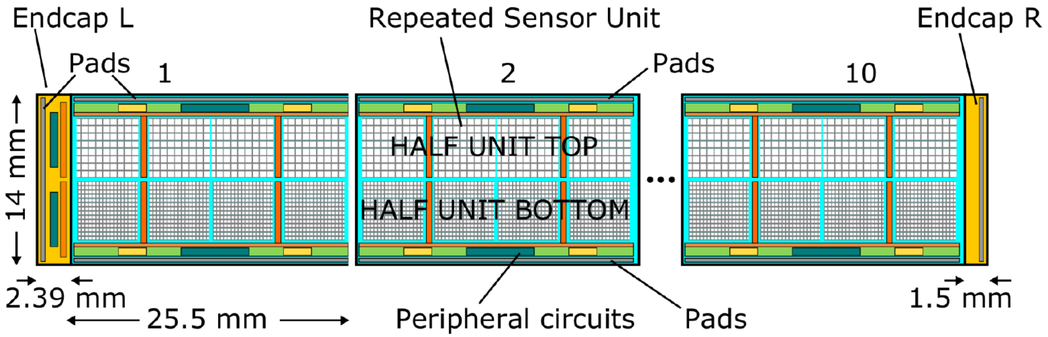
MOnolithic Stitched Sensor (MOSS) & MOnolithic Stitched sensor with Timing (MOST)

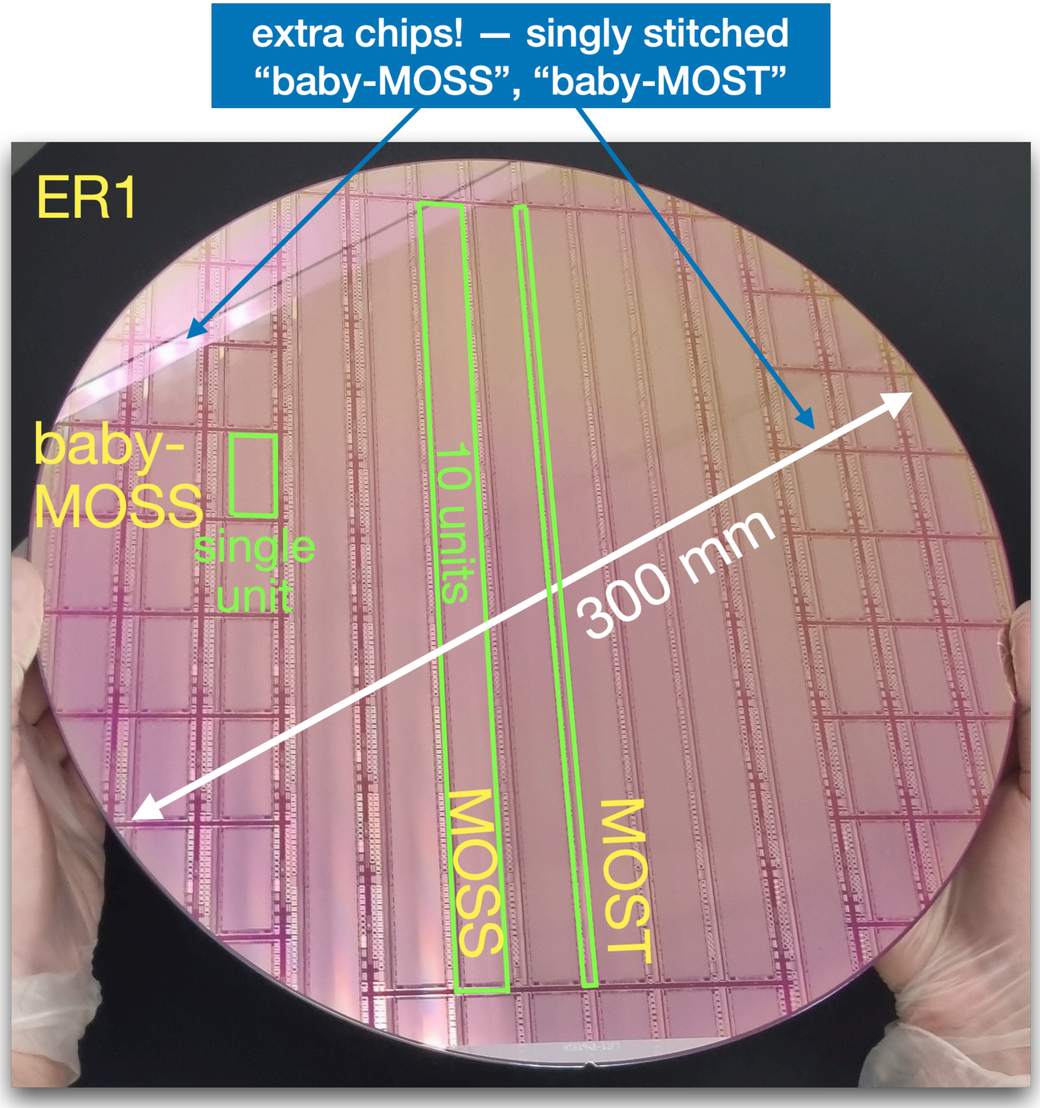
MOSS:

- **largest stitched chip** ER1 (25.9 cm x 1.4 cm)
- 6.72 million pixels
- **10 Repeated Sensor Units** (RSU) & two **end-caps regions** (powering and readout)
- 2 **independent** Half Units (HU) per RSU
  - Top HU: 4 matrices of 256 x 256 22.5 μm pixels
  - Bottom HU: 4 matrices of 320 x 320 18 μm pixels

MOST:

- 25.9 cm x 2.5 mm dimension
- 10 tightly packed matrices
- 64 x 352 18 μm pitch sub-matrices/matrix
- shared wafer-scale digital asynchronous readout per matrix





MOSS performance

SETUP
- ~2000 wire bonds on proximity board
- 5 FPGA based readout cards

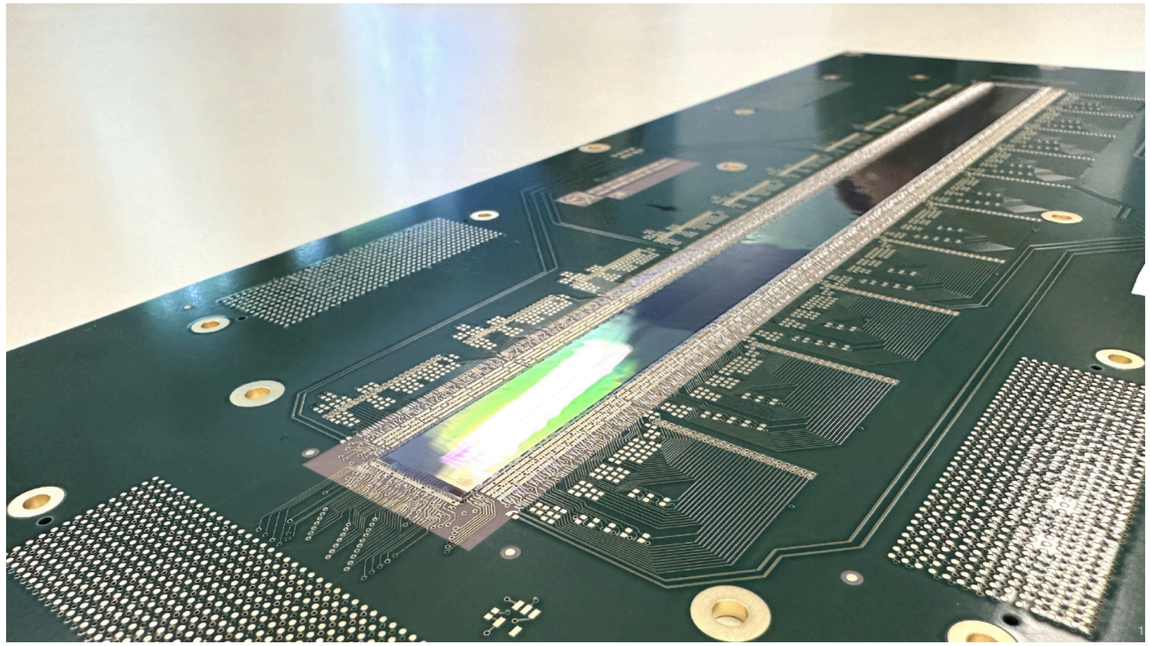
Procedure WIP
- looking for hotspots
- wafer probing
- IV curves at CMOS nodes

Wafer 24

	RSU1	RSU2	RSU3	RSU4	RSU5	RSU6	RSU7	RSU8	RSU9	RSU10
1-TOP	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I	OK - II	OK - I	OK - I	OK - I
1-BOT	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I
2-TOP	OK - II	OK - I	OK - I	OK - II	OK - I	OK - I	OK - II	OK - I	OK - II	OK - I
2-BOT	LIMIT	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I	OK - II	OK - I
3-TOP	to be tested									
3-BOT										
4-TOP	OK - I	LIMIT	OK - I	OK - I	OK - I	OK - I	OK - II	OK - I	OK - I	OK - I
4-BOT	OK - I	OK - I	OK - I	OK - II	OK - I	OK - I	OK - I	OK - I	LIMIT	OK - I
5-TOP	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I	OK - II	OK - I
5-BOT	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I
6-TOP	OK - II	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I
6-BOT	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I	OK - I

MOSS chip from first production

97% (97/100 chips) "OK"



Yield
- ≤ 2% missing pixels due to production yield
- 2/3 wafers comply
- 1440 regions (tiles)/sensor --> can be remotely switched off in case of production failure

Full ITS3 sensor production
- 18 wafers from ER1 yield extrapolation
- plan to produce 50 wafers

Next steps

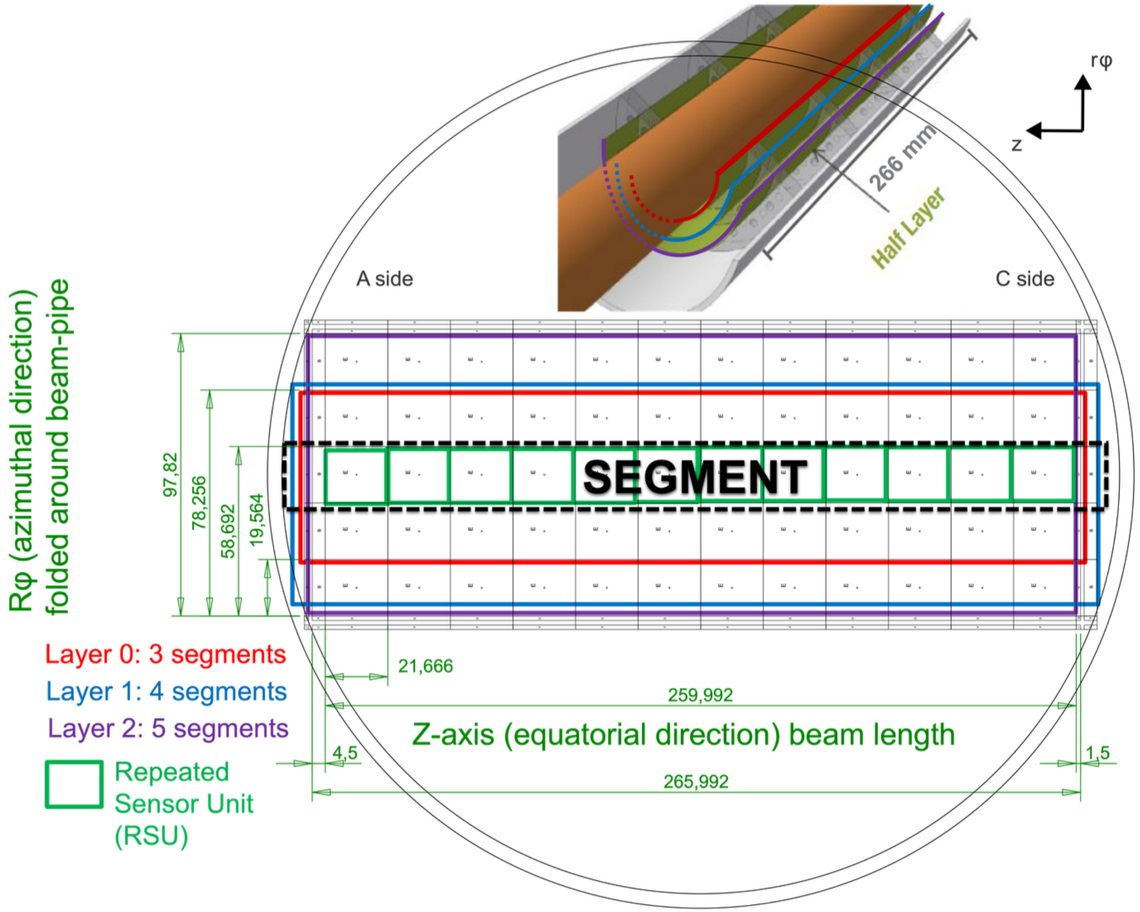
ITS3 construction and implementation phase

MOSS test beam

- First results confirm extrapolated (MLR1) performance in terms of detection efficiency and spatial resolution

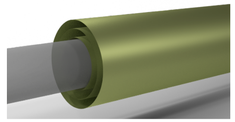
Looking at the future

- ER2 - producing full-size and full-functionality prototype
- ER3 - final detector-grade production version
- optimization of detector integration and assembly sequence → 2 qualification model (QM) half barrels
- final model → 4 half-barrel (final model)



Conclusion

ITS3
truly cylindrical
wafer-scale MAPS



Kick off meeting

MLR1 65nm CMOS validation

ITS3 R&D phase

COMPLETED

MOSS ER1 wip

TDR

Technical design report of ITS3
A bent wafer-scale monolithic pixel detector

ALICE collaboration
January 29, 2024, version: V1r-xxxt

https://arxiv.org/abs/2401.04629

ER2

ER2, full scale & full functionality prototype

ER3

ER3, full scale & full functionality production sensor

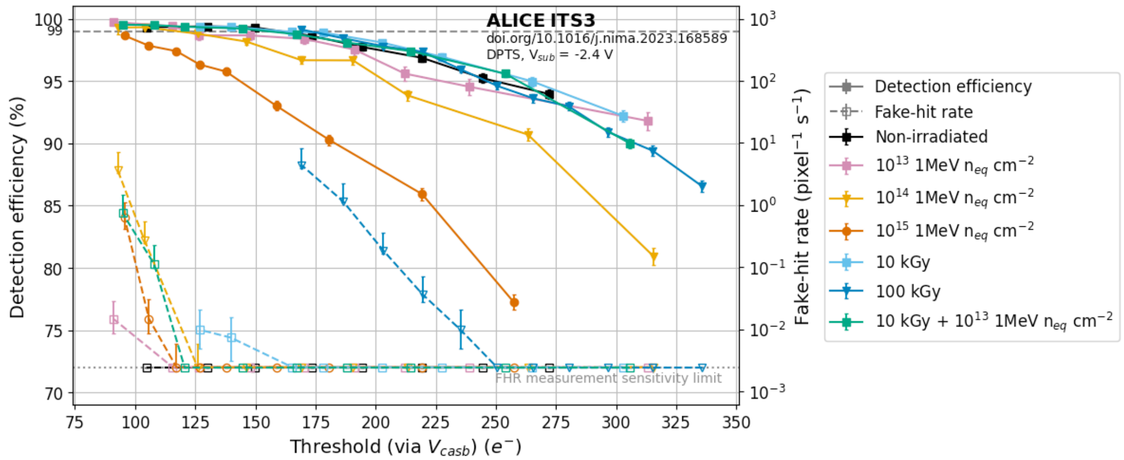
2019

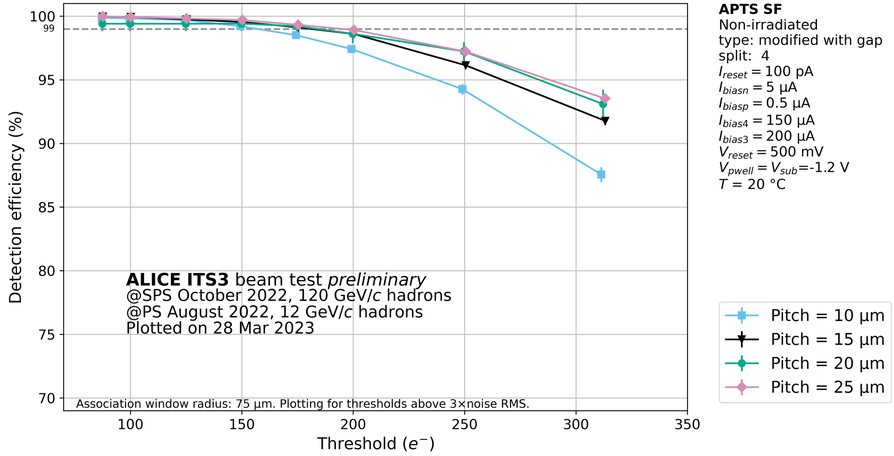
2027

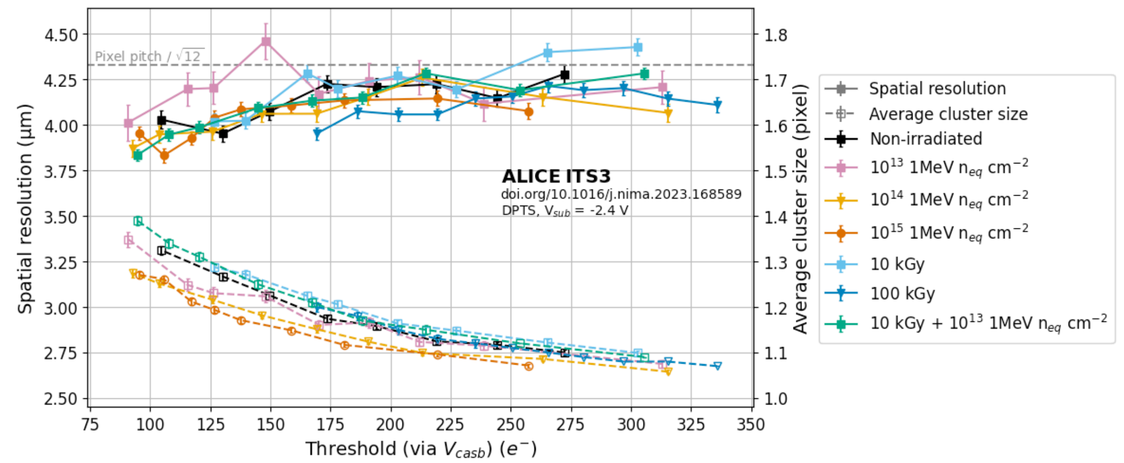
Spare slides

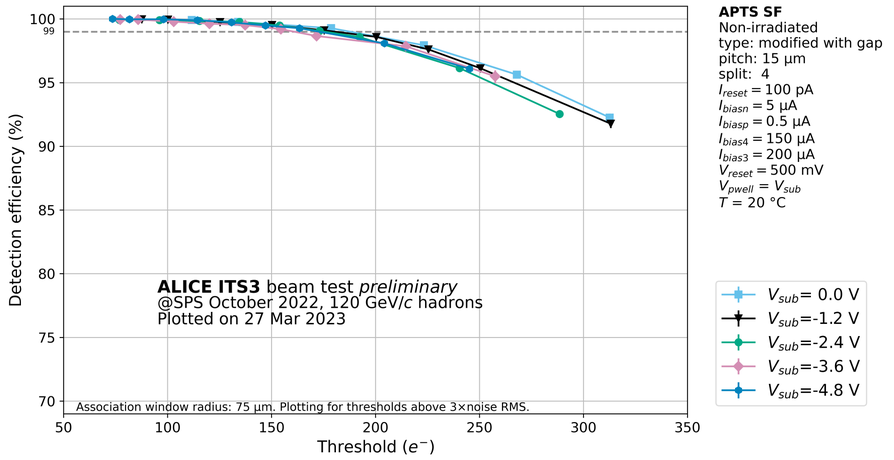
MLR1 characterization

Validation of the 65nm CMOS TPSCo process









ALPIDE bending

Bent along column