

# A discussion on timing, a case for a unified SAND readout and more...

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# Part 1: Timing

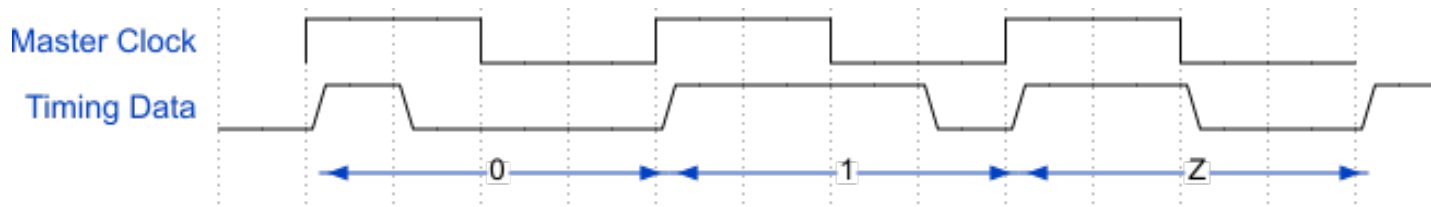
In which we tell the white rabbit that it's too late...





# Dune Timing System signal

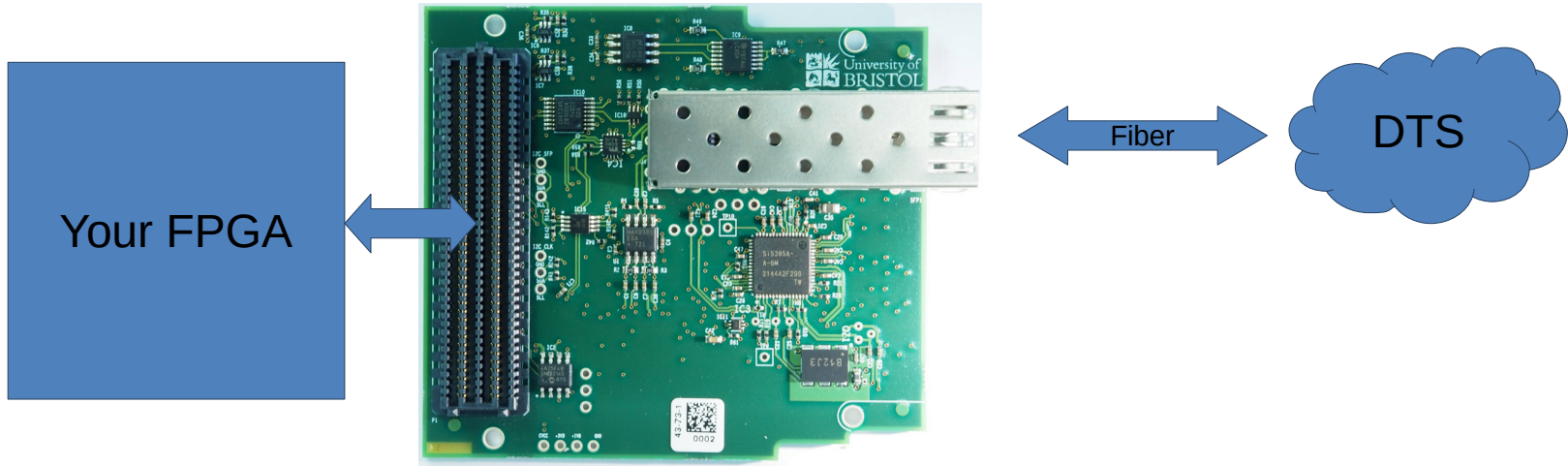
- Single mode fibre carrying clock and synchronization messages
  - 62.5 MHz clock (recovered from data stream)



- Data carries periodic timestamps and synchronous commands
- Syncs by timestamping an event and broadcasting a message
- Clock edges at timing endpoint aligned to each other to  $O(100\text{ps})$ , long term, over 1500 endpoints
  - Down to  $<10\text{ ps}$  within a spill and a small group of endpoints

# What is an “endpoint”?

- Reference endpoint hardware: an optical transceiver and a PLL



- DTS also provides reference firmware and a software library
- Built in delay compensation and control/monitoring functions

# Our requirements

- We asked for O(10)-O(100) ps rms depending on subdetector
  - Both **between** and **within** subdetectors
  - Our strongest requirement applies only within a spill
  - DTS only “promised” O(100) ps
  - But they meant long term (i.e. drift), short term is better

- **The requirement can be met**
  - Within a spill, and a group of endpoints

PLL BW	Skew stdev.
100Hz	31 ps
400Hz	6.9 ps
1kHz	2.8 ps
4kHz	1.8 ps

From  
<https://indico.fnal.gov/event/61796/>

# Open Questions

- More detailed measurements of variance per endpoint group
  - So far only hard numbers for groups of 8 (same fiber)
  - Perhaps useful to test more SFPs?
- **Beam timing measurement from accelerator seems lacking**
  - Certainly does not reach  $O(100)$  ps
  - From our meeting of ND+Timing, indication that **dedicated instrumentation** using the Dune clock would be useful
  - Whose responsibility would that be?

## Part 2: A common DAQ board?

In which we get to play with LEGO



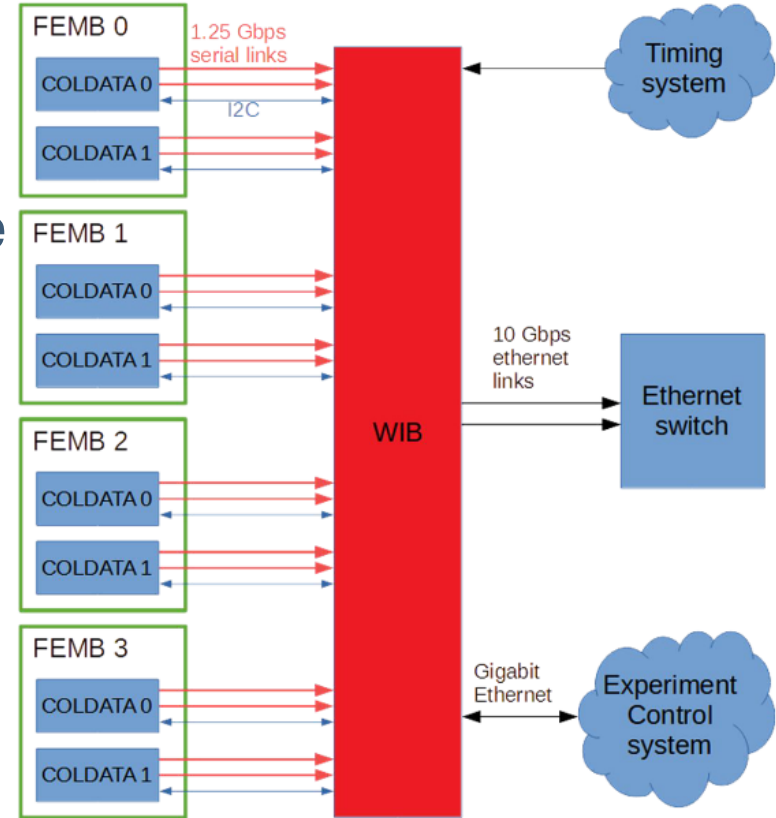


# Some info from FD development

- DAQ will use 10G Ethernet links
  - Uses commercial transceivers, switches, PCIe cards.
  - DAQ group will provide a firmware block.
- The DUNE Timing System will distribute a 62.5 MHz clock + sync data to the FD, and are willing to do the same for the ND
  - They also provide a firmware block and library.
- Slow control still somewhat more open

# FD example: the Warm Interface Board

- The warm part of FD readout
- Interfaces with cold boards on one side, DAQ + timing on the other
- Based on a Xilinx Zynq: FPGA + CPU (with embedded linux)
- Quite close to our idea for GRAIN

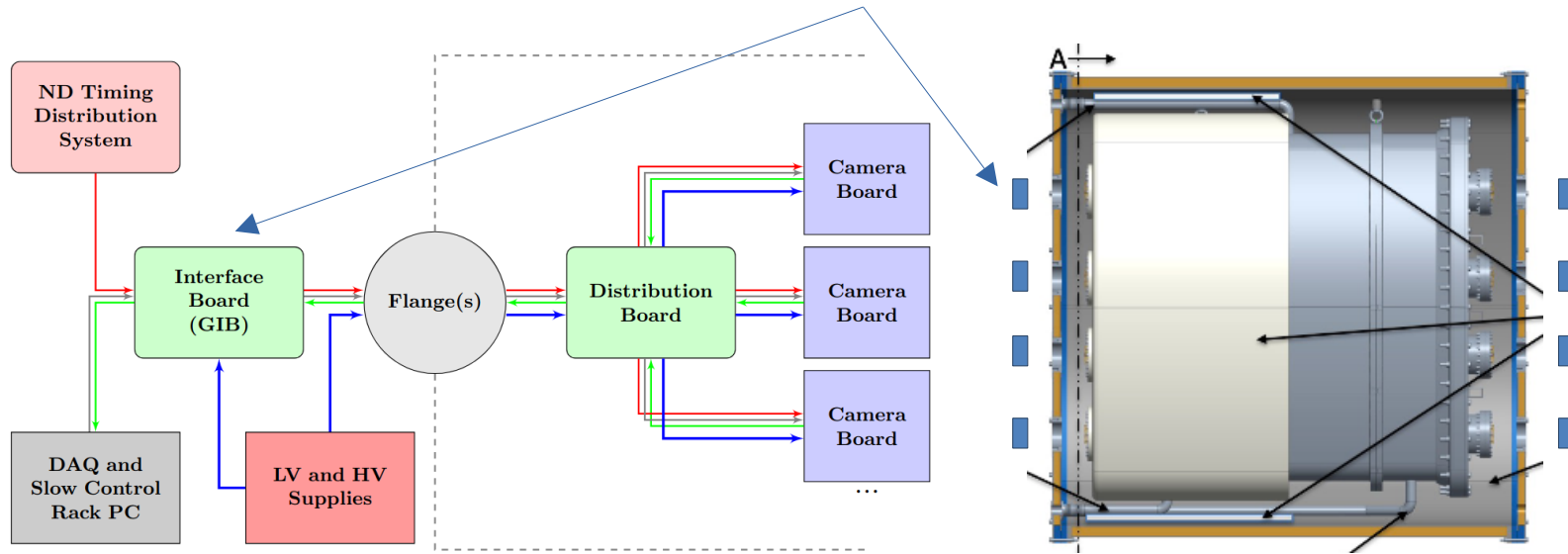


# A suitable architecture for SAND too

- We have already agreed to go with dunedaq software-wise
  - This means integrating the DAQ group firmware in our boards
- We like the DUNE timing system
  - This means integrating the DTS group firmware in our boards
- It is only reasonable to use a very similar device (i.e. a Zynq)
  - Firmware is not 100% portable so the closer the hardware the better

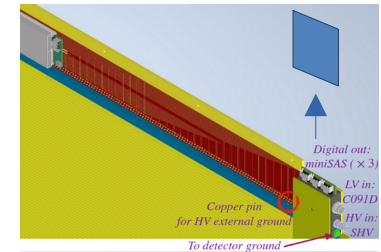
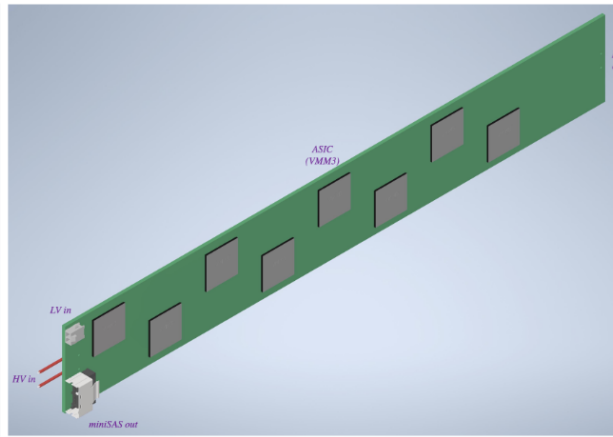
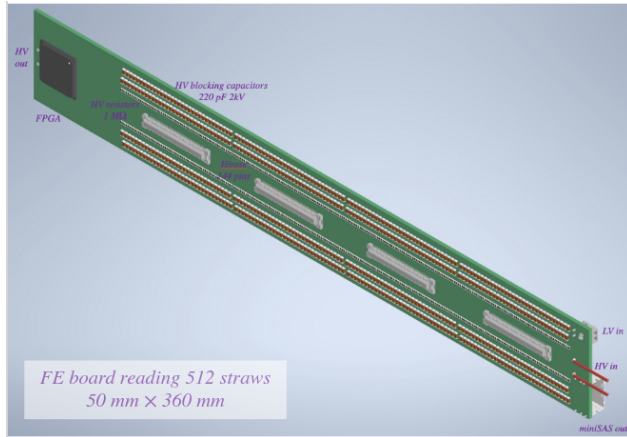
# We could all have our own board...

- GRAIN wants a few boards that sit outside the cryostat
  - Each handling up to 8 “ALCOR++” ASICs or 8192 channels
  - OK size and granularity to be a DAQ/DTS endpoint



# We could all have our own board...

- STT wants a few hundred FE boards, gas cooled, in the frames
  - With 8 VMM3/Tigers for a total of 512 channels (wires)
  - Can not be a DAQ/DTS endpoint as is (can not fit fiber SFPs, perhaps too high power, fiber routing issue, low-ish granularity)
  - Endpoint as a separate board, out of gas, one per module

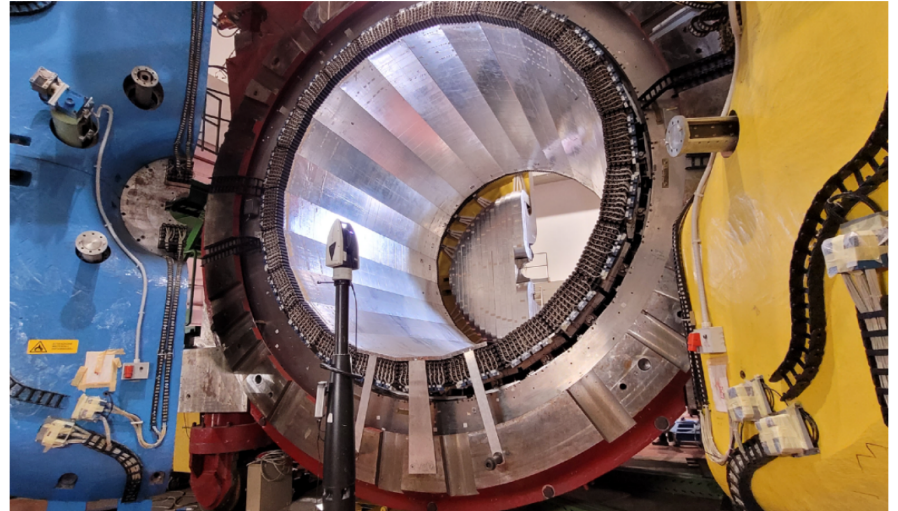


# We could all have our own board...

- Drift Chamber wants to separate ASICs and FPGA
  - Channel density is lower and we want to limit cable length
  - Single minimal ASIC board with one chip/64 ch
  - Digital I/O of multiple ASICs routed to an FPGA board
  - This board could be a DAQ/DTS endpoint.
  - A few endpoints per supermodule

# We could all have our own board...

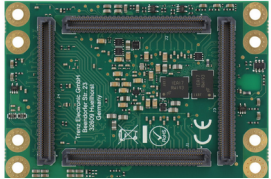
- ECAL has “only” 5000 channels
  - Lowest channel density, but largest data/channel
  - Does not have an ASIC yet, nor a specific location for the boards
  - Any board made for ECAL could be a DAQ/DTS endpoint
  - Analog signal from PMTs
  - Digitization outside magnet
  - More on this in Part 3



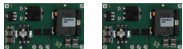
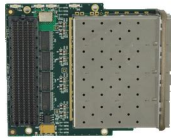
# ... but we can share many components



Photo Shows  
Similar Product



52mm x 76mm



A custom base board for each system, **BUT**

- Common FPGA:

- For example Zynq Ultrascale “System on Module”

- Includes FPGA, ARM CPU, RAM, Flash, ...

- Commercial support claimed until 2035

- **Can share large fraction of Firmware and Software**

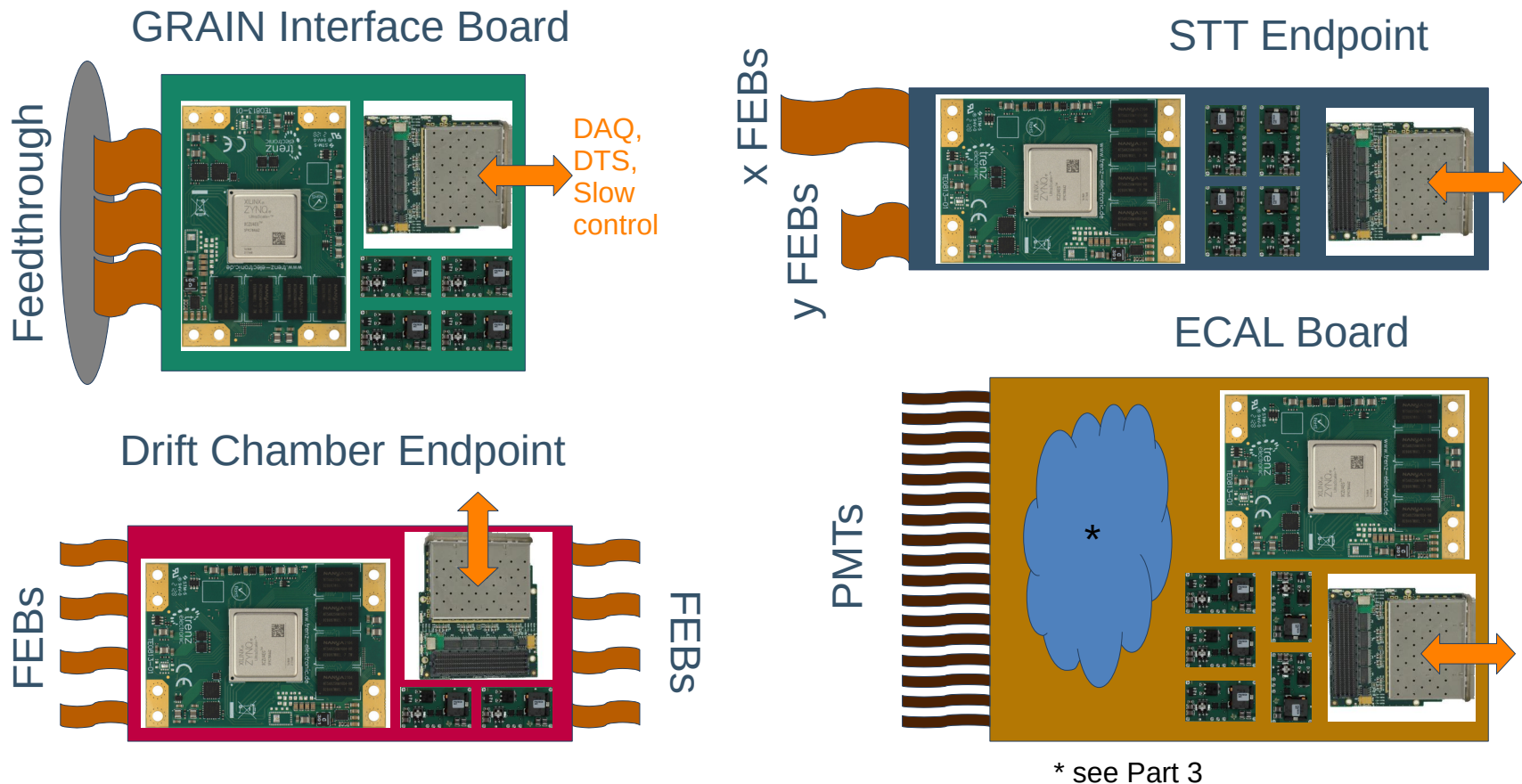
- Common DAQ/DTS part

- Common power components (B field tolerant)

- ...



# ... but we can share many components



# Semi-common on-detector DAQ design

## PROS

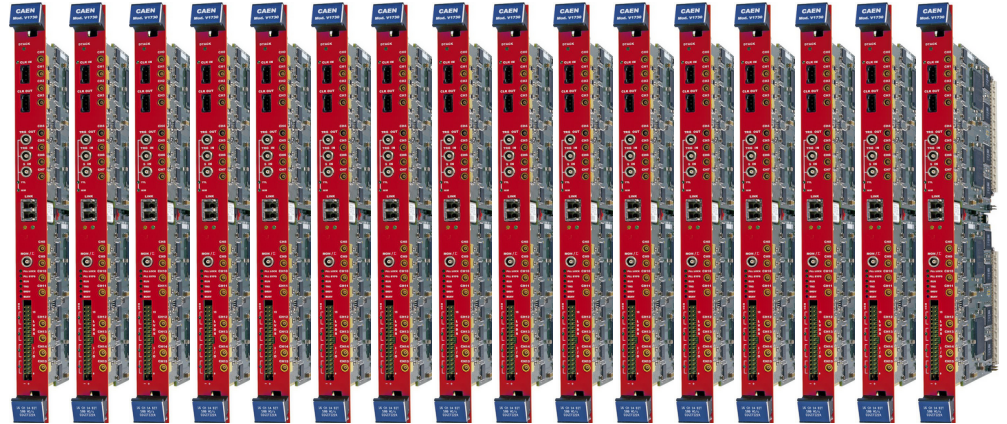
- Reduced risk and complexity of PCB design
- Only one major modular firmware + software suite to develop and maintain
- Economies of scale on hardware component purchases
- Easier repairs/spare inventory

## CONS

- Need to size the baseboards to have comparable “weight” i.e. data volume
- Need more cooperation on hardware development

# Part 3: ECAL

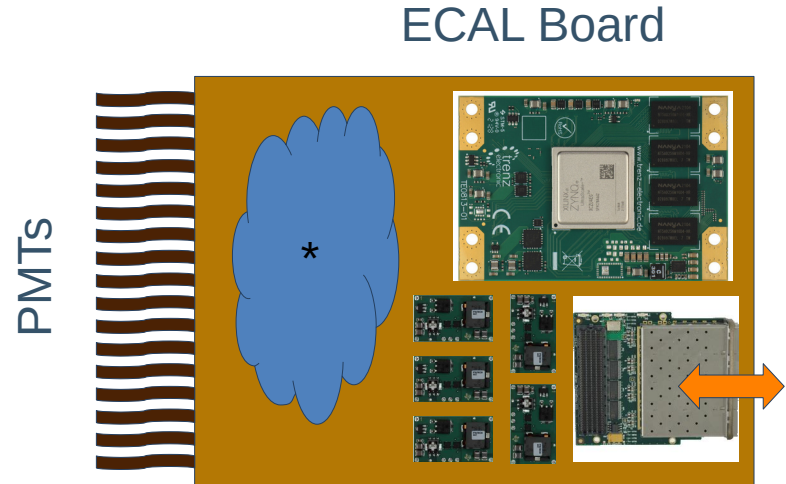
In which we try to avoid these



# ECAL Front End

Why no FERS or similar?

- It does not *really* offer the required performance because the ASICs themselves do not
- It's impossible to hook it up to the DAQ and DTS
- It still costs quite a bit



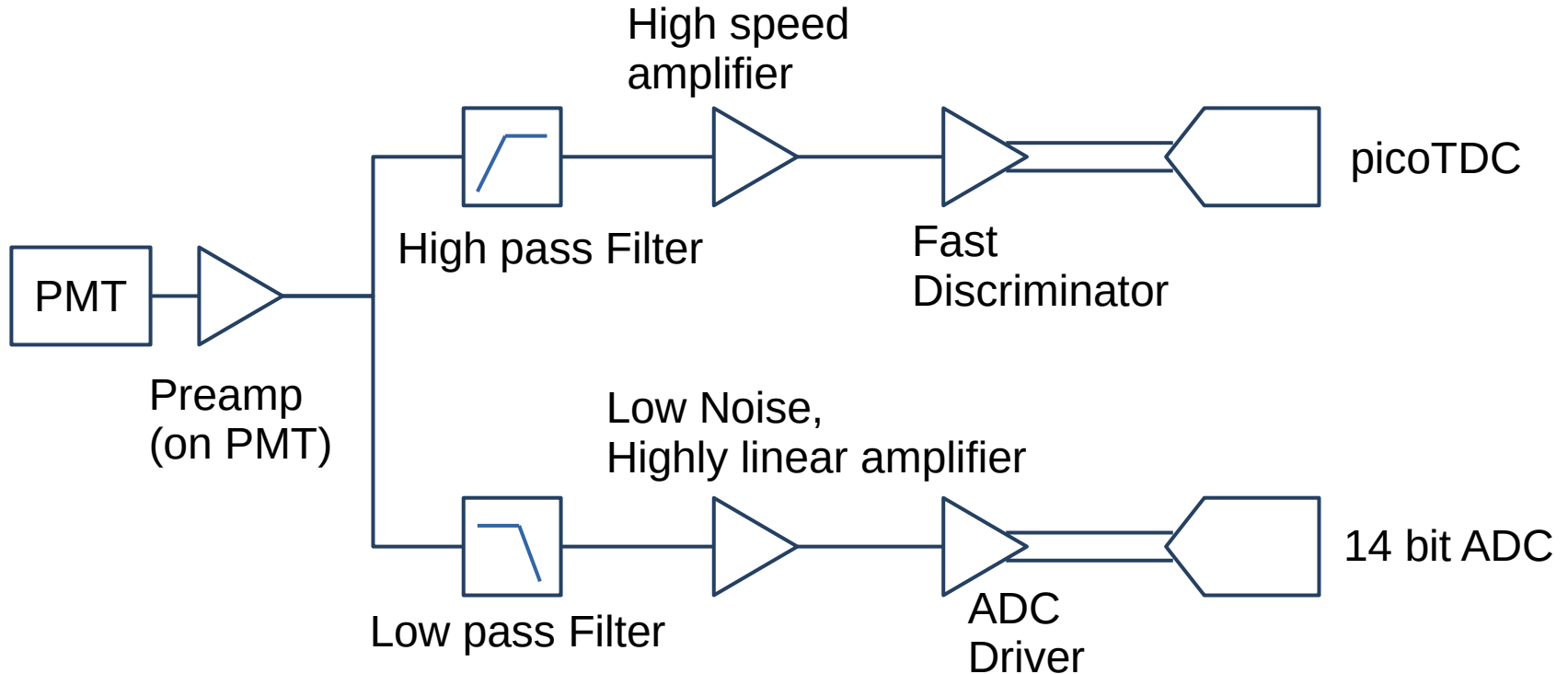
The common components approach needs a Front End

- Let's try to design one

# ECAL Front End

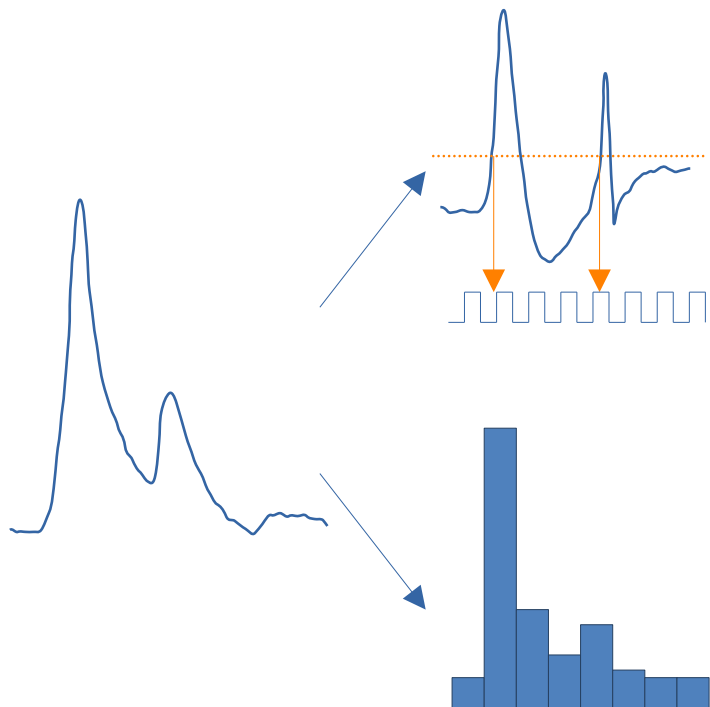
- A pure digitizer solution is very expensive (CAEN or homemade)
  - It's not just the ADCs, it takes a lot of FPGAs to read them
- No ASIC that I could find reaches the required resolutions
  - PicoTDC can reach the time, but ToT has poor amplitude resolution
  - MAROC is almost fast enough at 60 ps, but only 30 p.e. range
  - Analog memories are too short to capture the spill
- Left with *old school* separate solution, but with modern chips

# Split paths



Note: some stages may be folded into a single active component

# Expected signal response



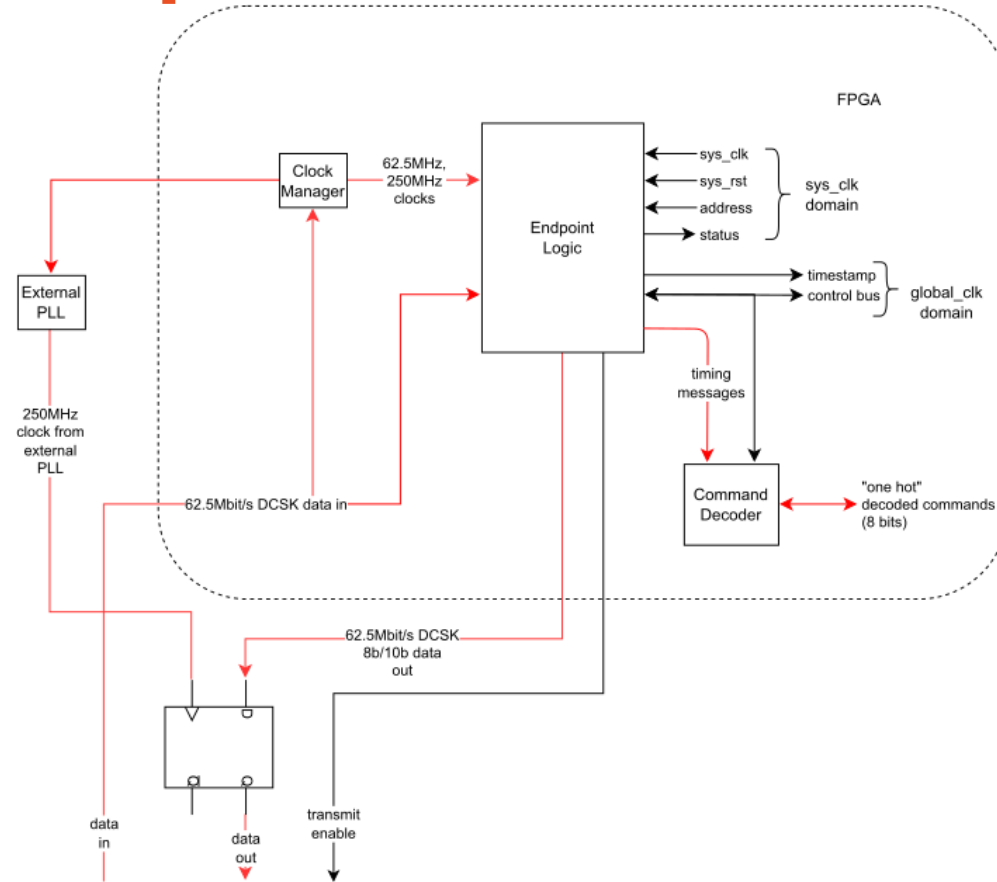
- Good time resolution
  - Down to  $O(10)$  ps after offline amplitude corrections
- Good charge resolution and range
  - 14 bit  $\rightarrow$  up to a few 1000 p.e. with appropriate gain
- Multi-hit capability
  - Can resolve hits  $<100$  ns apart after offline processing

## Part 4: Backup

In which I put extra slides because there were too many already

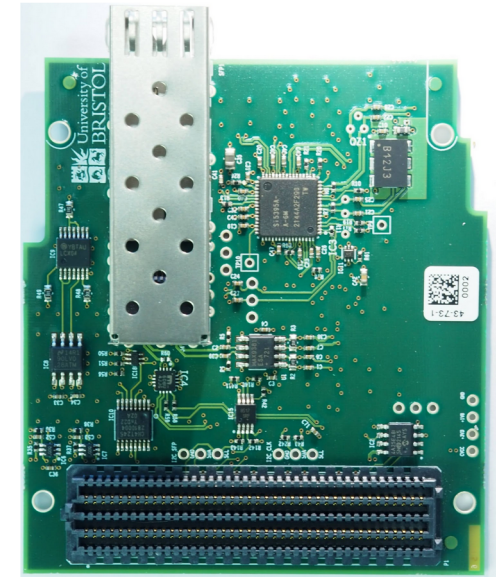


# Timing Endpoint reference diagram

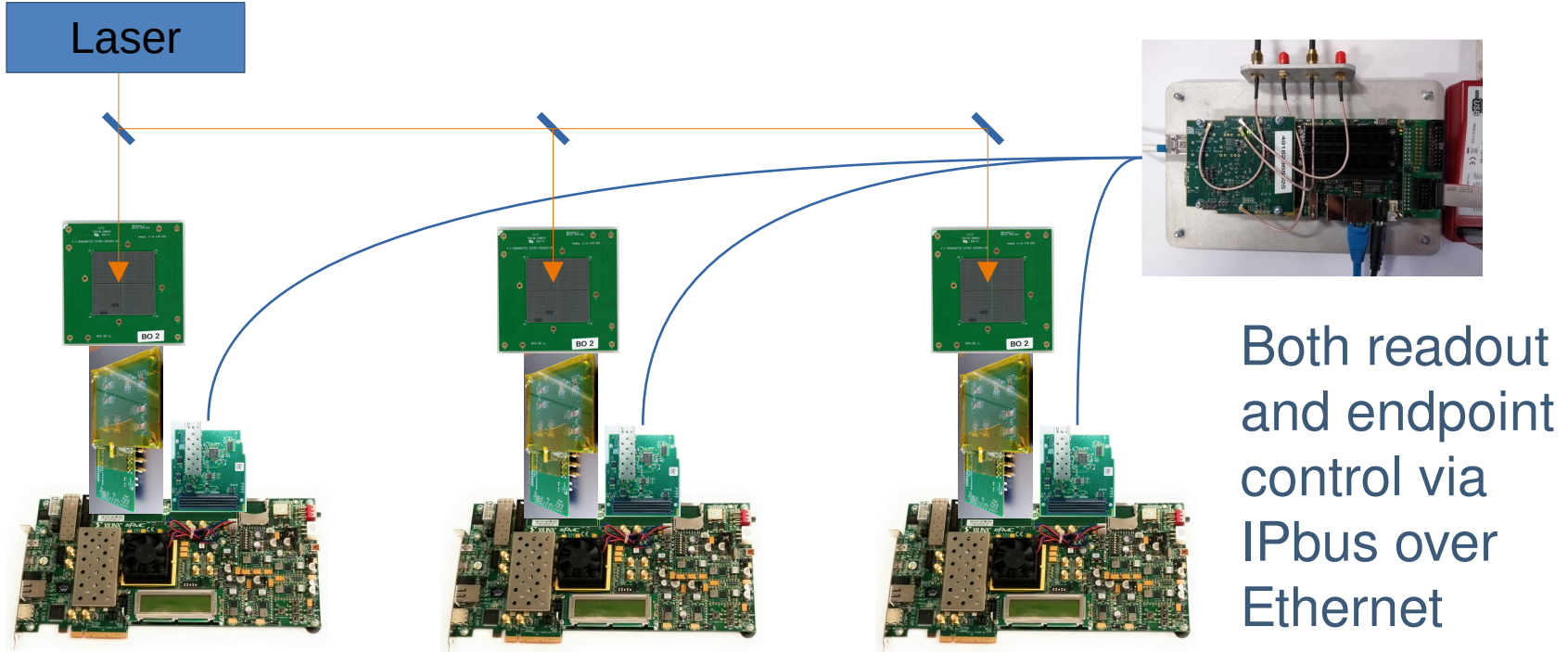


# Timing Exercise With ALCOR DAQ in ARTIC

- Bristol designed a reference Timing Endpoint
  - They can provide an FMC mezzanine, FW and SW (uses Ipbus)
  - Acts as master or endpoint depending on loaded firmware
- We can plug these in our VC707 DAQ boards
- We need also a timing master board



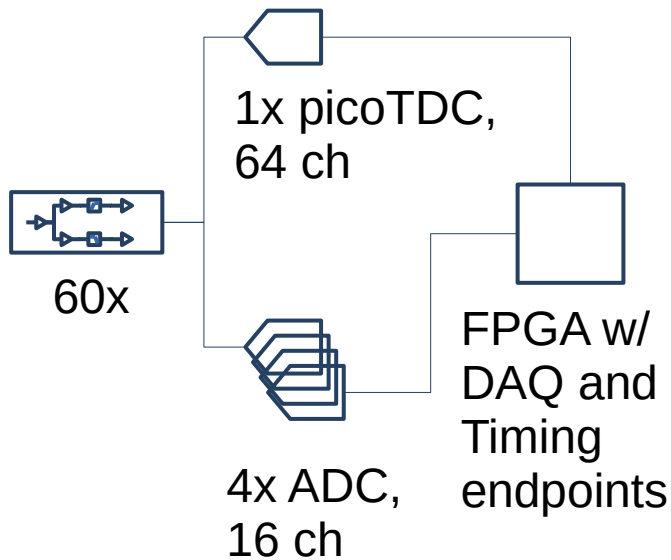
# Timing Exercise With ALCOR DAQ



- The VC707 has several SMA outputs that can be used to measure clocks (after its own PLL, but it may still be useful)

# ECAL costs guesstimate

- For a 60 channel barrel module



- 1x picoTDC @ ~100 EUR??
- 4x e.g. ADS52J90 @ 150 EUR
- Timing SFP, PLL, ... 100 EUR
- Discretes at least 600 EUR
- Board and connectors ~500 EUR

- SAND common FPGA on mezzanine
  - e.g. TE0813 (ZU4CG) @ 400 EUR

- O(50) EUR/ch, not including VAT, any R&D costs, different boards for endcap