TRIGGER module update

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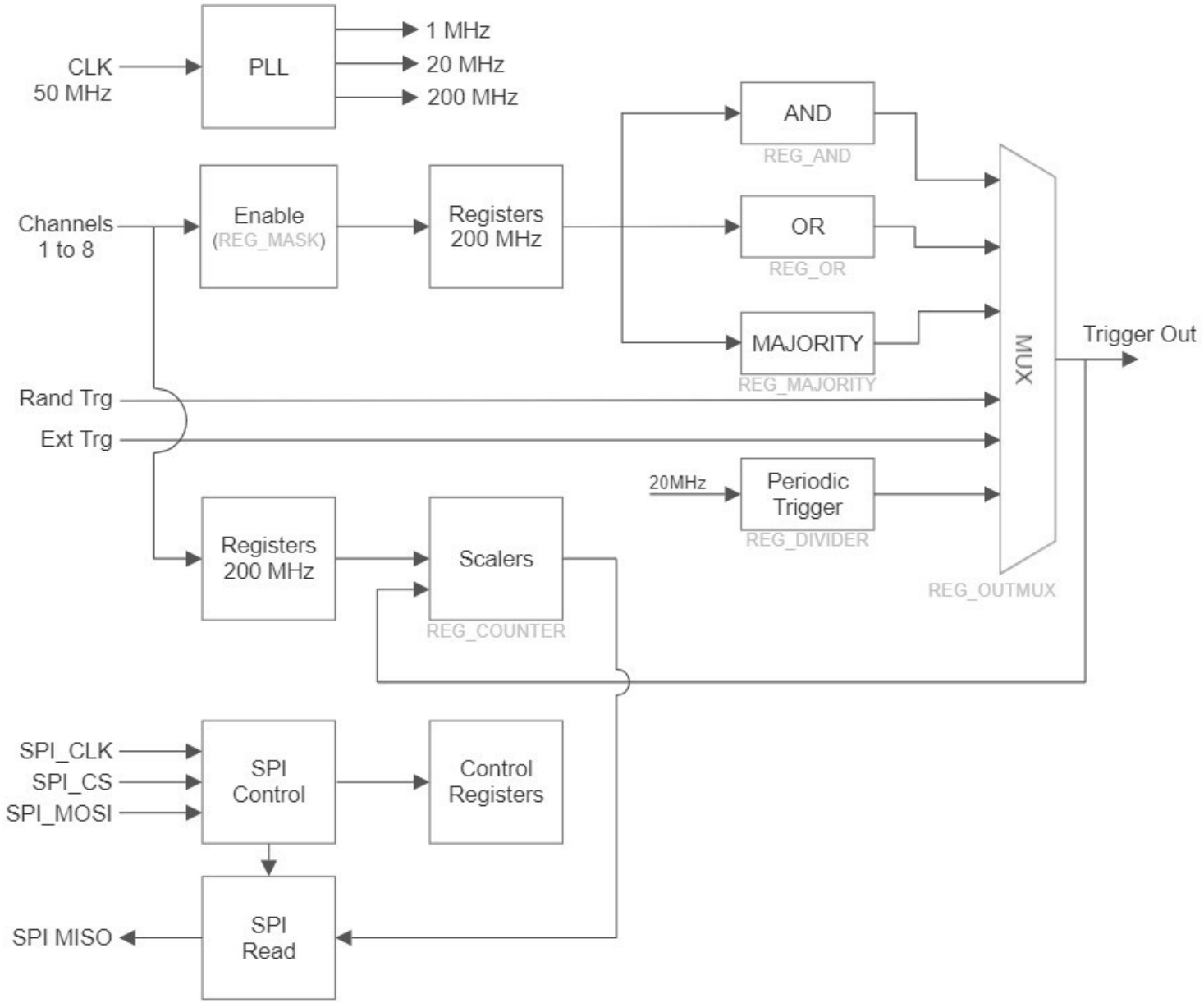
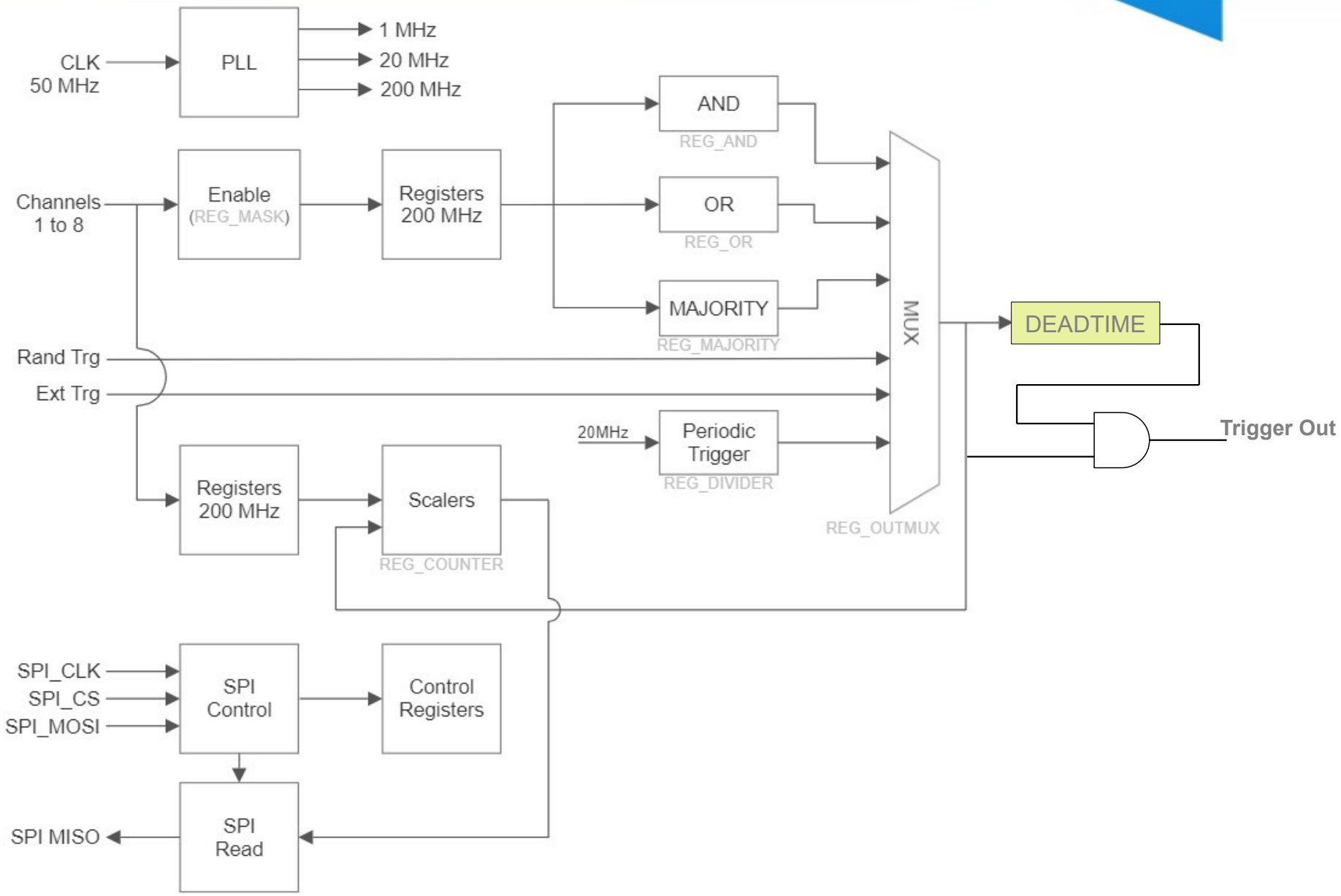
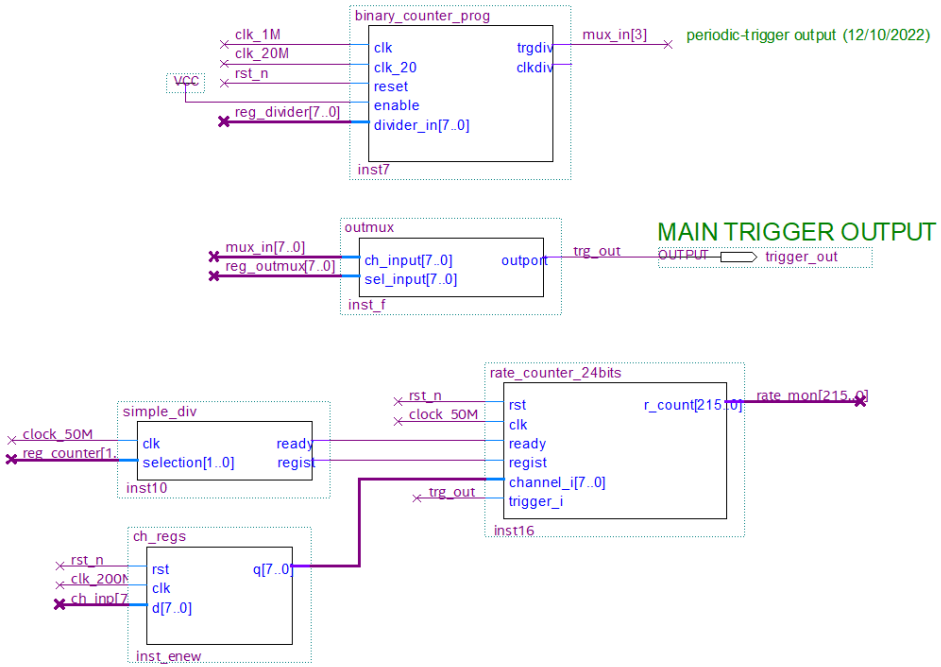
FPGA firmware overview



FPGA firmware overview

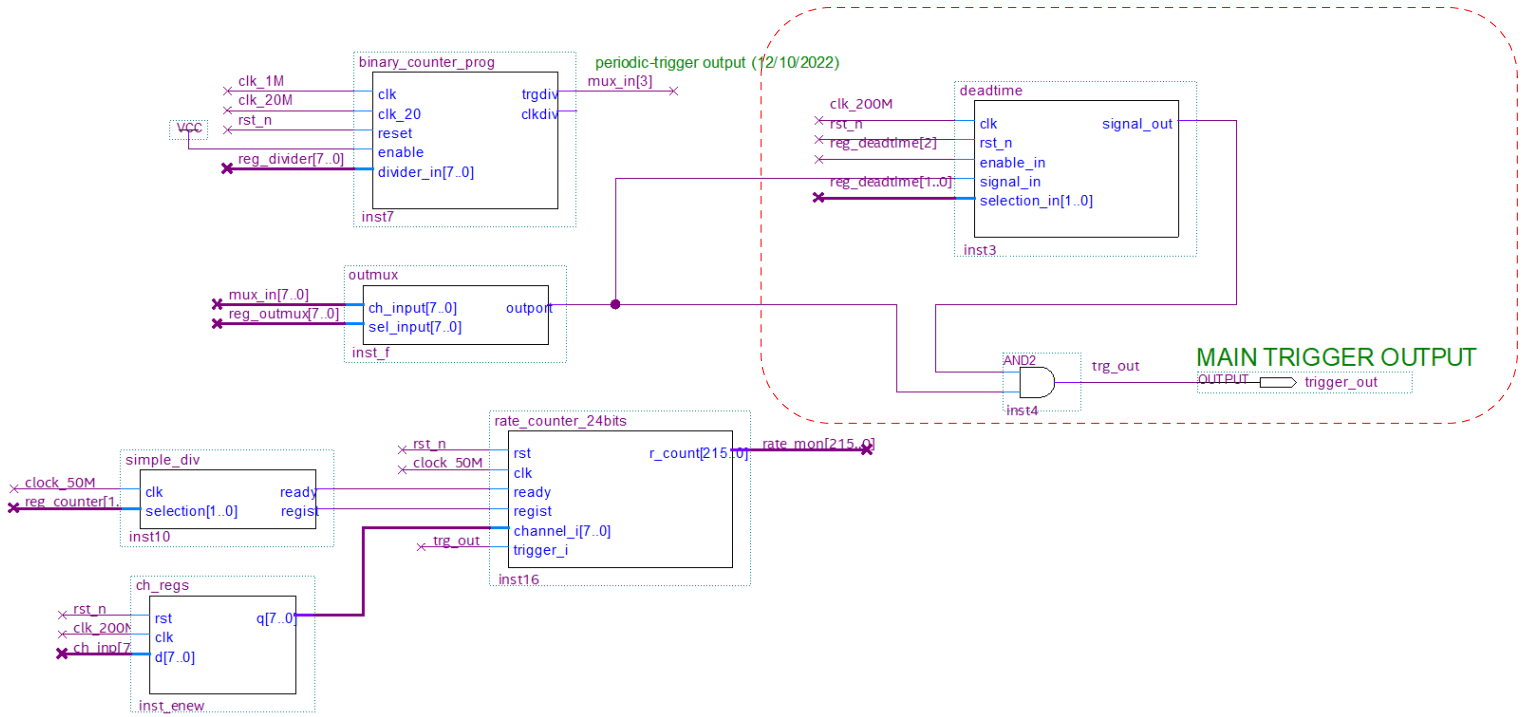


FPGA firmware



Trigger Output now in LIME

New Trigger Output for LIME



STATUS

- **Inputs:**
  - ✓ 4 PMT channels (expected rate 1 kHz, with some tolerance 0.2-50 kHz)
  - ✓ Gate DAQ server (signal ‘gate_in’ - pin allocated, how the input signal should be used?)
  - ✓ Camera exposure (signal ‘camera_in’ - pin allocated, how the input signal should be used?)
  - ✓ External Trigger input (signal ‘trigger_in’, selected when REG_OUTMUX=5)
  - ✓ External clock (needs to use a specific pin, hardware modification needed in Rome’s module)

- **Trigger logic:** the trigger is AND with (Gate DAQ server) AND (Camera exposure)
  - ✓ Majority
  - ✓ And
  - ✓ Or
  - ✓ Periodic (10-100 Hz)
  - ✓ Random

- **Outputs:**
  - ✓ Trigger with/without DEADTIME
  - ✓ Busy
  - ✓ Clock (either the external or an internal one)

** new feature*
** to be implemented*

STATUS

- **Trigger Deadtime**: configurable time window in the FPGA to block any trigger in a given time after a new trigger. Current options: 10us, 25us, 50us, 100us. New configuration register:
  - ✔ 10 us (REG_DEADTIME=4),
  - ✔ 25 us (REG_DEADTIME=5),
  - ✔ 50 us (REG_DEADTIME=6),
  - ✔ 100 us (REG_DEADTIME=7).

- **Counters**: tested and working 16-bits counters on PMT channels 1 to 4 and 8 bits on Trigger output. Four configurable time bases:
  - ✔ 0.5 s (REG_COUNTER=0),
  - ✔ 1.0 s (REG_COUNTER=1),
  - ✔ 10.0 s (REG_COUNTER=2),
  - ✔ 100.0 s. (REG_COUNTER=3).

- Data payload: counters and time stamp

** new feature*
** to be implemented*