BES-III OFF-DETECTOR READOUT ELECTRONICS FOR THE CGEM-IT DETECTOR: status report





SUMMARY:

- GEMROC Modules
 - hardware upgrade/fix description:
 - Clock Booster upgrade installation
 - TPULSE SYNCHRST fix
 - inventory
- GEM-DC (Data Concentrator, Uppsala University, Pawel Marciniewski)
 - Firmware upgrade description and status
 - Hardware survey
- GEMROC integration in BES-III Slow/Run control/DAQ software
- CGEM-IT Modular Fast Control System (FCS) FANOUT: overview
 - CGEM-IT GEMROC-based FCS INTERFACE MODULE
 - hardware
 - firmware and python scripts
 - Modular FCS Local FANOUT
 - FCS termination card
 - status
- Outlook





2

GEMROC Module hardware upgrade: Clock Booster upgrade installation

ISSUE:

The main source of corruption in the serial data received at the GEMROC FPGA (detected as 10b/8b decoder errors) has been found to be the marginal quality of the clock signal reaching the TIGER FEBs on the "long haul cable + DLVPC + short haul cable" path, resulting in excessive jitter in the serial data transmitted from the TIGER to the GEMROC.

"Clock Booster Patch Cards" (CBPC) designed by Roberto Malaguti (INFN-FE) in October 2019







3

GEMROC Module hardware upgrade: Clock Booster upgrade installation

Upgrade details:

- 8 resistors must be removed from the GEMROC_IFC card
- 2 Clock Booster Patch cards must be installed across the pads of the removed resistors







GEMROC Module hardware upgrade: Clock Booster upgrade installation

Upgrade details:

- 8 resistors must be removed from the GEMROC_IFC card
- 2 Clock Booster Patch cards must be installed across the pads of the removed resistors.

More details in: «Preparazione_moduli_GEMROC_con_IFC_CARD_v4d6_EES_2023.docx», A.C.R., last modified 15 sep 2023, available at:

https://pandora.infn.it/ws-tiger-gemroc-documentation/GEMROC_AND_OTHERS/GEMROC_IFC_CARD%20(BES-III%20interface%20cm/



TODO:

GEMROC modules already at IHEP must be upgraded (A.C.R. during nov 2023 business trip)





GEMROC Module hardware upgrade: "TPULSE" "SYNCHRST" nets fix

ISSUE:

due to undetected issues in the GEMROC_IFC card schematic:

- net T3_T2_TPULSE is short circuited to net T1_T0_TPULSE
- net T3T2_SYNCHRST is short circuited to net T1T0_SYNCHRST
- net T7_T6_TPULSE is short circuited to net T5_T4_TPULSE
- net T7T6_SYNCHRST is short circuited to net T7T6_SYNCHRST FIX:
- 8 resistors must be removed from the GEMROC_IFC card
- patch wires must be installed

More details in: «Preparazione_moduli_GEMROC_con_IFC_CARD_v4d6_EES_2025.dock», A.C.R., last modified 15 sep 2023, available at:

https://pandora.infn.it/ws-tiger-gemroc-documentation/GEMROC_AND_OTHERS/GEMROC_IFC_CARD%%%BES_III%20interface%20card)



TODO: GEMROC modules already at IHEP must be upgraded (A.C.R. during nov 2023 business trip)





GEMROC Module inventory

GEMROC modules at IHEP (according to Michela's e-mail of 2 nov 2023):

- 22 GEMROC for DAQ of which 1 with possible issues reported by Giulio/Alberto
- 1 GEMROC used as GEMROC SYSTEM FANOUT

GEMROC modules at INFN-FE:

- 2 upgraded and tested
- 1 from Torino to be fixed and upgraded
- 3 GEMROC_IFC cards to be fixed (2 were damaged at IHEP) and upgraded

ArriaV GX DK-START-5AGXB3N development kits:

- 5 still sealed stocked at INFN- Ferrara as of 6 nov 2023
- 2 will remain as spare if the 3 GEMROC_IFC cards above can all be fixed and assembled into GEMROC modules

GEMROC modules enclosures:

- plenty of off-the-shelf enclosures available
- 4 enclosures being custom machined at INFN-Ferrara





ISSUES:

A GEM-DC module was read out in 2019 at IHEP via a VME CPU. The GEM-DC was properly configured and readout in polling mode: the VME CPU needed to poll the status register of the GEM-DC to know when an event was ready to be readout.

BES-III DAQ expert requested that the GEM-DC would be upgraded to:

- generate VME interrupt request (IRQ) when ready to be readout
- handle the subsequent VME interrupt acknowledge cycle originated by the VME CPU

FIX:

Pawel upgraded the GEM-DC firmware during his stay at Ferrara (28-31 mar 2023). Subsequent tests showed issues with the interrupt generation for which a patch was prepared at INFN-Ferrara (P.M. / A.C.R.). In order to compile, download and test the patch a dedicated notebook has been prepared (A.C.R.).

STATUS:

A test of the modified GEM-DC has been carried out at INFN-Ferrara by installing the GEM-DC in a VMP crate equipped with a CAEN VX1718 - VME-USB2.0 Bridge.

The verification of the firmware modification is still in progress, due to lack of time and some limitations in the generation of the VME interrupt acknowledge cycle for the USB2.0-driven version of the VME bridge. An attempt at a more conclusive test will be performed during the integration week at IHEP.





A test of the modified GEM-DC has been carried out at INFN-Ferrara by installing the GEM-DC in a VME crate equipped with a CAEN VX1718 - VME-USB2.0 Bridge.

The screenshot reported in the next slide is from the "ChipScope" tool of the Xilinx-ISE development suite used on a dedicated notebook to open the "ATLB_CGEM" design by Pawel Marciniewski, Uppsala University.

The activity captured in the GEM-DC FPGA refers to its VME interface and shows that the firmware is not properly responding to the IACK_IN signal from the CPU: the GEM-DC propagates directly the IACK signal to the IACK_OUT line even when the GEM-DC contains an event to be read out.

In order to trigger this activity I had to:

- reset the GEM-DC by writing 0x10000 to the GEM_DC CSR register
- enable the generation of IRQ1 by the GEM-DC by writing 0x101 to address 0x400000 in the GEM-DC address space. Note: when I do this the IRQ1 of the dataway display of the CAEN VME Bridge immediately turns OFF
- start an "INTERRUPT CHECK" routine of the CAEN VME bridge control software by choosing option "I" of the user interface menu. Note: the interface prints 0x3E as the status of the VME IRQ lines seen by the bridge
- repeat (???) the step above: at this time the Interrupt acknowledge cycle is really performed by the bridge on the VME BUS and the "ChipScope" detects the trigger condition (V_IACK_IN going LOW) and captures the FPGA activity (unfortunately its shows that the firmware fails to respond properly)



The "ChipScope" must be setup by pointing to a specific project in the ATLB_CGEM hierarchy which associates meaningful label to the generic ID of the signals saved in the FPGA for the ChipScope capture.

Waveform - DEV:1 MyDevic Bus/Signal X © fsmi_out 0 o reg_sol 40 • reg_sol 0 • sst_grale_c 00 • sst_grale_c 00 • sst_grale_c 00 • v_a FFFFF • v_a FFFFF • v_a 3F - v_lword 1 - v_write 1 - v_eas 1 - v_berr 1 - v_ptery 1	value cc1 (XC5VL) 0 400 0 400 0 400 0 400 0 400 1 1 1 1 1 1	X X X X X X X X X X X X X X X X X X X	Kadix 0 80 1 X 00 0 X 14 X X	Counter
Waveform - DEV:1 MyDevice Bus/Signal X 0 fsmi_out 0 0 reg_sel 40 0 sst_cycle_c 00 0 est_cycle_c 00 0 sst_cycle_c 00 0 sst_cycle_c 00 0 sst_cycle_c 00 0 sst_cycle_c 01 0 sst_cycle_c 01 0 v_adr 14 0 v_adr 14 0 v_adr 14 0 v_adr 11 0 v_une 11 0 v_est 11 0 v_estry 11 0 v_etry 11	cel (XC5VL Q QO 0 0 40 0 0 0 1 1 1 1 1 1	X X X X X X X X X X X X X X X 0 0 -320 -240 -160 -80 0 40 40 	0 80 1 0 00 0 0 X 14 X 14	60 240 320 400 480
Waveform - DEV:1 MyDevic Bus/Signal X 0- fsmi_out 0 0- reg_sel 40 0- sst_cycle_c 00 0- sst_cycle_c 00 0- sst_cycle_c 00 0- v_a FFFF. 0- v_adr 14 0- v_un 3F -v_lword 1 -v_vas 1 -v_ess 1 -v_retry 1 -v_retry 1	Cce1 (XC5VL 0 400 0	X 0 7LX50T) UNIT:0 VME (ILA) -320 -240 -160 -80 40 40 FFFFFFFF 3F	X 0 0 0 0 0 X 14 X 14 X	60 240 320 400 480
Waveform - DEV:1 MyDevic Bus/Signal X \circ fsmi_out 0 \circ reg_sel 40 \circ sst_cycle_c 00 \circ sst_cycle_c 00 \circ sst_dran FFFF $\circ \circ$ v_adr 14 \circ v_am 3F $- v_1$ Word 1 $- v_sas$ 1 $- v_sas$ 1 $- v_ses$ 1 $- v_retry$ 1 $- v_retry$ 1	ccel (XC5VL 0 400 0	0 0 /LX50T) UNIT:0 VME (ILA)	0 80 1 0 00 0 0 X 14 X 14	60 240 320 400 480
Waveform - DEV:1 MyDevic Bus/Signal X 0 5 fsmi_out 0 0 reg_sel 40 0 sst_cycle_c 00 0 sst_cycle_c 00 0 sst_trans_rate 0 0 v_adr 14 0 v_am 3F -v_lword 1 - -v_ss 1 -v_ess 1 -v_berr 1 -v_etry 1 -v_ddir 0	Cel (XC5VL O 0 40 0 0 0 0 0 0 0 0 0 0 0 0 0	/LX50T) UNIT:0 VME (ILA)	0 80 1 X 00 X 14 X 14 X	60 240 320 400 480
Sga Waveform - DEVT MyDevic Bus/Signal X 0-fsmi_out 0 0-reg_sel 40 0-sst_crycle_c 00 0-sst_crycle_c 00 0-sst_crycle_c 00 0-sst_crycle_c 00 0-v_adr FFFF 0-v_adr 14 0-v_am 3F -v_lword 1 -v_urite 1 -v_berr 1 -v_tretry 1 -v_ddir 0	O WO 0 WO 0 WO 40 WO 00 WO 14 WO 3F WO 1 WO 1 WO 1 WO 1 WO 1 WO 1 WO	.12.501) UNI: 0 VME (ILA) .320 .240 .160 .80 0	0 80 1 X 00 00 X X 14 X X	60 240 320 400 480 C FF 00000004 00
Bus/Signal X • fsmi_out 0 • fsmi_out 0 • set_cycle_c 00 • set_cycle_c 00 • vac FFFF • v_a FFF • v_adr 14 • v_uan 3F - v_lword 1 - v_vorite 1 - v_perr 1 - v_tetry 1 - v_ddir 0	0 20 400	-32U -24U -10U -8U 	U 80 1 X 00 0 X X 14 X	00 240 320 400 480
• fsmi_out 0 • reg_sel 40 • sst_cycle_c 00 • sst_vrans_rate 0 • v_adr FFFF.FF • v_adr 14 • v_am 3F - v_lword 1 - v_vrite 1 - v_sa 1 - v_erst 1 - v_drit 1	0 40 0 5 5 7 5 7 7 7 1 1 1 1 1 1 1	0 40 FFFFFFF 3F	X 00 0 X 14 X 14 X	C FF 00000004
○ reg_sel 40 ○ sst_cycle_c 00 ○ sst_trans_rate 0 ○ st_trans_rate 0 ○ v_adr 14 ○ v_am 3F - v_lword 1 - v_ss 1 - v_ss 1 - v_ss 1 - v_ss 1 - v_est 1 - v_retry 1 - v_ddir 0	40 00 FFFF: 14 3F 1 1 1 1 1	40 FFFFFFF 3F	X 00 0 X 14 X 14 X	FF 00000004 00
	00 0 FFF: 14 3F 1 1 1 1 1 1 1 1 1 1	FFFFFFF	00 0 X 14 X	00000004
• •sst_trans_rate 0 • • v_a FFFF • • v_adr 14 • • v_am 3F - v_lword 1 - v_write 1 - v_berr 1 - v_tretry 1	0	FFFFFFF	0 X 14 X	00000004
0 ~ v_a FFFF FI 0 ~ v_adr 14 0 ~ v_am 3F - v_lword 1 - v_vrite 1 - v_berr 1 - v_berr 1 - v_retry 1	FFF: 14 3F 1 1 1 1 1 1 1	FFFFFFF	X14	00000004
0. v_adr 14 0. v_am 3F -v_lword 1 -v_write 1 -v_berr 1 -v_berr 1 -v_tretry 1	14 3F 1 1 1 1	3F	X 14 X	00
• v_anr 14 • v_anr 3F - v_lword 1 - v_write 1 - v_berr 1 - v_berr 1 - v_retry 1	14 3F 1 1 1	3F	X	00
organ 3F -v_lword 1 -v_write 1 -v_ss 1 -v_ber 1 -v_retry 1 -v_ddir 0	3F 1 1 1 1	3F		00
-v_lword 1 -v_write 1 -v_as 1 -v_berr 1 -v_retry 1 -v_ddir 0	1			
-v_write 1 -v_as 1 -v_berr 1 -v_retry 1 -v_ddir 0	1			
-v_as 1 -v_berr 1 -v_retry 1 -v_ddir 0	1			
-v_berr 1 -v_retry 1 -v_ddir 0	1			
-v_retry 1 -v_ddir 0				
v_ddir 0	1			
	0			
- u adán - O				
V_adii 0				
add_ph2_ok 1	-			
add_ph1_ok 1	1			
-add_sst_ok 0	0			
add_mb_ok 0	0			
-add_bl_ok 0	0			
add_sg_ok 1	1			
fifo wr inc 0	0			
fife empty 0				
0	° –			
v_iack 1	1			
v_iackin 1	1			
v_iackout 1	1			
1 m				
	-fifo_wr_inc 0 -fifo_empty 0 -fifo_full 0 -v_iack 1 -v_iackin 1 -v_iackout 1	fifo_wr_inc 0 0 fifo_empty 0 0 fifo_tall 0 0 v_iack 1 1 v_iackin 1 1 v_iackout 1 1	fifo_wr_inc 0 0 fifo_empty 0 0 fifo_full 0 0 v_iack 1 1 v_iackin 1 1 v_iackout 1 1	fifo_wr_inc 0 0 fifo_empty 0 0 fifo_fill 0 0 v_iack 1 1 v_iackin 1 1 v_iackout 1 1

10

INFN

Istituto Nazionale di Fisica Nucleare DEGLI STUDI DI FERRARA

Unfortunately the "ChipScope" record shows that the firmware fails to respond properly to the IACK transaction \rightarrow the firmware was then modified but not tested again. Further debugging could take place at IHEP (A.C.R. nov 2023)

	Waveform - DEV:1	MyDevice1	1 (XC5V	VLX50T) UNIT:0 VME (ILA)
Anitor Console	Bus/Signal	x o	400	-360 -320 -280 -240 -200 -160 -120 -80 -40 0 480 120 160 200 240 280 320 360 400 440 480 520 560
r Setup	edi	FFFF FFFF	F	FFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFF
rm -	e fan out	00 00		
	Cont out	00 00		
O (ILA)	- ISHI_OUC	0 0		
Setup	v- reg_sei	40 40		11 04
m	• sst_cycle_c	00 00	° 📥	00
t	◦ sst_trans_rate	0 0	•	0
DW_CTRL_VME (ILA) Setup	°~ v_a	FFFF. FFFF	F.	FFFFFFF X 00000004
m	⊶ v_adr	14 14	4	14
	∽v_am	3F 31	F _	3F X 00
· 🖻	v_lword	1 1	1	
AT: 0	v_write	1 1	1	TT Promot dei comandi - CAENVMEDemo.exe V17180 —
ount a	- v_as	1 7	1	
	-v berr	1 1	1	CAEN VME Manual Controller
	v retry	1 2	1	
	-v ddin	0 0		R - READ
vord	v_uuii			B - BLOCK TRANSFER READ
s	v_adir	0 0		T - BLOCK TRANSFER WRITE
err	-add_ph2_ok	1 1	1	I - CHECK INTERRUPT
etry tack	add_phl_ok	1 1	1	1 - ADDRESS [14400000]
dir	add_sst_ok	0 0	0	3 - 045 ADML33 [AG0000] 3 - 0471 [032]
dir Lob2 ok	add_mb_ok	0 0	0	4 - ADDRESSING MODE [A32]
	add_bl_ok	0 0	0	5 - BLOCK TRANSFER SIZE [256]
Lsst_ok	add_sg_ok	1 1	1	
_hb_ok	-fifo_wr_inc	0 (0	8 - VIEW BLT DATA
_sg_ok	fifo_empty	0 (0	F - FRONT PANEL I/O
_wr_inc rd_inc	- fifo_full	0 1	0	A - EXECUTE SCRIPT FILE
empty	v jack	1		A - Kort Halor Counterry
ckin	-v jackin	1 2	1	Bus Error !!!
ck	-v jackout	1		INO status: 35
at_broken[252] 531	72(252)			walling for intertupt ress any key to stop.
4]	12[200]		۳ <u>⊢</u>	
kout		4 > 4 >		
	Waveform of	aptured 27	7-apr-20	0123 12:26:24 X:400 € C:400 € Δ(X-0):0

11

BES-III Italia workshop, Ferrara, 6 nov 2023, A. Cotta Ramusino

DI FERRARA

GEM-DC: Hardware survey

GEM-DC modules at IHEP :

• 1 GEM-DC; it was left with the BES-III DAQ experts by Pawel during his business trip to IHEP in 2019

GEM-DC modules at INFN-FE:

- 1 GEM-DC sent by LNF
- 2 GEM-DC brought by Pawel during during his business trip to INFN-Ferrara in March 2023.





GEMROC integration in BES-III Slow/Run control/DAQ software

CGEM-IT Online Software architecture – BASELINE:

- TIGER Power Control and Detector Environmental Control (FEB Vsupply, FEB Isupply, FEB Temp, GEMROC Temp):
 - performed via Ethernet UDP by the CGEM-IT SLOW CONTROL software
- GEMROC T_{delay} scan, Threshold scan, diagnostic mode setup, DAQ_PAUSE etc.:
 - performed via Ethernet UDP by the CGEM-IT RUN CONTROL software
- CGEM-IT trigger matched readout: performed by CGEM-IT DAQ software via the GEM-DCs over VME bus

CGEM-IT Online Software development:

CGEM-IT SLOW / RUN CONTROL software development at BES-III:

- The development of the SLOW and RUN control software is being carried out by BES-III experts to some extent by porting the routines included in the omni-comprehensive GUFI framework written by Alberto Bortone.
- Minor issues in the porting process have been flagged from time to time by BES-III experts and have been addressed and solved by Alberto.
- Most substantial issue so far: some of the fields of the UDP packet exchanged between host PC and GEMROC modules to perform SLOW / RUN control functions could be modified by both the SLOW and the RUN control programs, leading to possible inconsistencies if the SLOW and the RUN control programs are independent processes, as in BES-III.

The solution proposed by Alberto Bortone was adopted because it requires minimal changes to the data format of the protocol (Ethernet UDP based) of communication between the GEMROC and the host PC and thus minimal changes to the SLOW/RUN control software routines.





GEMROC integration in BES-III Slow/Run control/DAQ software

CGEM-IT DAQ software development at BES-III:

The development of the CGEM-IT DAQ software should have been, in the original plans, the earliest to occur, because of being based on the VME readout of GEM-DC cards and because of:

- the availability of the GEM-DC cards right from the start.
- the possibility for the GEM-DC to generate dummy data formatted according to a format defined in collaboration with the BES-III DAQ experts and thus the potentiality to test unpacking routines and data integrity checks.

The development of the DAQ software has started in 2019 and is proceeding now instead but being based on a solid VME architecture it should proceed fast.

A GEM-DC module was tested in 2019 and data generated (by internal test pulse) by a GEMROC connected to the GEM-DC was readout.

For this test the VME CPU had to poll the GEM-DC status register to know when the data was ready and then schedule the read. A VME IRQ-based readout mode is preferred instead.

Requirements to the GEM-DC firmware developer by the BES-III DAQ expert:

In a dedicated meeting with the BES-III DAQ experts (XiaoLu Ji, Ma Si, Tingxuan Zeng) recently organized on October 5th 2023 by Michela, the experts re-stated that:

- The GEM-DC shall generate a VME interrupt request (IRQ) when ready to be readout and handle the subsequent VME interrupt acknowledge (IACK) cycle originated by the VME CPU. The request and its implementation have been discussed above.
- **BES-III DAQ will read one event from the GEM-DC for every L1 TRIGGER** it releases the requirements on the GEM-DC on-line memory because it is not required to buffer more than one event (an event in the GEM-DC is assembled by merging the Trigger matched event packets received from the connected GEMROCs).





14

GEMROC integration in BES-III Slow/Run control/DAQ software

Requirements to the GEMROC firmware developer by the BES-III DAQ expert:

In the dedicated meeting with the BES-III DAQ experts above cited, the experts also reviewed:

- The proposed approach to use the DAQ_PAUSE flag to put the CGEM-IT detector in a "On-hold" state after initial configuration by the RUN control software. Currently it is foreseen for the GEMROC modules to exit the "On-hold" state upon the first received L1Trigger (which also causes the generation of a "SOFT RESET within each GEMROC and to the connected TIGERs to reset the timing measurement units). This approach was favourably commented by the DAQ experts.
- The handling of the Trig_Check signal by the GEMROC firmware. This analysis resulted in the following **REQUIREMENT:**
 - IF a mismatch of the distributed "L1_CHK" signal and the one internally calculated by the GEMROC (by counting the L1 triggers modulo 256) occurs **THEN** the GEMROC should set a "L1_CHK_ERROR" flag in all the following trigger matched output data packets to inform the online DAQ software about the mismatch condition.



•

BES-III Italia workshop, Ferrara, 6 nov 2023, A. Cotta Ramusino



15

CGEM-IT MODULAR FCS FANOUT: overview

The BES-III Fast Control (Timing/trigger) System:

- CLK, L1, L1 CHK are sourced by the BES-III FCS □ signal level: pECL
- global FULL signal from the CGEM subdetector is sinked by the **BES-III FCS**
 - signal level: pECL

JNIVERSITÀ Degli studi Di ferrara





CGEM-IT GEMROC-based FCS INTERFACE MODULE

The CGEM-IT FCS INTERFACE MODULE is a modified GEMROC module which connects to the CLK, L1, L1 CHK, FULL signals from the BES-III Fast Control System.

It is made programmable to generate simulated Fast Control signals

- The CGEM-IT FCS INTERFACE MODULE has:
- 4 FAN OUT ports for CLK, L1, L1_CHK (LVDS) TO the 4 groups of GEMROC installed around the BES-III detector (North East, South East, North West, South West)
- 4 FAN IN ports for the FULL signals from each of the 4 groups of GEMROC installed around the BES-III detector
- 2 FAN OUT ports for CLK, L1, L1_CHK (NIM) TO the 2 GEM-DC
- 2 FAN IN ports for FULL (NIM) FROM the GEM-DC

The FCF will be located at the top of the detector, close to the BES-III "BES-III FCS Card" assigned to the C-GEM detector



17

CGEM-IT FCS INTERFACE MODULE:Hardware

The CGEM-IT FCS INTERFACE MODULE is based on a GEMROC module.

Details on the preparation necessary are given in the file:

"Preparaz moduli GEMROC con IFC CARD v4d3 LINK FCSFanout 2021 v2.docx" available at:

https://pandora.infn.it/ws-tiger-gemroc-documentation/GEMROC_AND_OTHERS/GEMROC_FCS_FANOUT_MASTER

Below a picture of the setup at INFN Ferrara (A.C.R. nov 2023) to test the Local FCS FANOUT modules.







CGEM-IT FCS INTERFACE MODULE: Firmware and Python scripts

The CGEM-IT FCS INTERFACE MODULE is controlled by the exchange of UDP packets from a host PC. The packet protocol and the Python scripts to control the to emulate the CGEM-IT FCS INTERFACE MODULE are available at the repository shown in the next slide.

Command Prompt - python FCS_FANOUT_UI_2021.py 7 0xf	- 0 X
:\angelo\BES III\FCS_FANOUT_UI>python FCS_FANOUT_UI_2021.py 7 0xf	
EMROC_FCS_FANOUT_CFG V1.1; last mod: 2021-04-14, A.C.R. INFN-FE;	
ENU:	
FCW	SysFanoutConfigWrite: read the default settings file and update the SYS FANOUT configuration register with its contents.
FCR	SysFanoutConfigRead: read and print setting of GEMROC SYS FANOUT configuration register
FRST	SysFanoutConfigReset
FHR	SysFanout HARD RESET
KEXT <on_off_param></on_off_param>	Select Clock source for SysFanout functions: "1" for clock derived from External source; "0" for for clock derived from on-board g
nerator	
KSIM <on_ott_param></on_ott_param>	Set to "1" for the SysFanout to generate simulated BES-III CLK signal; set to "0" to output the real BES-III CLK signal; default i
CSSIM <un_off_param></un_off_param>	Set to "1" for the SysFanout to generate simulated FLS signals: L1, L1_LHK; set to 0 to output the real BES-III FLS signals; der
	C_{1} to C_{2} and C_{2}
"0"	Set to 1° to select 1x frequency divider and 0° to select 4x frequency scaling (40mHz -> 10mHz) for the output clock, default 1s
P2CHK <on_off_param></on_off_param>	Tpulse_Merged_With_L1Chk_enable: set to "1" to mix a TP pulse (4 CLK periods wide) onto the L1_CHK line; default is "0"
TG <num generated="" soft_tp=""> (range 1 to 1023) <interval (<="" between="" in="" soft_tp="" td="" us=""><td>approx)> (range 1 to 511) <tp_width_in_burst>(0 thru 15) Soft Test Pulse Generation.</tp_width_in_burst></td></interval></num>	approx)> (range 1 to 511) <tp_width_in_burst>(0 thru 15) Soft Test Pulse Generation.</tp_width_in_burst>
	Note: period between "soft" test pulses is determined by the execution speed of the test pulse generation routine by the microcon
roller implemented in FPGA	
L1G <num generated="" soft_l1=""> (range 1 to 1023) <interval between="" in="" soft_l1="" td="" us<=""><td>(approx)> (range 1 to 511) Soft L1 trigger generation.</td></interval></num>	(approx)> (range 1 to 511) Soft L1 trigger generation.
	Note: period between "soft" L1 is determined by the execution speed of the L1 pulses generation routine by the microcontroller im
lemented in FPGA	
ULL <on_off_param></on_off_param>	Set to "1" for the SysFanout to generate a dummy FULL output to BES-III FCS system; set to "0" to clear the dummy FULL; default is
DUMFULL <pre>cpattern_param> range 0x0 to 0xf </pre>	Set a pattern of dummy FULL signals URed to the FULL signals from each of the SYS FANOUT input ports (on KEL connectors)
FULLEN <pattern_param> range 0x0 to 0x1</pattern_param>	Set a pattern of ENABLE bits to the FULL signals (true FULL signals from each of the SYS FANOUT input ports (on KEL connectors) UK
a with DUMMY FULL signals)	C. t. t. "4" to each to the TOUR FCC inpute driven by DFC III. if this hit is get to "A" then the FCC signals sawe from the simulaton
KUEFUS KUN_UTT_PARAMAX	set to 1 to enable the TRUE FCS inputs driven by BES-111, if this bit is set to 0 then the FCS signals tome from the simulator
	Sotup the SVS EANOUT to energite in the planar gam satur at FE
Abtru (A)uit: loovo	setup the Sis PANOOT to operate in the planar gem setup at PE
Quit. icave	



BES-III Italia workshop, Ferrara, 6 nov 2023, A. Cotta Ramusino

19



CGEM-IT FCS INTERFACE MODULE: Firmware and Python scripts

The CGEM-IT FCS INTERFACE MODULE firmware, UDP packet definition and Python scripts are shared here:

$\leftarrow \ \rightarrow \ \mathbf{G}$	🛇 🖞 🖻 🗝 https://pandora.infn.it/ws-tiger-gemroc-documentation/GEMROC_AND_OTHERS/GEMROC_FCS_FANOUT_MASTER
💊 Come iniziare 🛛 🔼 ownCloud	
Angelo Cotta Ra :	TIGER GEMROC documentation / GEMROC_AND_OTHERS / GEMROC_FCS_FANOUT_MASTER
ED 🛱 🗘 📅	
My Workspaces	< parent folder
Adobe	FCS_FANOUT_ACR_test_Python_scripts Modified on May, 8th
Amministrazione Centrale	GEMROC_FCS_FANOUT_MASTER_FPGA_DESIGN(ARRIAVGX) Modified on May, 8th
Mathematica	GEMROC_FCS_FANOUT_MASTER_UDP_PACKET_FORMAT Modified on May, 8th
Microsoft	GEMROC_FCS_FANOUT_MASTER_front _panel_description.pdf Modified on May, 8th
National Instruments Pandora Editing	howto_flash_ArriaVGX_board_HW_and_NIOSII_FW_acr2021_SYS_FANOUT.docx Modified on May, 8th
Sistema Informativo Solidworks	Preparaz_moduli_GEMROC_con_IFC_CARD_v4d3_LINK_FCSFanout_2021_v2.docx Modified on May, 8th





MODULAR FCS LOCAL FANOUT

The FCS LOCAL Fanout (FCLF) are a LOW COST, non programmable, fanout modules which connects to the CLK, L1, L1_CHK, FULL ports of the CGEM-IT FCS INTERFACE MODULE.

Four (+ spares) FCLF are needed The FCLF will have:

- 2 alternatives for the connection to the CGEM-IT FCS INTERFACE MODULE:
 - 1 "copper" port for LVDS signals carried by a 17- twisted pair, shielded cable ("green cable"), with auxiliary BNC ports for stand-alone operation
 - 3 fiber optic duplex ports for FCS signals (DC to 50MHz)
 - 6 output ports, each dedicated to a single GEMROC module

The FCLF(s) will be located at the middle of each of the 4 groups of FEBs located around the BES-III detector







MODULAR FCS LOCAL FANOUT Modular FCS Local FANOUT applied to the planar GEM setup at INFN-Ferrara:



The local modular fanout is used to provide FCS signals (clock and trigger) to the 2 GEMROC modules used in the setup









MODULAR FCS LOCAL FANOUT: FCS termination card







INFN Ferrara purchase order started by Nicholas Menegatti o 25 Oct 2023







OUTLOOK:

Looking forward to the integration week at IHEP in which the following goals would be pursued (subject to shared considerations on priority):

- upgrade of GEMROC Modules with the latest GEMROC_IFC card patches
- deployment of an upgraded GEMROC-based FCS INTERFACE MODULE FCS fanout
- deployment of 4 FCS LOCAL FANOUT MODULES
- commissioning of all the above at the CGEM-IT detector
- optimization of the CGEM-IT grounding and shielding layout
- debug of the GEM-DC module IRQ/IACK acknowledge functions in collaboration with the BES-III DAQ software experts





BACKUP slides





• development of the modular Fast Control Signals (FCS) FANOUT system GEMROC-based FCS <u>SYSTEM</u> FANOUT



• development of the modular Fast Control Signals (FCS) FANOUT system Modular FCS Local FANOUT

QUANTITY NEEDED:

- 6 pieces:
 - 4 in operation at BES-III
 - 1 for prompt backup at BES-III
 - 1 used for firmware debugging / development

Status:

FCS_BKPLN_IFC, FCS_BKPLN, FCS_PORT, and XCVR delivered



from a presentation to the referees, 2 jun 2021, Angelo Cotta Ramusino

development of the modular Fast Control Signals (FCS) FANOUT system •



from a presentation to the referees, 2 jun 2021, Angelo Cotta Ramusino