BES-III OFF-DETECTOR READOUT ELECTRONICS FOR THE CGEM-IT DETECTOR: status report

SUMMARY:

- GEMROC Modules
  - hardware upgrade/fix description:
    - Clock Booster upgrade installation
    - TPULSE SYNCHRST fix
  - inventory
- GEM-DC (Data Concentrator, Uppsala University, Pawel Marciniewski)
  - Firmware upgrade description and status
  - Hardware survey
- GEMROC integration in BES-III Slow/Run control/DAQ software
- CGEM-IT Modular Fast Control System (FCS) FANOUT: overview
  - CGEM-IT GEMROC-based FCS INTERFACE MODULE:
    - hardware
    - firmware and python scripts
  - Modular FCS Local FANOUT
    - FCS termination card
  - status
- Outlook

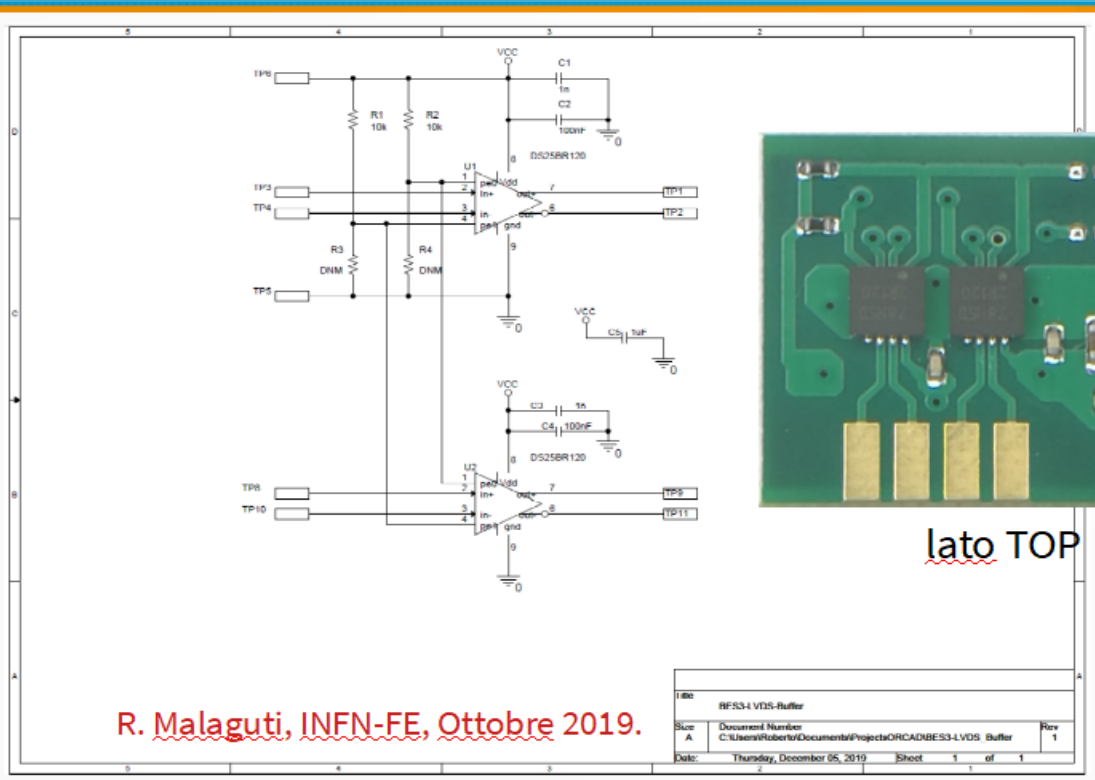
GEMROC Module hardware upgrade: Clock Booster upgrade installation

ISSUE:

The main source of corruption in the serial data received at the GEMROC FPGA (detected as 10b/8b decoder errors) has been found to be the marginal quality of the clock signal reaching the TIGER FEBs on the "long haul cable + DLVPC + short haul cable" path, resulting in excessive jitter in the serial data transmitted from the TIGER to the GEMROC.

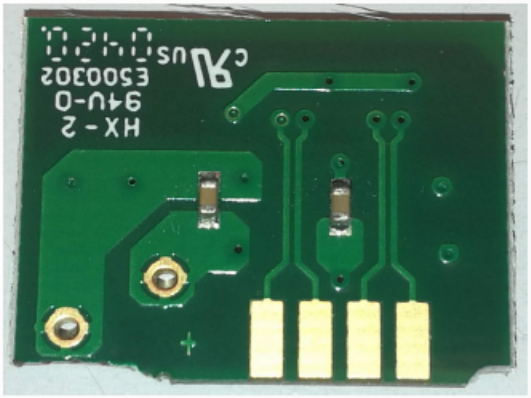
FIX:

"Clock Booster Patch Cards" (CBPC) designed by Roberto Malaguti (INFN-FE) in October 2019



Abbiamo 60 schede "LVDS Buffer" progettate da Roberto e realizzate dalla ARTEL nel 2019.

lato TOP



lato BOTTOM

GEMROC Module hardware upgrade: Clock Booster upgrade installation

Upgrade details:

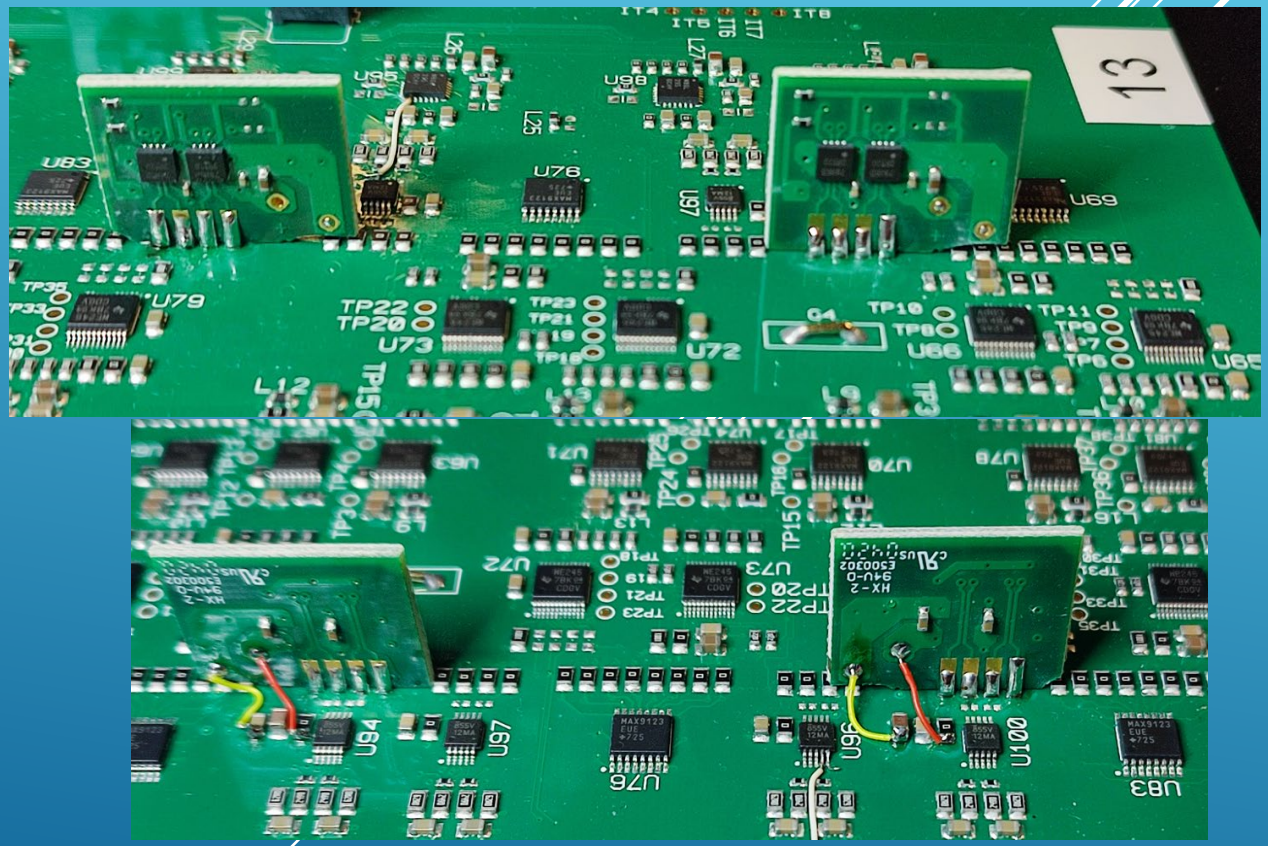
- 8 resistors must be removed from the GEMROC_IFC card
- 2 Clock Booster Patch cards must be installed across the pads of the removed resistors

GEMROC Module hardware upgrade: Clock Booster upgrade installation

Upgrade details:

- 8 resistors must be removed from the GEMROC_IFC card
- 2 Clock Booster Patch cards must be installed across the pads of the removed resistors.

More details in: «Preparazione_moduli_GEMROC_con_IFC_CARD_v4d6_EES_2023.docx», A.C.R., last modified 15 sep 2023, available at:
https://pandora.infn.it/ws-tiger-gemroc-documentation/GEMROC_AND_OTHERS/GEMROC_IFC_CARD%20(BES-III%20interface%20card)



TODO:
GEMROC modules already at IHEP must be upgraded (A.C.R. during nov 2023 business trip)

GEMROC Module hardware upgrade: “TPULSE” “SYNCHRST” nets fix

ISSUE:

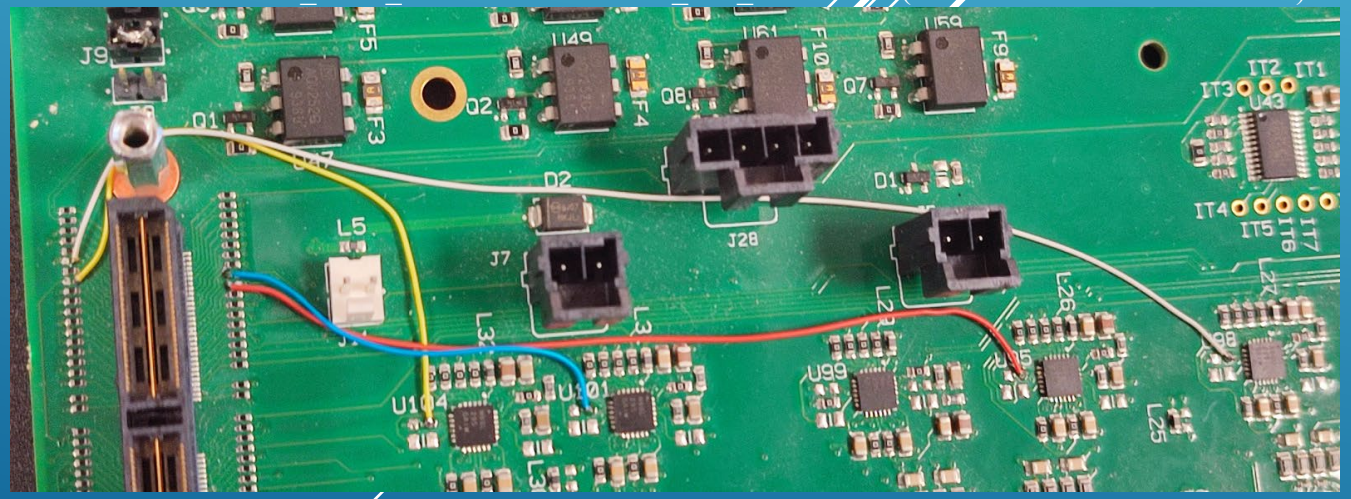
due to undetected issues in the GEMROC_IFC card schematic:

- net T3_T2_TPULSE is short circuited to net T1_T0_TPULSE
- net T3T2_SYNCHRST is short circuited to net T1T0_SYNCHRST
- net T7_T6_TPULSE is short circuited to net T5_T4_TPULSE
- net T7T6_SYNCHRST is short circuited to net T7T6_SYNCHRST

FIX:

- 8 resistors must be removed from the GEMROC_IFC card
- patch wires must be installed

More details in: «Preparazione_moduli_GEMROC_con_IFC_CARD_v4d6_EES_2023.docx», A.C.R., last modified 15 sep 2023, available at:
https://pandora.infn.it/ws-tiger-gemroc-documentation/GEMROC_AND_OTHERS/GEMROC_IFC_CARD%20(BES-III%20interface%20card)



TODO:

GEMROC modules already at IHEP must be upgraded (A.C.R. during nov 2023 business trip)

GEMROC Module inventory

GEMROC modules at IHEP (according to Michela's e-mail of 2 nov 2023):

- 22 GEMROC for DAQ of which 1 with possible issues reported by Giulio/Alberto
- 1 GEMROC used as GEMROC SYSTEM FANOUT

GEMROC modules at INFN-FE:

- 2 upgraded and tested
- 1 from Torino to be fixed and upgraded
- 3 GEMROC_IFC cards to be fixed (2 were damaged at IHEP) and upgraded

ArriaV GX DK-START-5AGXB3N development kits:

- 5 still sealed stocked at INFN- Ferrara as of 6 nov 2023
- 2 will remain as spare if the 3 GEMROC_IFC cards above can all be fixed and assembled into GEMROC modules

GEMROC modules enclosures:

- plenty of off-the-shelf enclosures available
- 4 enclosures being custom machined at INFN-Ferrara

GEM-DC: Firmware upgrade description and status

ISSUES:

A GEM-DC module was read out in 2019 at IHEP via a VME CPU. The GEM-DC was properly configured and readout in polling mode: the VME CPU needed to poll the status register of the GEM-DC to know when an event was ready to be readout.

BES-III DAQ expert requested that the GEM-DC would be upgraded to:

- generate VME interrupt request (IRQ) when ready to be readout
- handle the subsequent VME interrupt acknowledge cycle originated by the VME CPU

FIX:

Pawel upgraded the GEM-DC firmware during his stay at Ferrara (28-31 mar 2023). Subsequent tests showed issues with the interrupt generation for which a patch was prepared at INFN-Ferrara (P.M. / A.C.R.).

In order to compile, download and test the patch a dedicated notebook has been prepared (A.C.R.).

STATUS:

A test of the modified GEM-DC has been carried out at INFN-Ferrara by installing the GEM-DC in a VME crate equipped with a CAEN VX1718 - VME-USB2.0 Bridge.

The verification of the firmware modification is still in progress, due to lack of time and some limitations in the generation of the VME interrupt acknowledge cycle for the USB2.0-driven version of the VME bridge.

An attempt at a more conclusive test will be performed during the integration week at IHEP.

GEM-DC: Firmware upgrade description and status

A test of the modified GEM-DC has been carried out at INFN-Ferrara by installing the GEM-DC in a VME crate equipped with a CAEN VX1718 - VME-USB2.0 Bridge.

The screenshot reported in the next slide is from the "ChipScope" tool of the Xilinx-ISE development suite used on a dedicated notebook to open the "ATLB_CGEM" design by Pawel Marciniewski, Uppsala University.

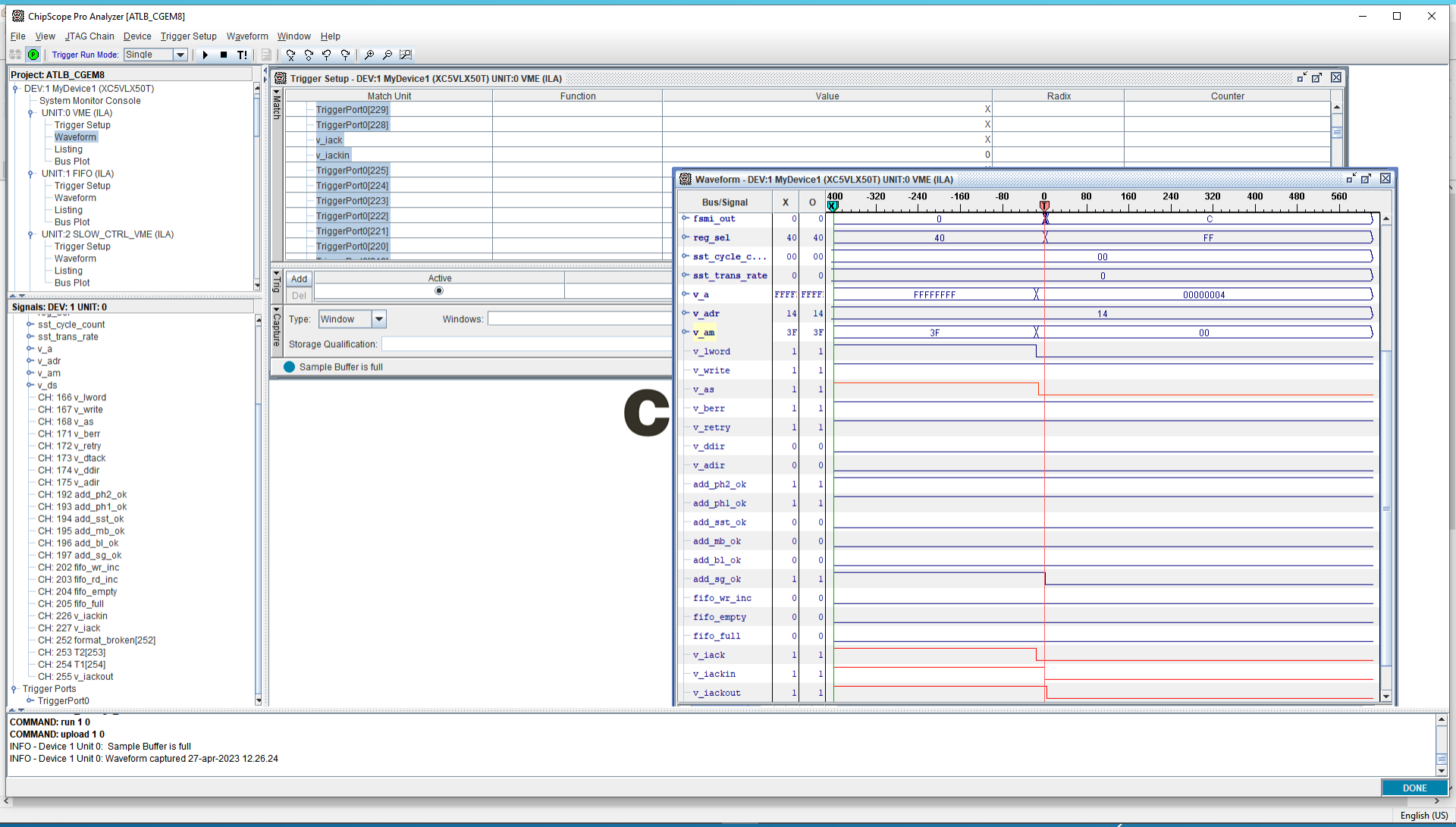
The activity captured in the GEM-DC FPGA refers to its VME interface and shows that the firmware is not properly responding to the IACK_IN signal from the CPU: the GEM-DC propagates directly the IACK signal to the IACK_OUT line even when the GEM-DC contains an event to be read out.

In order to trigger this activity I had to:

- reset the GEM-DC by writing 0x10000 to the GEM_DC CSR register
- enable the generation of IRQ1 by the GEM-DC by writing 0x101 to address 0x400000 in the GEM-DC address space. Note: when I do this the IRQ1 of the dataway display of the CAEN VME Bridge immediately turns OFF
- start an "INTERRUPT CHECK" routine of the CAEN VME bridge control software by choosing option "I" of the user interface menu. Note: the interface prints 0x3E as the status of the VME IRQ lines seen by the bridge
- repeat (???) the step above: at this time the Interrupt acknowledge cycle is really performed by the bridge on the VME BUS and the "ChipScope" detects the trigger condition (V_IACK_IN going LOW) and captures the FPGA activity (unfortunately its shows that the firmware fails to respond properly)

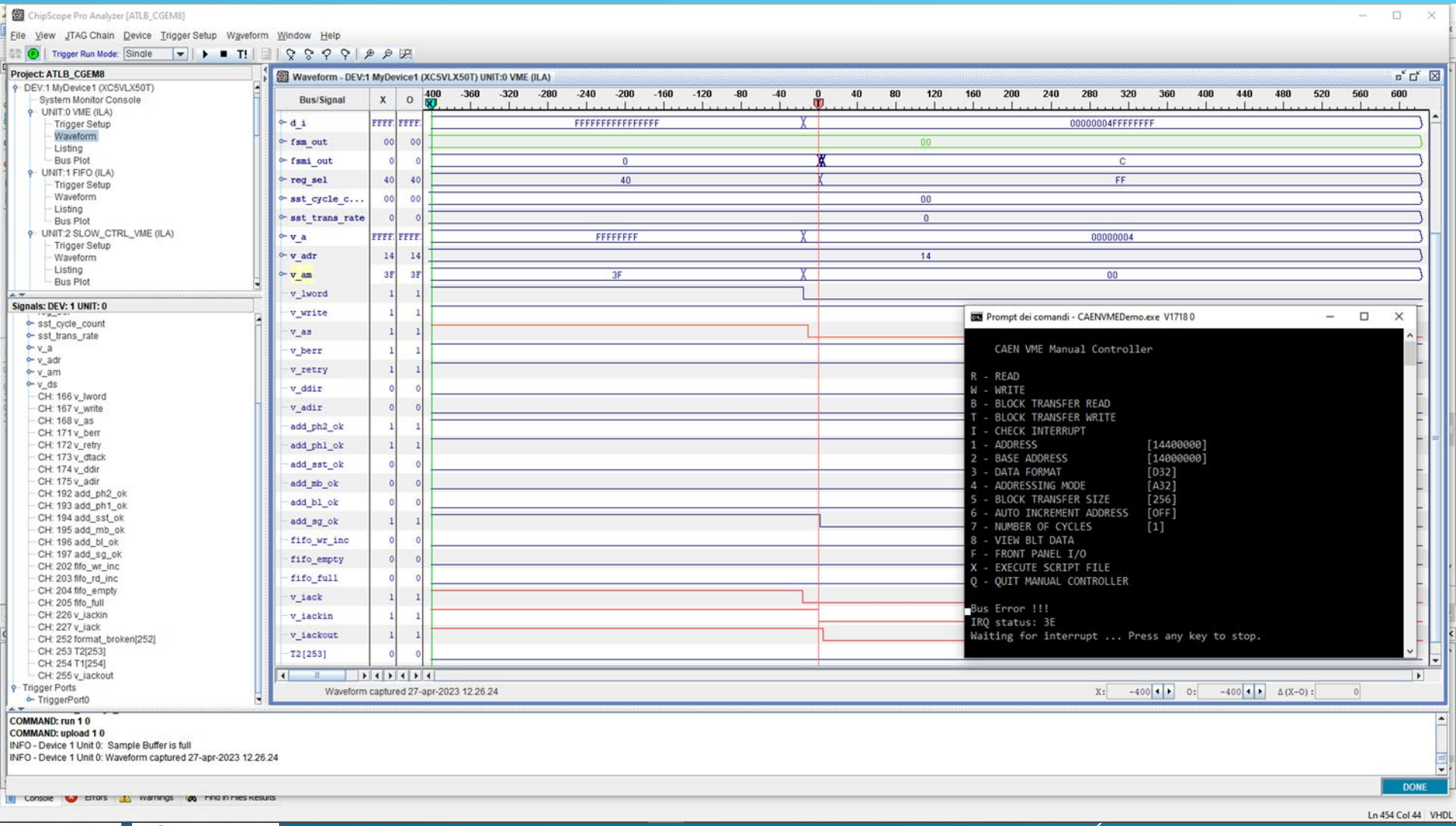
GEM-DC: Firmware upgrade description and status

The “ChipScope” must be setup by pointing to a specific project in the ATLB_CGEM hierarchy which associates meaningful label to the generic ID of the signals saved in the FPGA for the ChipScope capture.



GEM-DC: Firmware upgrade description and status

Unfortunately the "ChipScope" record shows that the firmware fails to respond properly to the IACK transaction → the firmware was then modified but not tested again. Further debugging could take place at IHEP (A.C.R. nov 2023)



GEM-DC: Hardware survey

GEM-DC modules at IHEP :

- 1 GEM-DC; it was left with the BES-III DAQ experts by Pawel during his business trip to IHEP in 2019

GEM-DC modules at INFN-FE:

- 1 GEM-DC sent by LNF
- 2 GEM-DC brought by Pawel during during his business trip to INFN-Ferrara in March 2023.

GEMROC integration in BES-III Slow/Run control/DAQ software

CGEM-IT Online Software architecture – BASELINE:

- TIGER Power Control and Detector Environmental Control (FEB_Vsupply, FEB_Isupply, FEB_Temp, GEMROC_Temp):
  - performed via Ethernet UDP by the CGEM-IT SLOW CONTROL software
- GEMROC T_{delay} scan, Threshold scan, diagnostic mode setup, DAQ_PAUSE etc.:
  - performed via Ethernet UDP by the CGEM-IT RUN CONTROL software
- CGEM-IT trigger matched readout: performed by CGEM-IT DAQ software via the GEM-DCs over VME bus

CGEM-IT Online Software development:

- **CGEM-IT SLOW / RUN CONTROL software development at BES-III:**
  - The development of the SLOW and RUN control software is being carried out by BES-III experts to some extent by porting the routines included in the omni-comprehensive GUFI framework written by Alberto Bortone.
  - Minor issues in the porting process have been flagged from time to time by BES-III experts and have been addressed and solved by Alberto.
  - Most substantial issue so far: some of the fields of the UDP packet exchanged between host PC and GEMROC modules to perform SLOW / RUN control functions could be modified by both the SLOW and the RUN control programs, leading to possible inconsistencies if the SLOW and the RUN control programs are independent processes, as in BES-III.\
    The solution proposed by Alberto Bortone was adopted because it requires minimal changes to the data format of the protocol (Ethernet UDP based) of communication between the GEMROC and the host PC and thus minimal changes to the SLOW/RUN control software routines.

GEMROC integration in BES-III Slow/Run control/DAQ software

- **CGEM-IT DAQ software development at BES-III:**

  The development of the CGEM-IT DAQ software should have been, in the original plans, the earliest to occur, because of being based on the VME readout of GEM-DC cards and because of:
  - the availability of the GEM-DC cards right from the start.
  - the possibility for the GEM-DC to generate dummy data formatted according to a format defined in collaboration with the BES-III DAQ experts and thus the potentiality to test unpacking routines and data integrity checks.

  The development of the DAQ software has started in 2019 and is proceeding now instead but being based on a solid VME architecture it should proceed fast.

  A GEM-DC module was tested in 2019 and data generated (by internal test pulse) by a GEMROC connected to the GEM-DC was readout.

  For this test the VME CPU had to poll the GEM-DC status register to know when the data was ready and then schedule the read. A VME IRQ-based readout mode is preferred instead.
- **Requirements to the GEM-DC firmware developer by the BES-III DAQ expert:**

  In a dedicated meeting with the BES-III DAQ experts (XiaoLu Ji, Ma Si, Tingxuan Zeng) recently organized on October 5th 2023 by Michela, the experts re-stated that:
  - **The GEM-DC shall generate a VME interrupt request (IRQ) when ready to be readout and handle the subsequent VME interrupt acknowledge (IACK) cycle** originated by the VME CPU. The request and its implementation have been discussed above.
  - **BES-III DAQ will read one event from the GEM-DC for every L1 TRIGGER** ⇒ it releases the requirements on the GEM-DC on-line memory because it is not required to buffer more than one event (an event in the GEM-DC is assembled by merging the Trigger matched event packets received from the connected GEMROCs).

GEMROC integration in BES-III Slow/Run control/DAQ software

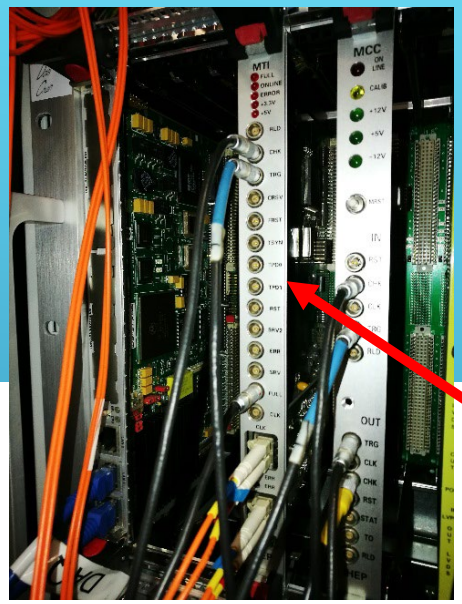
- **Requirements to the GEMROC firmware developer by the BES-III DAQ expert:**
  In the dedicated meeting with the BES-III DAQ experts above cited, the experts also reviewed:
  - The proposed approach to use the DAQ_PAUSE flag to put the CGEM-IT detector in a **"On-hold"** state after initial configuration by the RUN control software. Currently it is foreseen for the GEMROC modules to exit the **"On-hold"** state upon the first received L1Trigger (which also causes the generation of a "SOFT RESET within each GEMROC and to the connected TIGERs to reset the timing measurement units). This approach was favourably commented by the DAQ experts.
  - The handling of the Trig_Check signal by the GEMROC firmware. This analysis resulted in the following **REQUIREMENT:**
    - **IF** a mismatch of the distributed "L1_CHK" signal and the one internally calculated by the GEMROC (by counting the L1 triggers modulo 256) occurs **THEN** the GEMROC should set a "L1_CHK_ERROR" flag in all the following trigger matched output data packets to inform the online DAQ software about the mismatch condition.

CGEM-IT MODULAR FCS FANOUT: overview

The BES-III Fast Control (Timing/trigger) System:

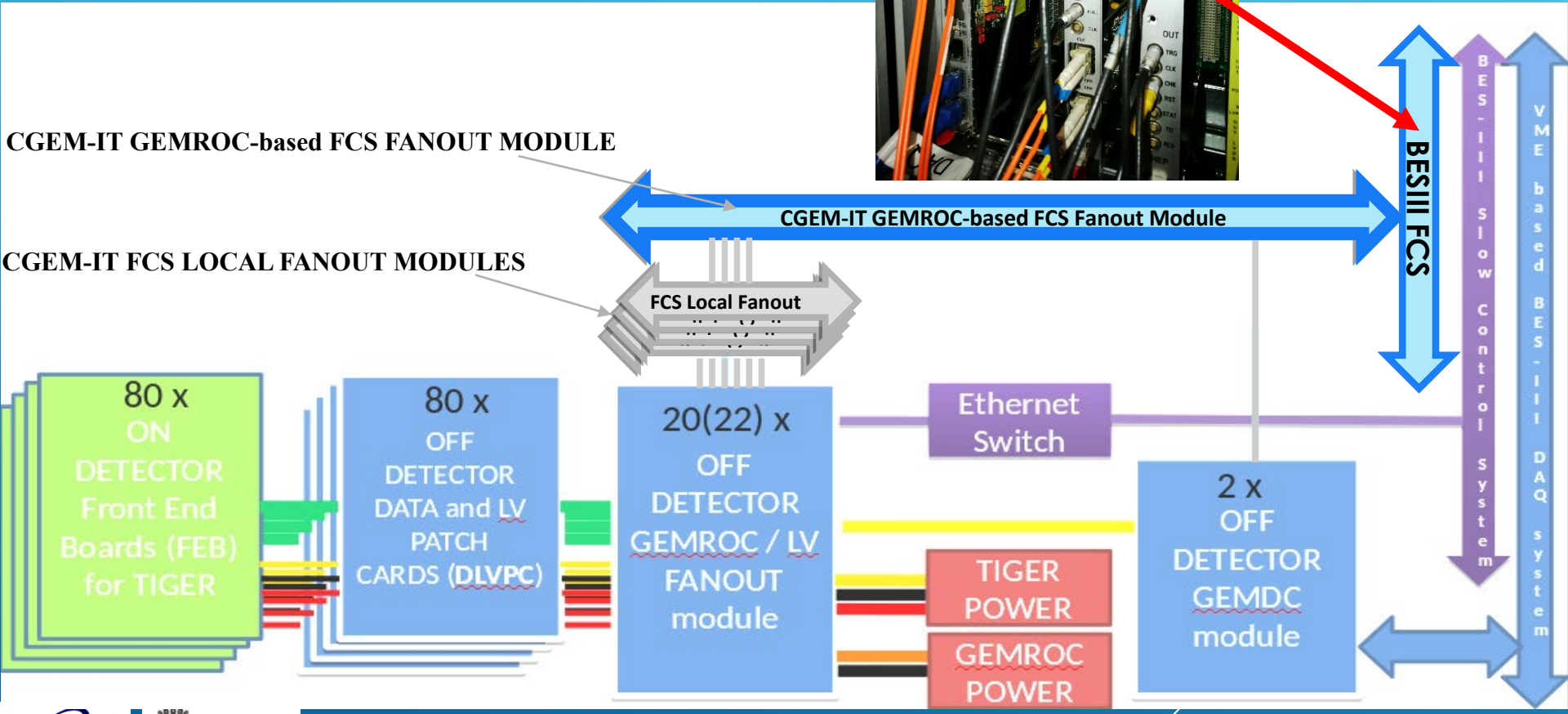
- **CLK, L1, L1_CHK are sourced by the BES-III FCS**
  - **signal level: pECL**
- **global FULL signal from the CGEM subdetector is sinked by the BES-III FCS**
  - **signal level: pECL**

The BES-III FCS is implemented by 9U VME "BES-III FCS Card" located in the experimental hall:



CGEM-IT GEMROC-based FCS FANOUT MODULE

CGEM-IT FCS LOCAL FANOUT MODULES

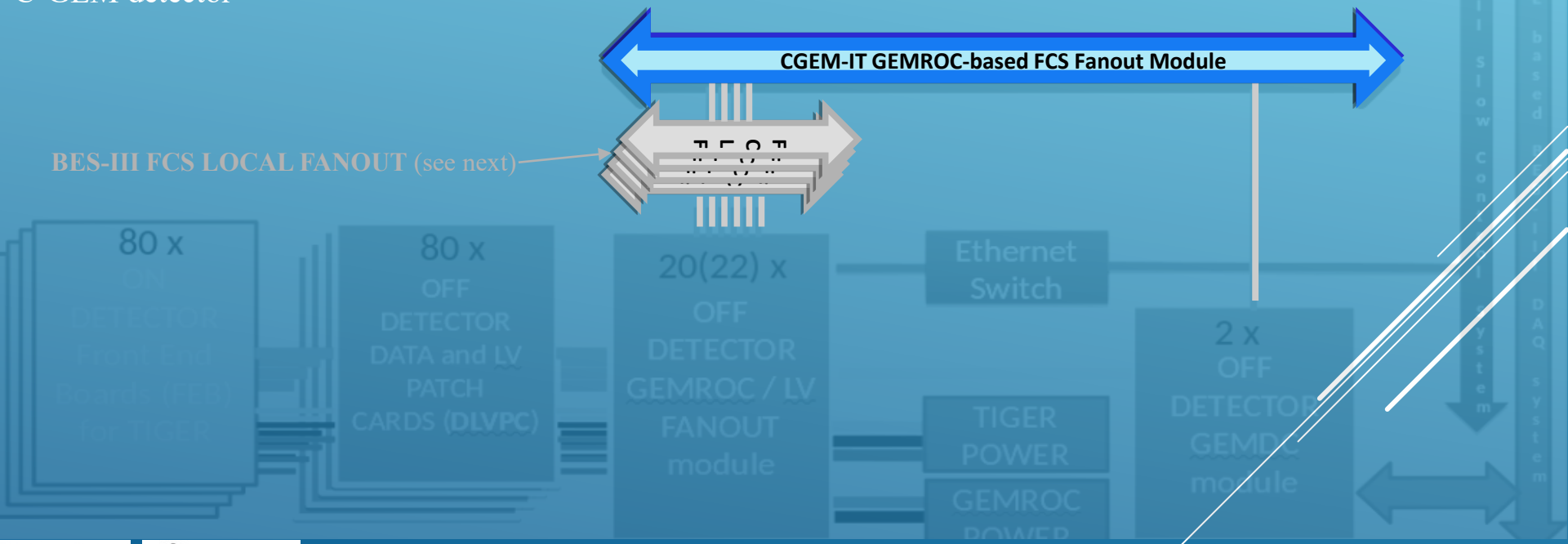


CGEM-IT GEMROC-based FCS INTERFACE MODULE

The CGEM-IT FCS INTERFACE MODULE is a modified GEMROC module which connects to the CLK, L1, L1_CHK, FULL signals from the BES-III Fast Control System.
It is made programmable to generate simulated Fast Control signals
The **CGEM-IT FCS INTERFACE MODULE** has:

- **4 FAN OUT ports for CLK, L1, L1_CHK (LVDS) TO the 4 groups of GEMROC installed around the BES-III detector** (North East, South East, North West, South West)
- 4 FAN IN ports for the FULL signals from each of the 4 groups of GEMROC installed around the BES-III detector
- 2 FAN OUT ports for CLK, L1, L1_CHK (NIM) TO the 2 GEM-DC
- 2 FAN IN ports for FULL (NIM) FROM the GEM-DC

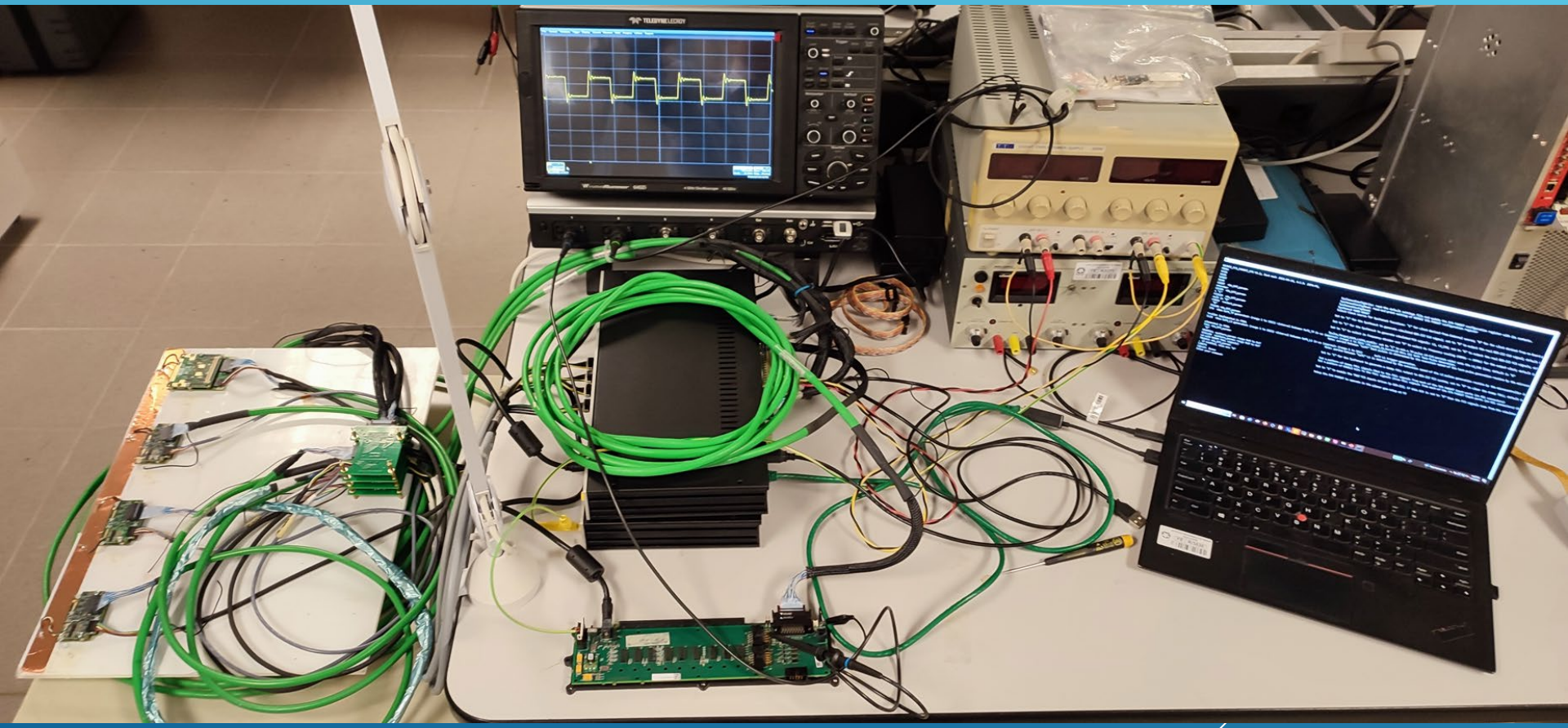
The FCF will be located at the top of the detector, close to the BES-III "BES-III FCS Card"assigned to the C-GEM detector



CGEM-IT FCS INTERFACE MODULE:Hardware

The CGEM-IT FCS INTERFACE MODULE is based on a GEMROC module.
Details on the preparation necessary are given in the file:
"Preparaz_moduli_GEMROC_con_IFC_CARD_v4d3_LINK_FCSFanout_2021_v2.docx" available at:
https://pandora.infn.it/ws-tiger-gemroc-documentation/GEMROC_AND_OTHERS/GEMROC_FCS_FANOUT_MASTER

Below a picture of the setup at INFN Ferrara (A.C.R. nov 2023) to test the Local FCS FANOUT modules.



CGEM-IT FCS INTERFACE MODULE:Firmware and Python scripts

The CGEM-IT FCS INTERFACE MODULE is controlled by the exchange of UDP packets from a host PC. The packet protocol and the Python scripts to control the to emulate the CGEM-IT FCS INTERFACE MODULE are available at the repository shown in the next slide.

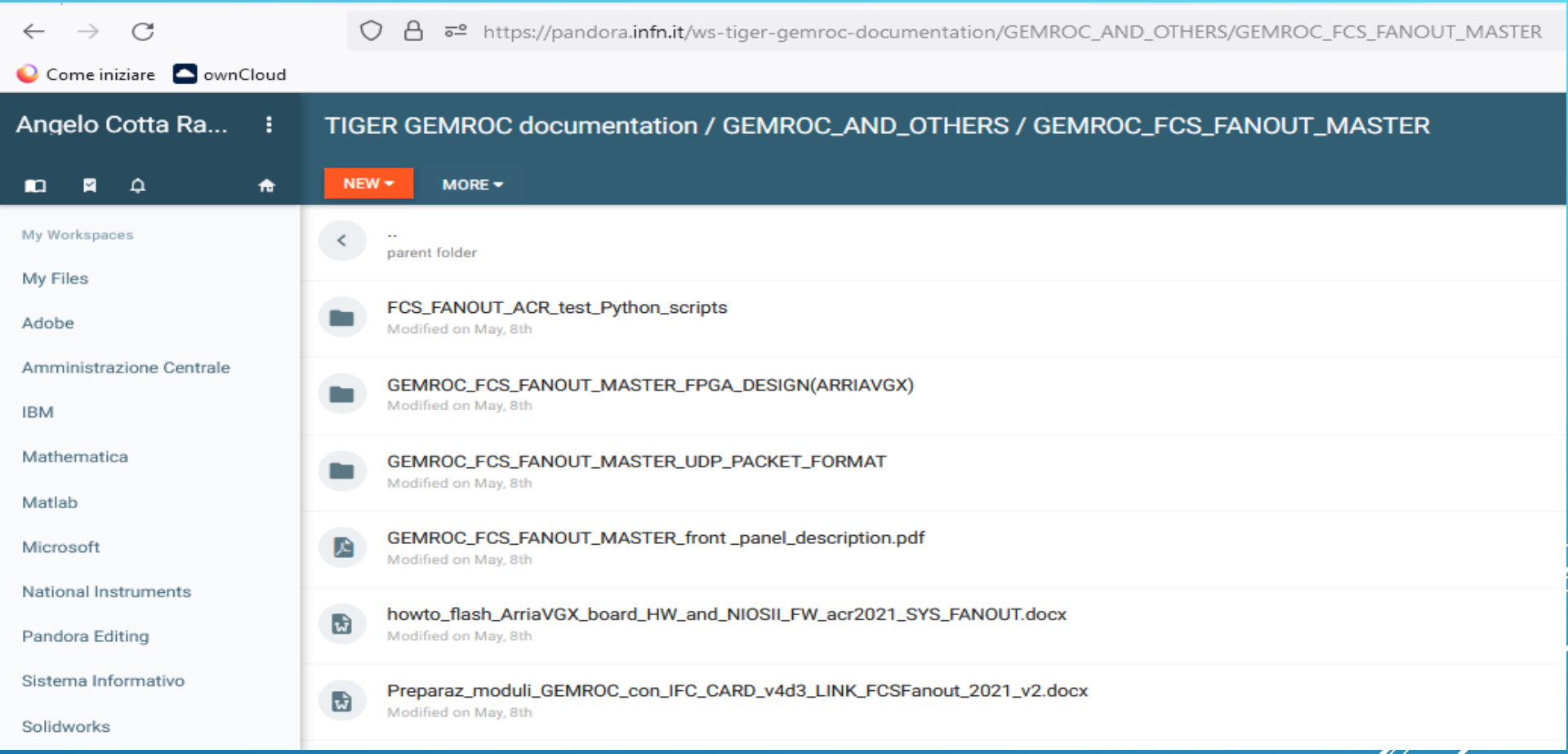
```
Command Prompt - python  FCS_FANOUT_UI_2021.py 7 0xf

C:\angelo\BES_III\FCS_FANOUT_UI>python FCS_FANOUT_UI_2021.py 7 0xf

GEMROC_FCS_FANOUT_CFG V1.1; last mod: 2021-04-14, A.C.R. INFN-FE;
MENU:
SFCW                                                    SysFanoutConfigWrite: read the default settings file and update the SYS FANOUT configuration register with its contents.
SFCR                                                    SysFanoutConfigRead: read and print setting of GEMROC SYS FANOUT configuration register
SFRST                                                   SysFanoutConfigReset
SFHR                                                    SysFanout HARD RESET
CKEXT  <On_Off_param>                                   Select Clock source for SysFanout functions: "1" for clock derived from External source; "0" for for clock derived from on-board g
enerator
CKSIM  <On_Off_param>                                   Set to "1" for the SysFanout to generate simulated BES-III CLK signal; set to "0" to output the real BES-III CLK signal; default i
s "1"
FCSSIM  <On_Off_param>                                  Set to "1" for the SysFanout to generate simulated FCS signals: L1, L1_CHK; set to "0" to output the real BES-III FCS signals; def
ault is "0"
CKDIV  <select_param>                                   Set to "1" to select 1x frequency divider and "0" to select 4x frequency scaling (40MHz -> 10MHz) for the output clock; default is
 "0"
TP2CHK <On_Off_param>                                   Tpulse_Merged_With_L1Chk_enable: set to "1" to mix a TP pulse (4 CLK periods wide) onto the L1_CHK line; default is "0"
STG  <Num Soft_TP generated> (range 1 to 1023) <Interval between Soft_TP in us (approx)> (range 1 to 511) <TP_width_in_burst>(0 thru 15) Soft Test Pulse Generation.
                                                         Note: period between "soft" test pulses is determined by the execution speed of the test pulse generation routine by the microcon
troller implemented in FPGA
SL1G  <Num Soft_L1 generated> (range 1 to 1023) <Interval between Soft_L1 in us (approx)> (range 1 to 511)       Soft L1 trigger generation.
                                                         Note: period between "soft" L1 is determined by the execution speed of the L1 pulses generation routine by the microcontroller im
plemented in FPGA
FULL <On_Off_param>                                     Set to "1" for the SysFanout to generate a dummy FULL output to BES-III FCS system; set to "0" to clear the dummy FULL; default is
 "0"
SDUMFULL <pattern_param> range 0x0 to 0xf               Set a pattern of dummy FULL signals ORed to the FULL signals from each of the SYS FANOUT input ports (on KEL connectors)
SFULLEN  <pattern_param> range 0x0 to 0xf               Set a pattern of ENABLE bits fo the FULL signals (true FULL signals from each of the SYS FANOUT input ports (on KEL connectors) OR
ed with DUMMY FULL signals)
TRUEFCS <On_Off_param>                                  Set to "1" to enable the TRUE FCS inputs driven by BES-III; if this bit is set to "0" then the FCS signals come from the simulator
, if enabled, else are "0"
LABCFG                                                  Setup the SYS FANOUT to operate in the planar gem setup at FE
(Q)uit: leave
Enter your command:
```

CGEM-IT FCS INTERFACE MODULE: Firmware and Python scripts

The CGEM-IT FCS INTERFACE MODULE firmware, UDP packet definition and Python scripts are shared here:



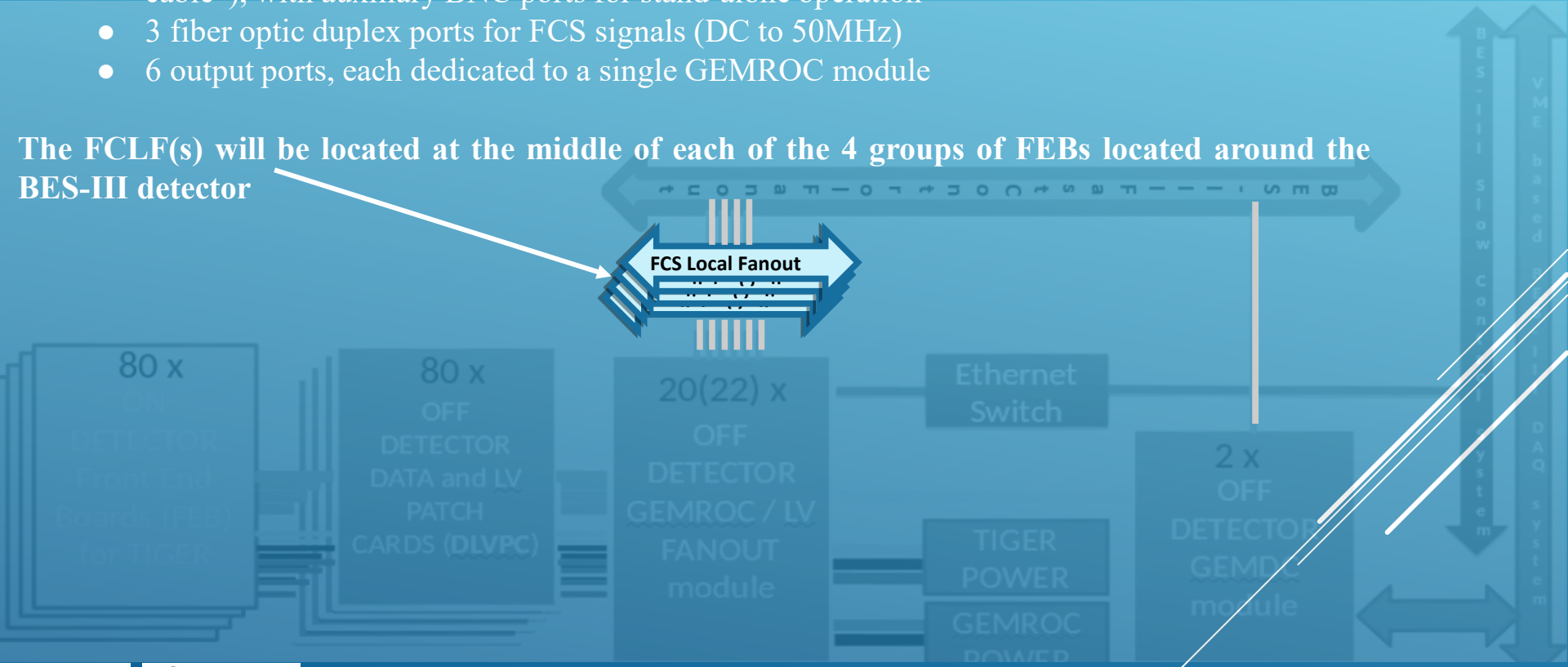
MODULAR FCS LOCAL FANOUT

The FCS LOCAL Fanout (FCLF) are a LOW COST, non programmable, fanout modules which connects to the CLK, L1, L1_CHK, FULL ports of the CGEM-IT FCS INTERFACE MODULE.

Four (+ spares) FCLF are needed
The FCLF will have:

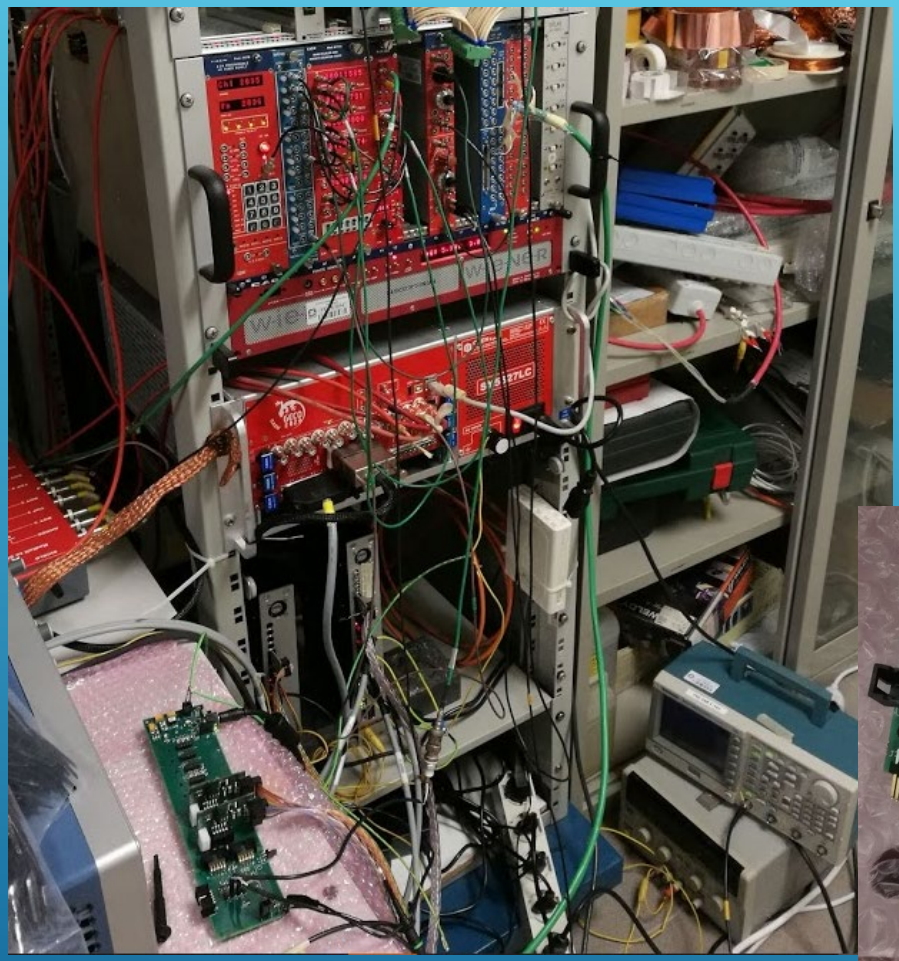
- 2 alternatives for the connection to the CGEM-IT FCS INTERFACE MODULE:
  - 1 "copper" port for LVDS signals carried by a 17- twisted pair, shielded cable ("green cable"), with auxiliary BNC ports for stand-alone operation
  - 3 fiber optic duplex ports for FCS signals (DC to 50MHz)
  - 6 output ports, each dedicated to a single GEMROC module

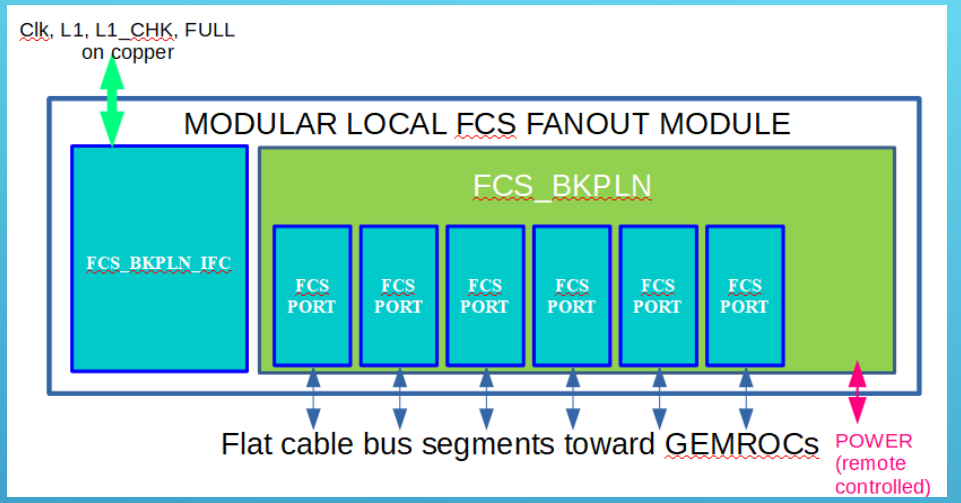
The FCLF(s) will be located at the middle of each of the 4 groups of FEBs located around the BES-III detector

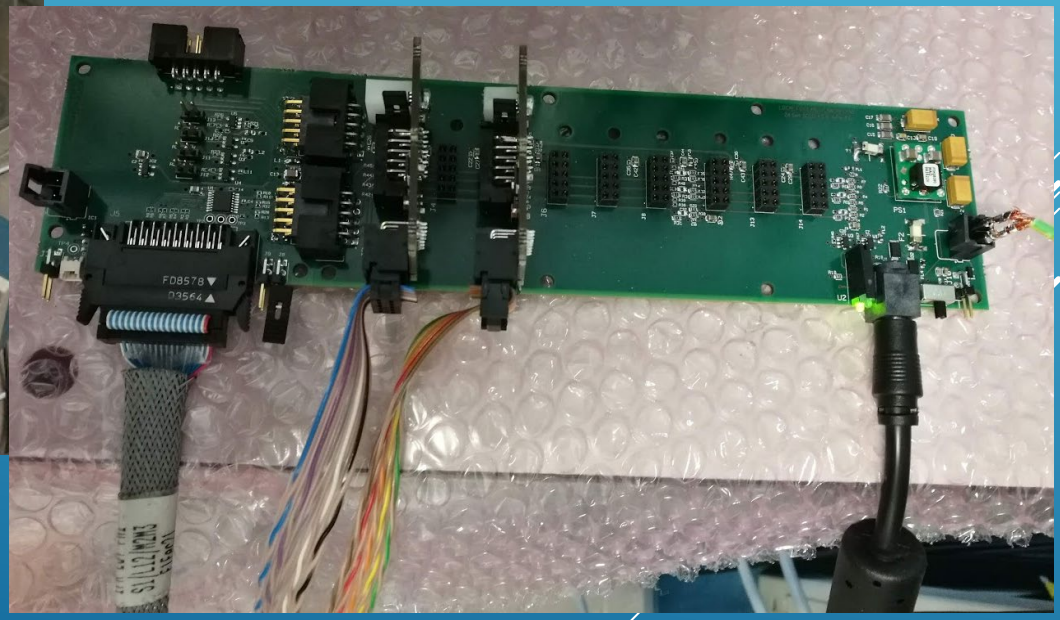


MODULAR FCS LOCAL FANOUT

Modular FCS Local FANOUT applied to the planar GEM setup at INFN-Ferrara:

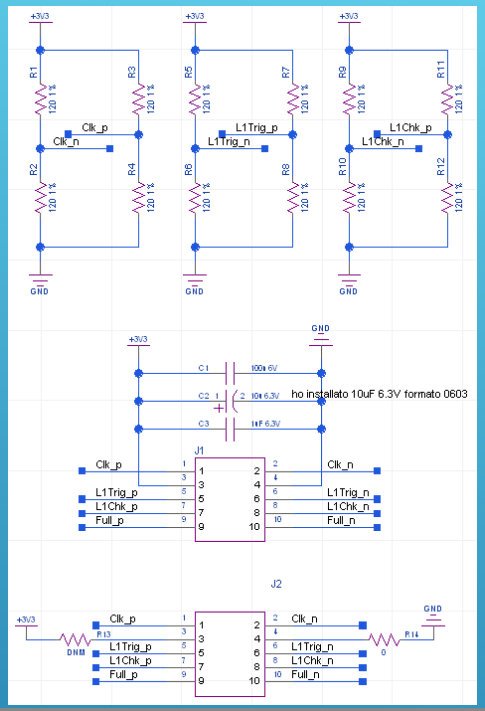


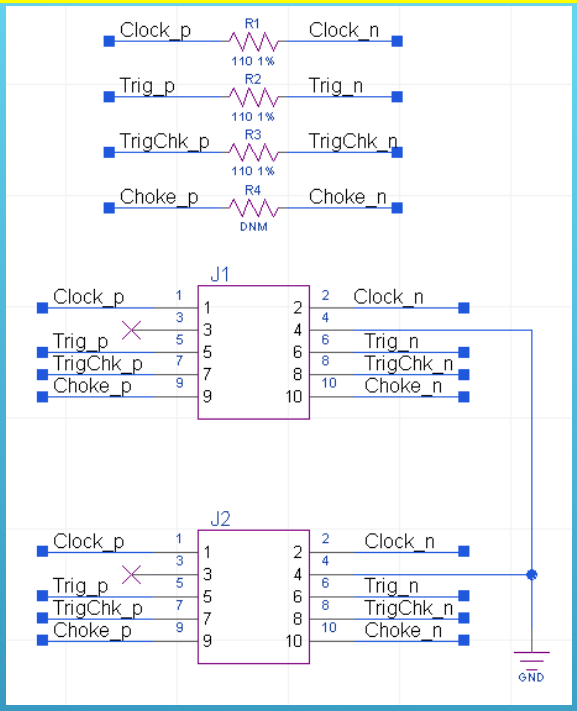


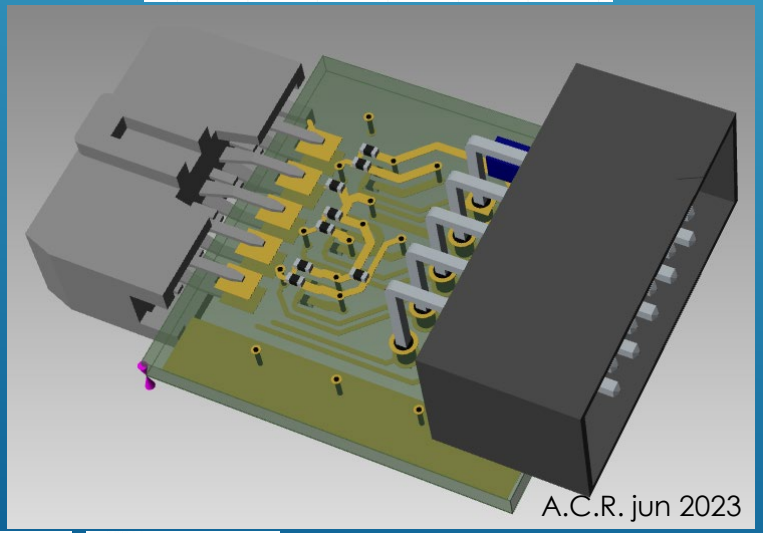


The local modular fanout is used to provide FCS signals (clock and trigger) to the 2 GEMROC modules used in the setup

MODULAR FCS LOCAL FANOUT: FCS termination card







OUTLOOK:

Looking forward to the integration week at IHEP in which the following goals would be pursued (subject to shared considerations on priority):

- upgrade of GEMROC Modules with the latest GEMROC_IFC card patches
- deployment of an upgraded GEMROC-based FCS INTERFACE MODULE FCS fanout
- deployment of 4 FCS LOCAL FANOUT MODULES
- commissioning of all the above at the CGEM-IT detector
- optimization of the CGEM-IT grounding and shielding layout
- debug of the GEM-DC module IRQ/IACK acknowledge functions in collaboration with the BES-III DAQ software experts

BACKUP slides

- **development of the modular Fast Control Signals (FCS) FANOUT system**

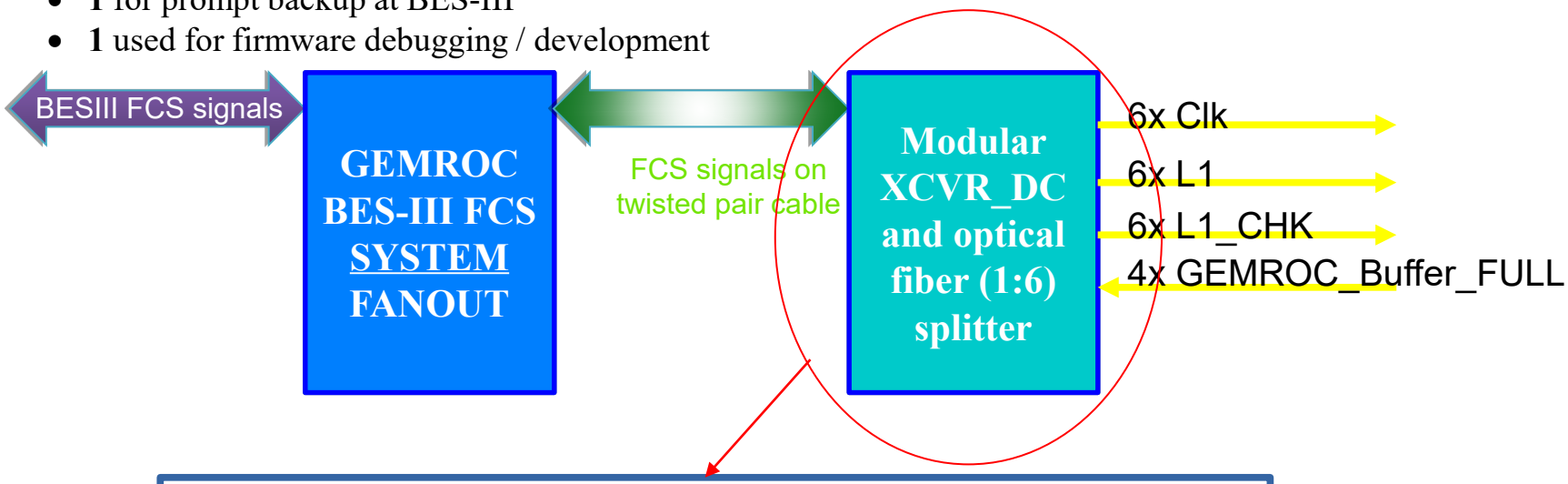
GEMROC-based FCS SYSTEM FANOUT

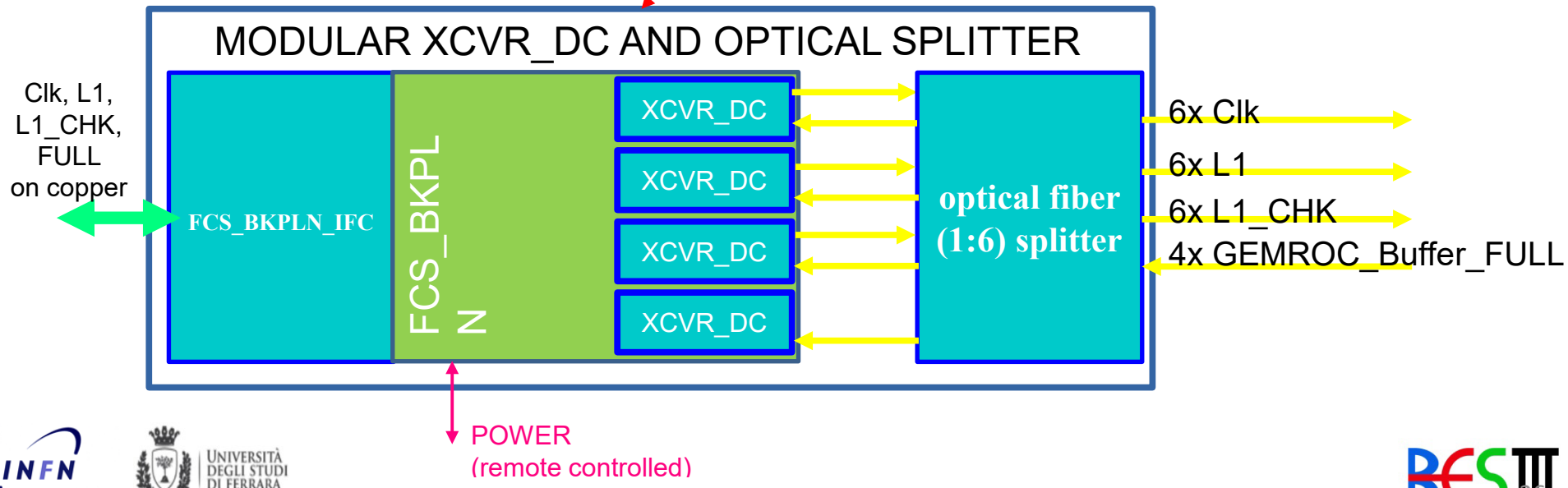
QUANTITY NEEDED:

- **3** pieces of **BES-III FCS SYSTEM Fanout**:
  - **1** in operation at BES-III
  - **1** for prompt backup at BES-III
  - **1** used for firmware debugging / development

Status:

FCS_BKPLN and XCVR delivered





- **development of the modular Fast Control Signals (FCS) FANOUT system**

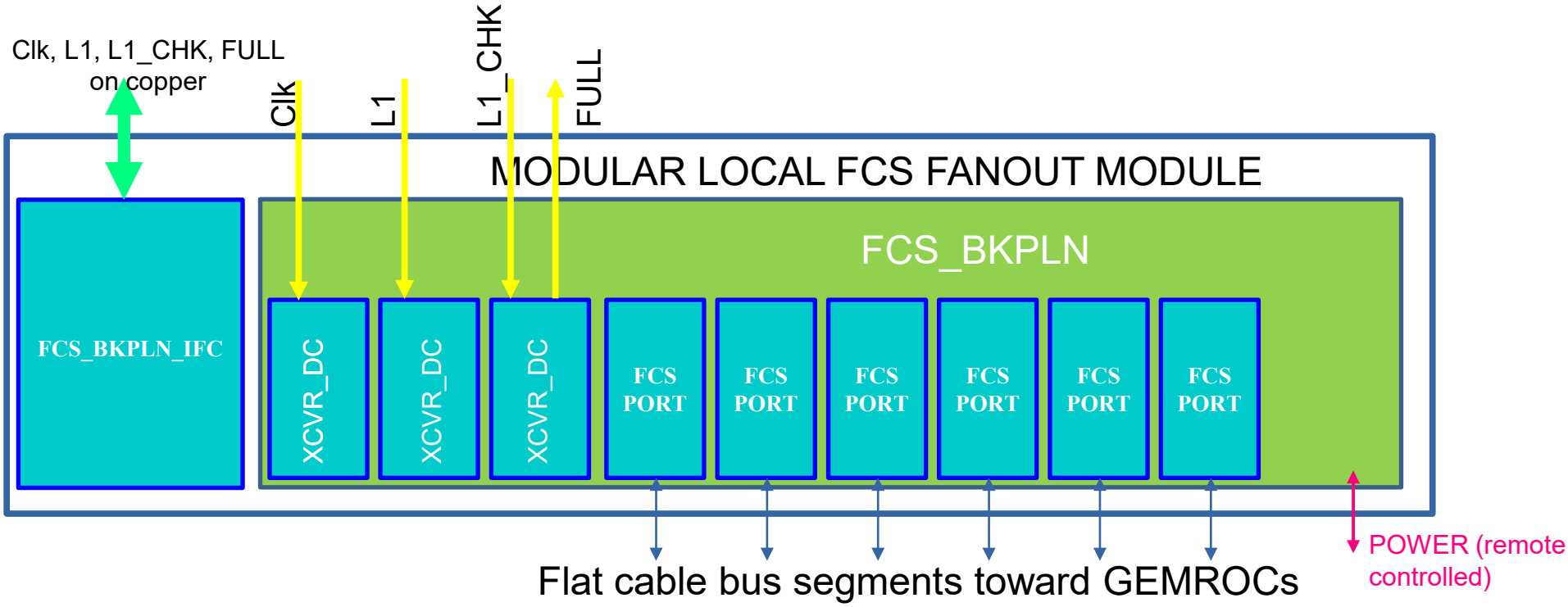
Modular FCS Local FANOUT

QUANTITY NEEDED:

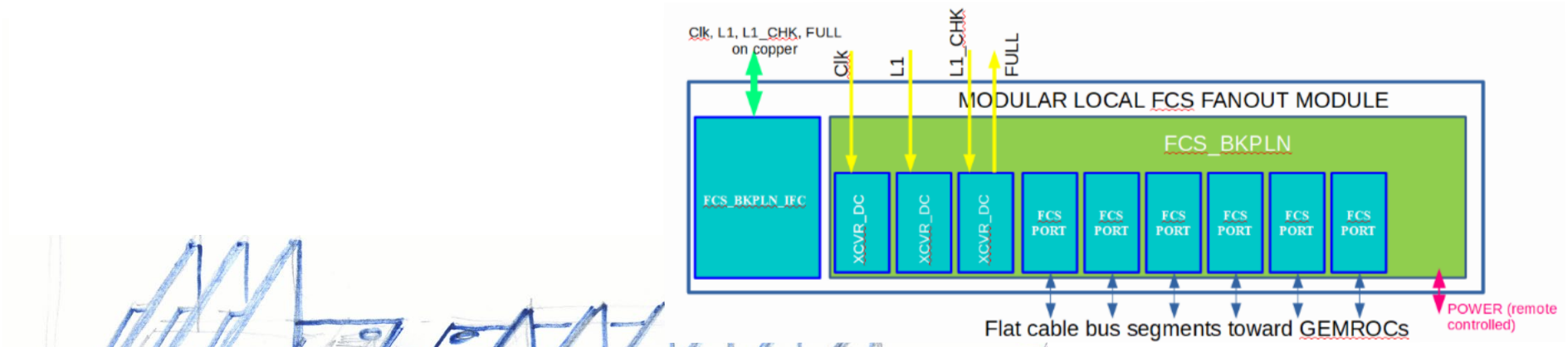
- 6 pieces:
  - **4** in operation at BES-III
  - **1** for prompt backup at BES-III
  - **1** used for firmware debugging / development

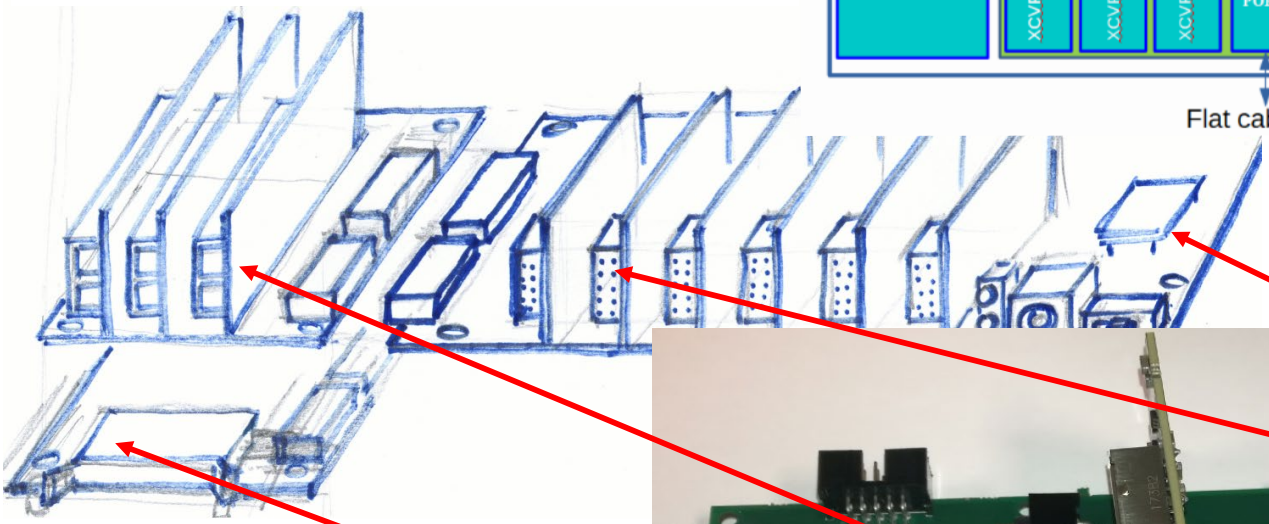
Status:

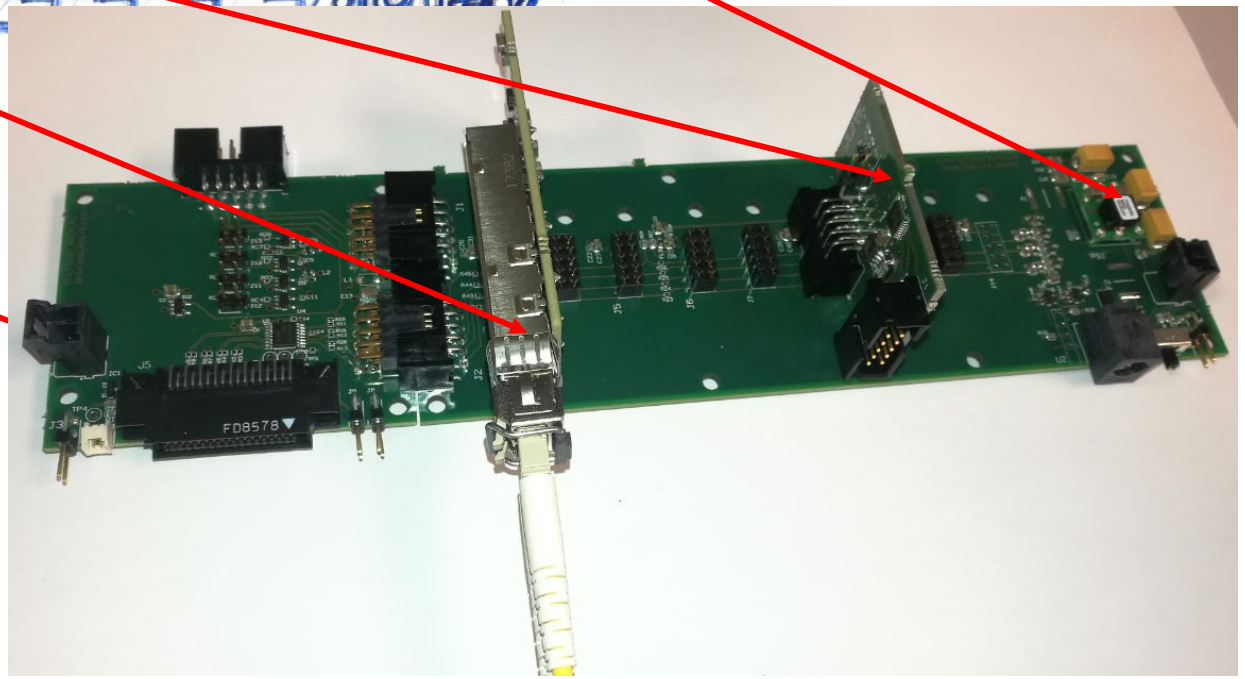
FCS_BKPLN_IFC,
FCS_BKPLN,
FCS_PORT,
and XCVR delivered



- **development of the modular Fast Control Signals (FCS) FANOUT system**







All elements of the modular FCS FANOUT system have been manufactured and are being assembled and tested.