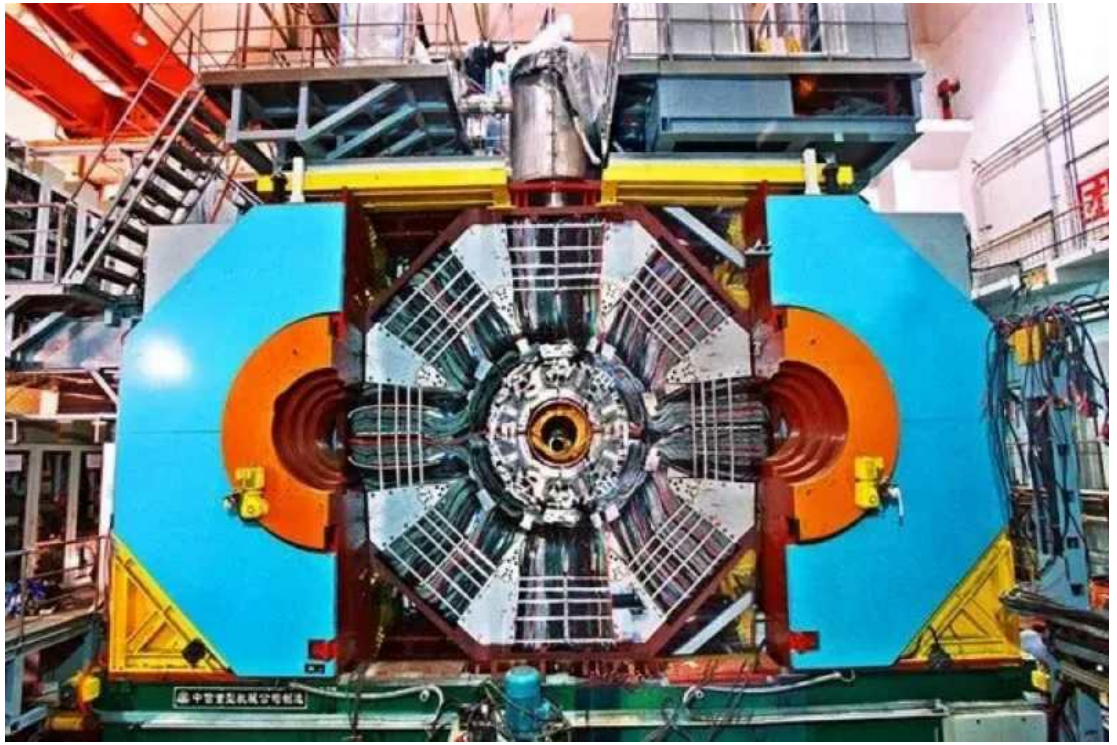
CGEM-INTEGRATION

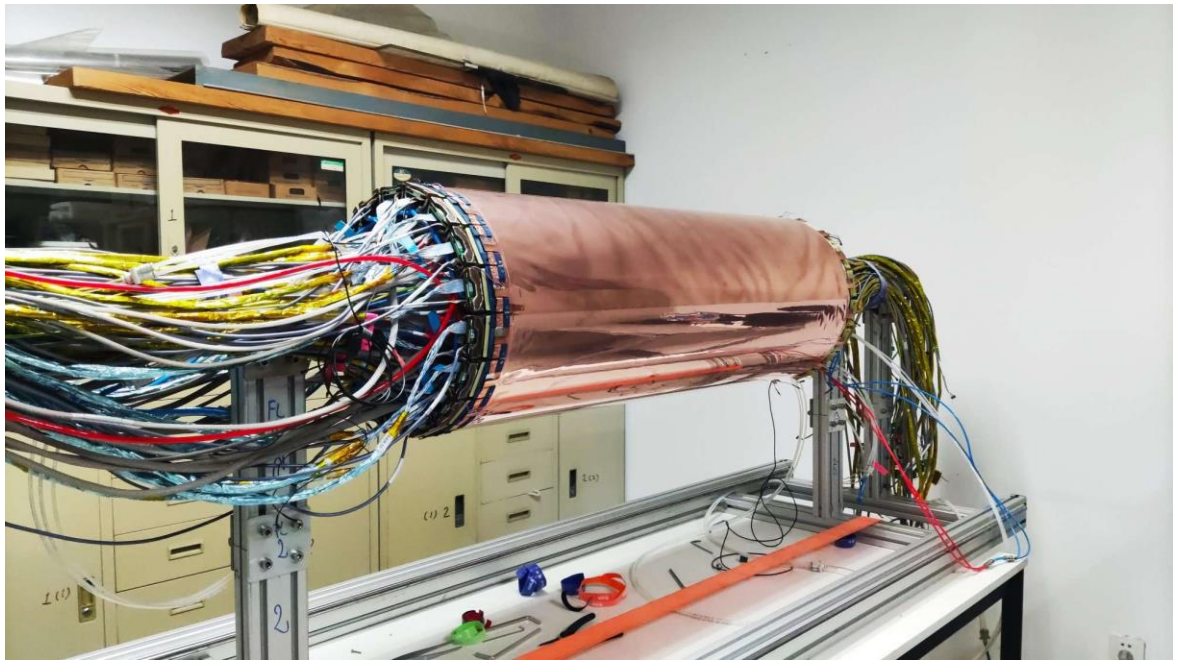
MGRECO on behalf of CGEM-IT working group

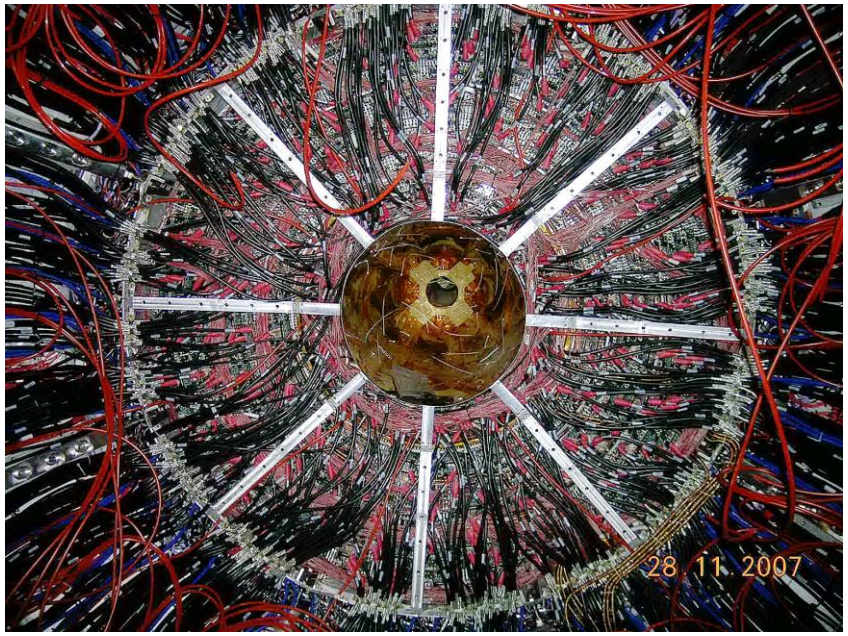
OUTLINE

1. CGEM/BESIII
2. CGEM frontend electronics
3. CGEM readout
4. CGEM readout/BESIII DAQ
5. CGEM/BESIII Slow Control

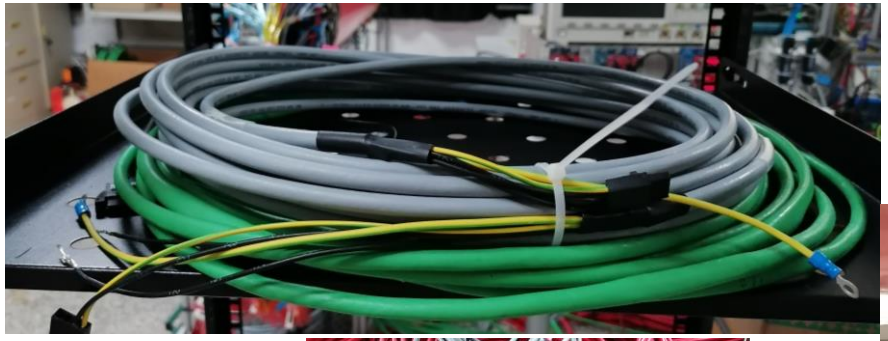
CGEM/BESIII

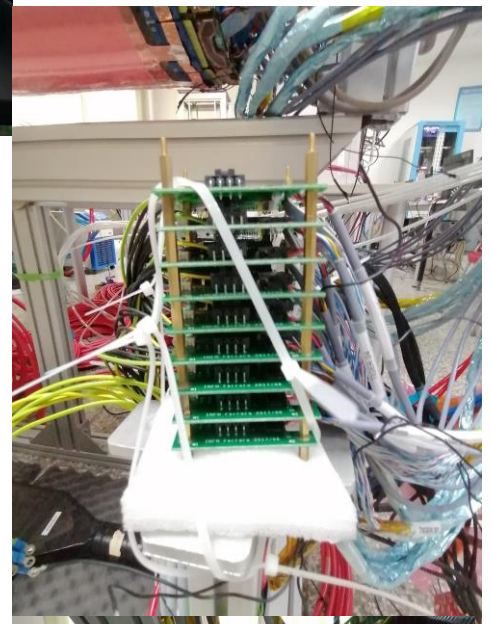






CGEM/BESIII





INTEGRATION issues for electronics

Placement of HV-LV-ROC Power Supply mainframes
Placement of GEM ROC modules
Cable Routing

Information exchange with Mingyi Dong in July

M. Greco, CGEM workshop,
15 September 2017

BESIII CGEM-IT

ROC+LV/HV PS

GEM ROC PS
on the cabinet (N)

GEM ROC PS & LV PS
on the cable trays (S)

HV PS on the
platform

M. Greco, CGEM workshop, September 2017 CGEM-IT

ROC+PS

On site survey with Angelo Cotta Ramusino

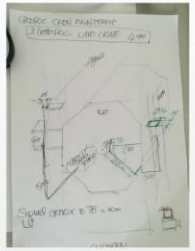
ph@ A. C. Ramusino

GEM ROCs
In frames on the gray columns
On E/W/N/S

GEM ROC stand alone modules: 334 mmx176mmx44mm

M. Greco, CGEM workshop, September 2017 CGEM-IT

ROUTING

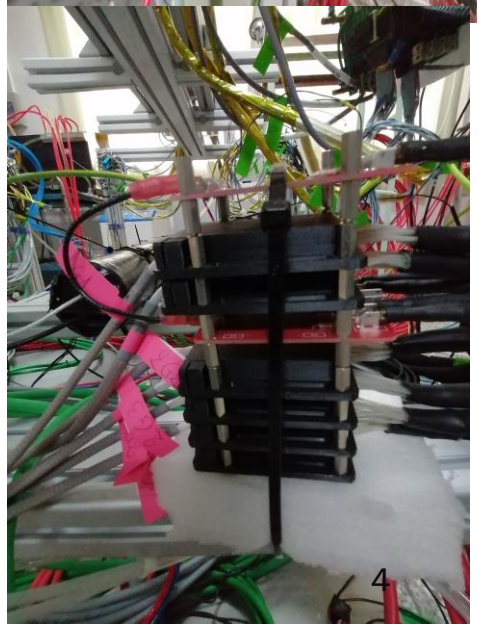


A. C. Ramusino

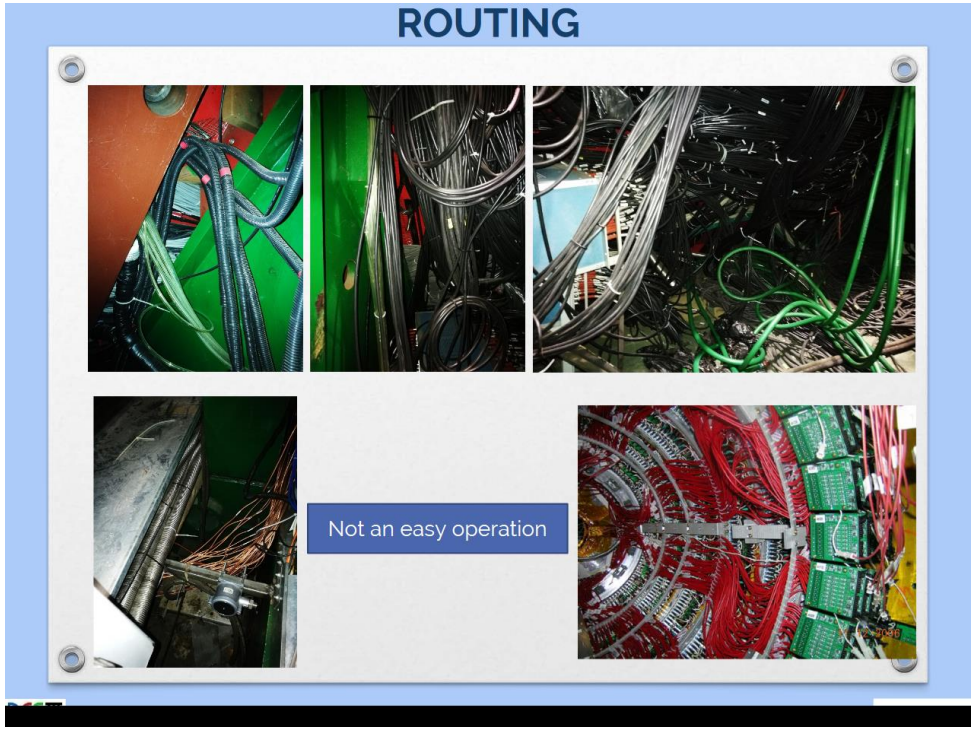
Signal cable length from LV-DATA
TB to GEM ROC modules about 10 m

Cable length from GEM ROC to
GEM ROC PS about 4 m (N)
about 5 m (S)

Cable length from GEM ROC to LV PS
about 10 m (N)
about 5 m (S)

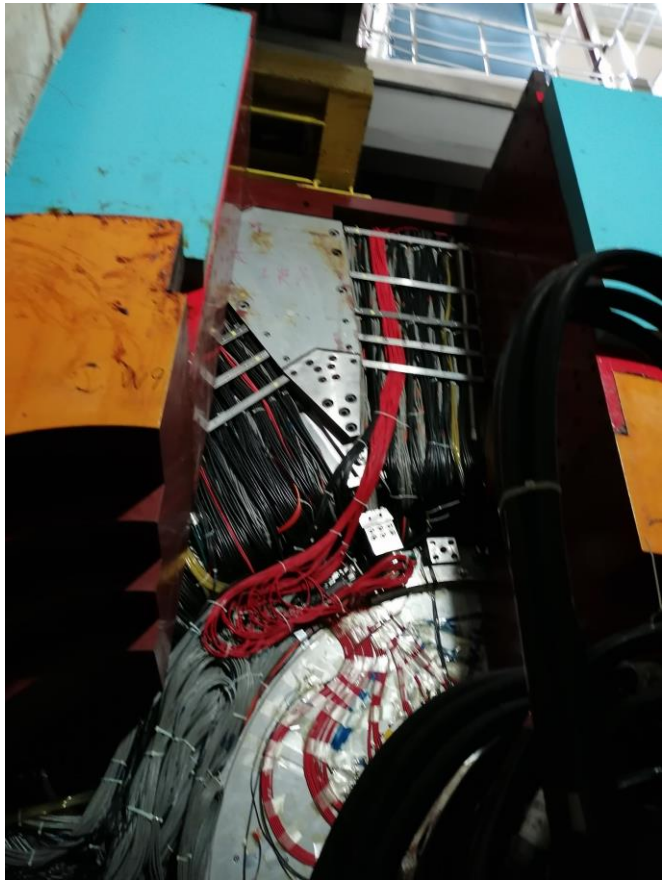


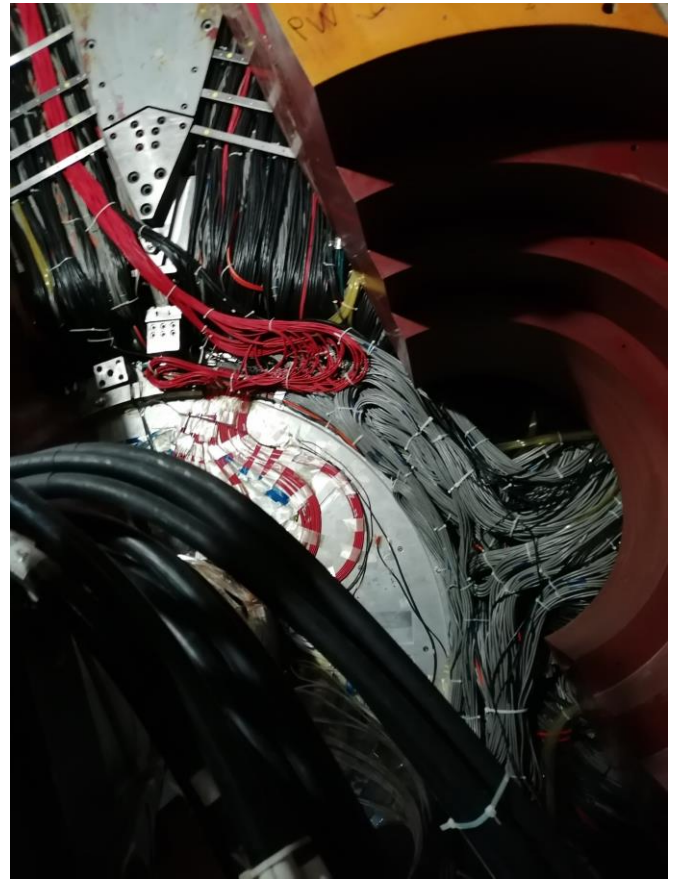
CGEM/BESIII

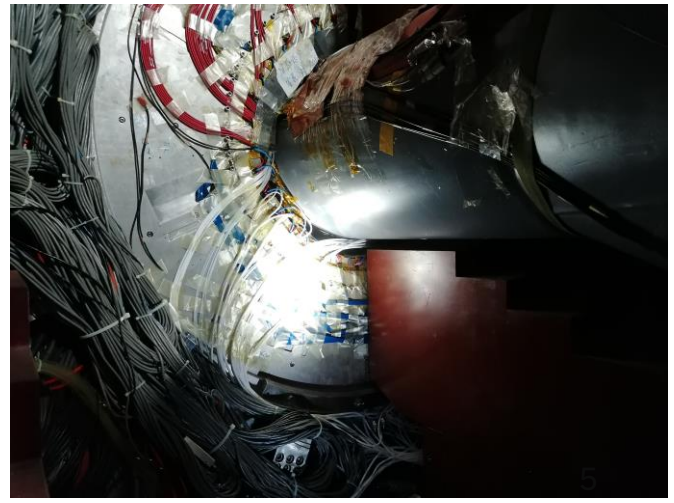


2017/2023

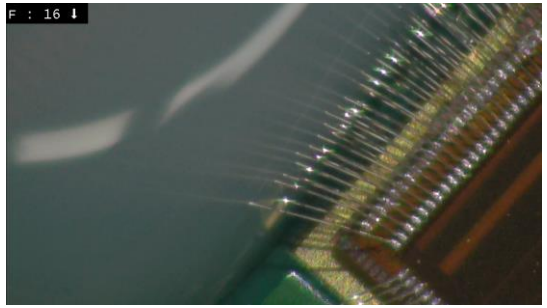
not an easy operation







CGEM FRONT-END ELECTRONICS



TIGER

All chips have been encapsulated. Few losses.
Monitoring since July

Further FEB spares: order ongoing

CGEM READOUT ELECTRONICS: GEMROC

22 GEMROC needed

>> talk by Angelo

16 already used for L1/L2/half L3;

21 available at Beijing +1 «malfunctioning» @Beijing

2 already mounted by ACR(to be sent with GG &Riccardo)

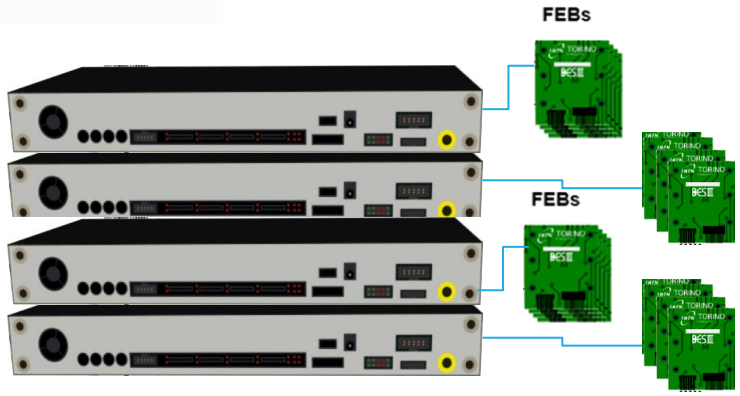
-Spares:
4 to be mounted by ACR (or mounted in the meanwhile)
1 sent to Ferrara

>> talk by Ilaria Neri

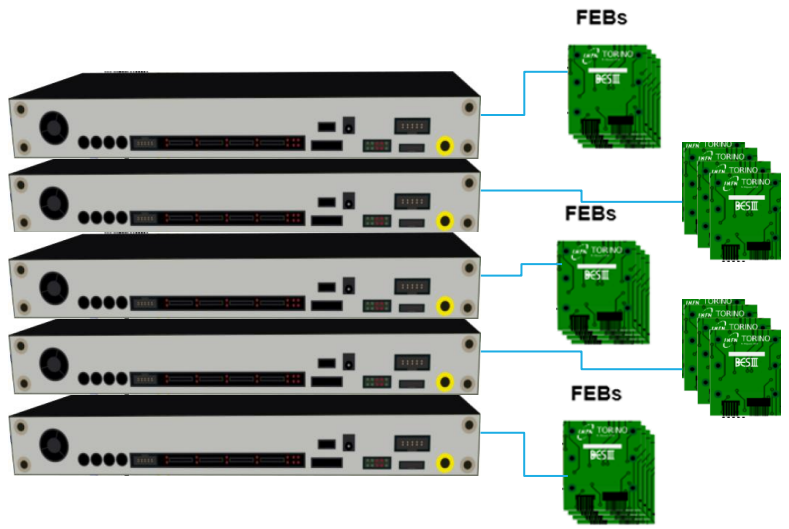
Further developments

GEMROC

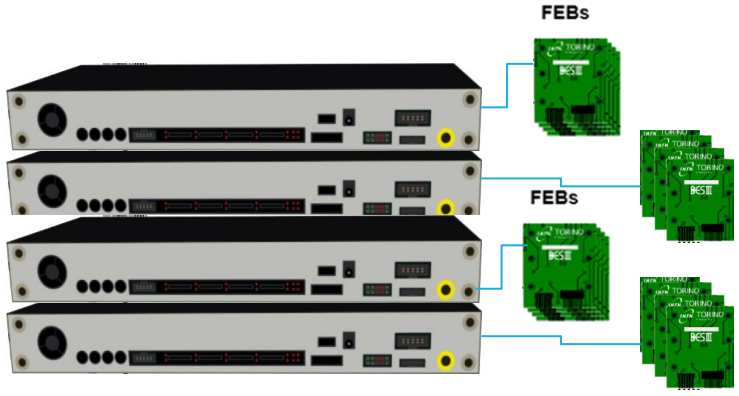
Layer 1

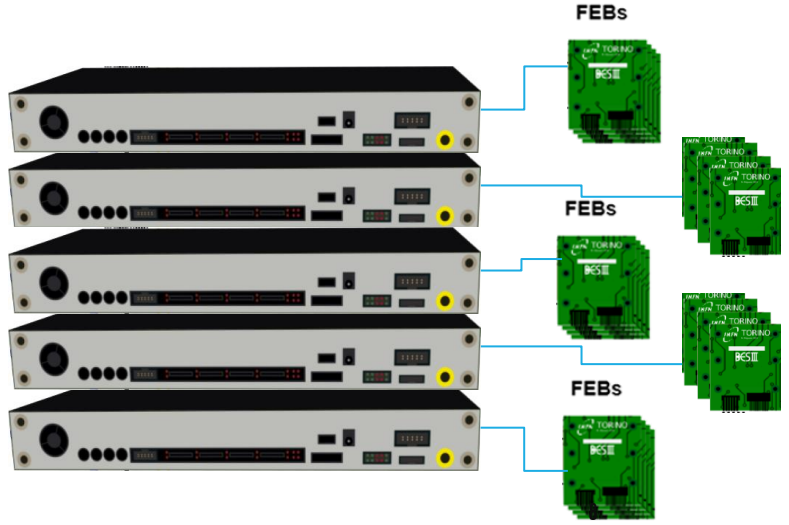


Layer 2



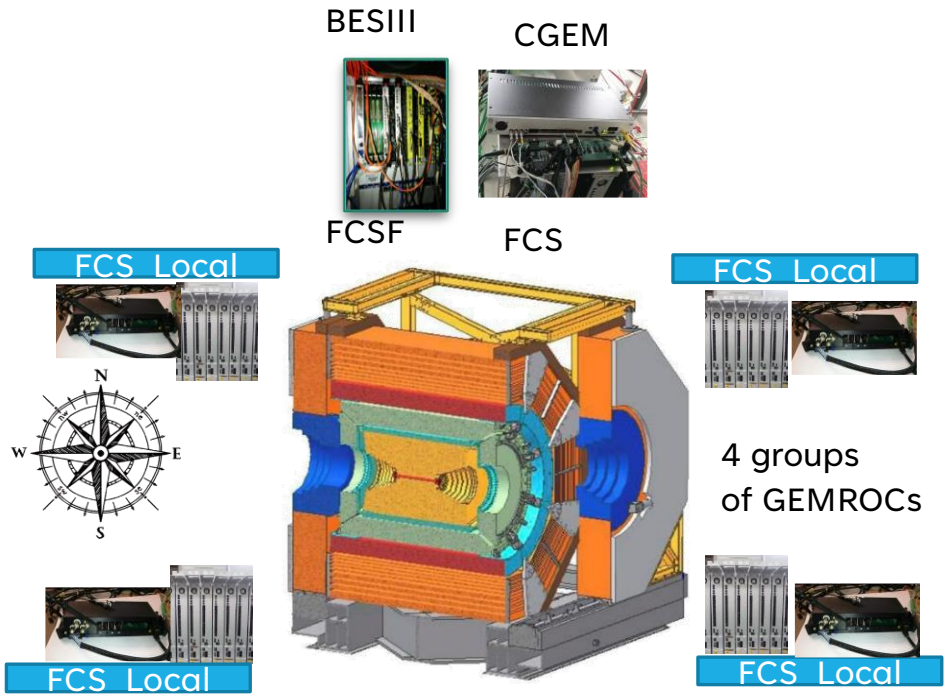
Layer 3





CGEM READOUT ELECTRONICS: FANOUT

FCS: a modified GEMROC module which connects to the CLK, L1, L1_CHK, FULL signals
from the BESIII Fast Control System Fanout



FCS_Local, fanout modules which connects to the CLK, L1, L1_CHK, FULL signals from FCS

>> talk by Angelo

FCS_Local
FCS backplane: 5 available (4 needed)
FCS Flat Cable Ports: 5 available (4 needed)
FCS backplane interface: under check ->checked
FCS terminator: layout refined, under production

Modules will be mounted with the help of Nicholas

READOUT ELECTRONICS: GEMROC<>GEMDC

>> talk by Angelo

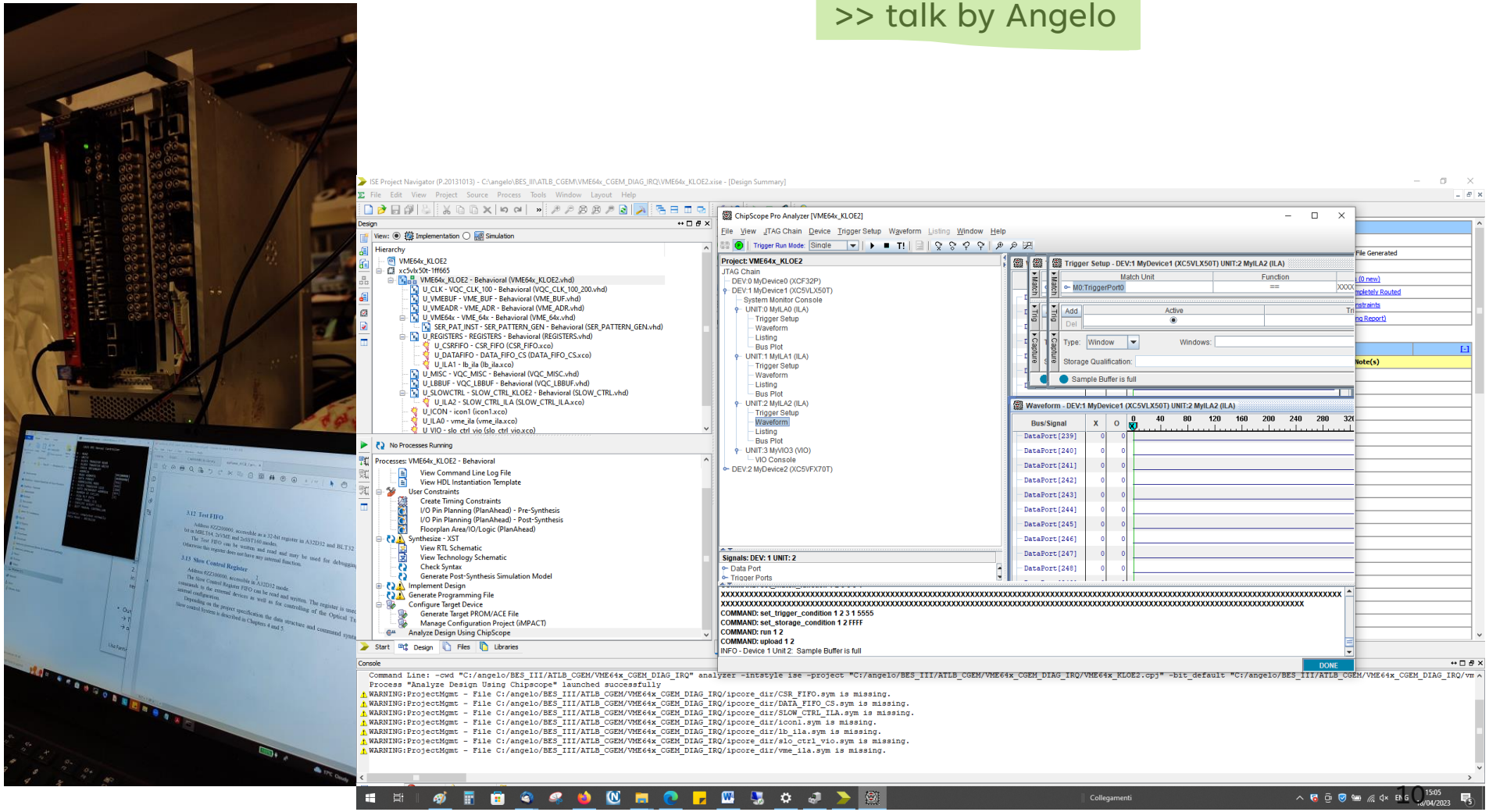
GEM DC from LNF

Pawel @ Fe

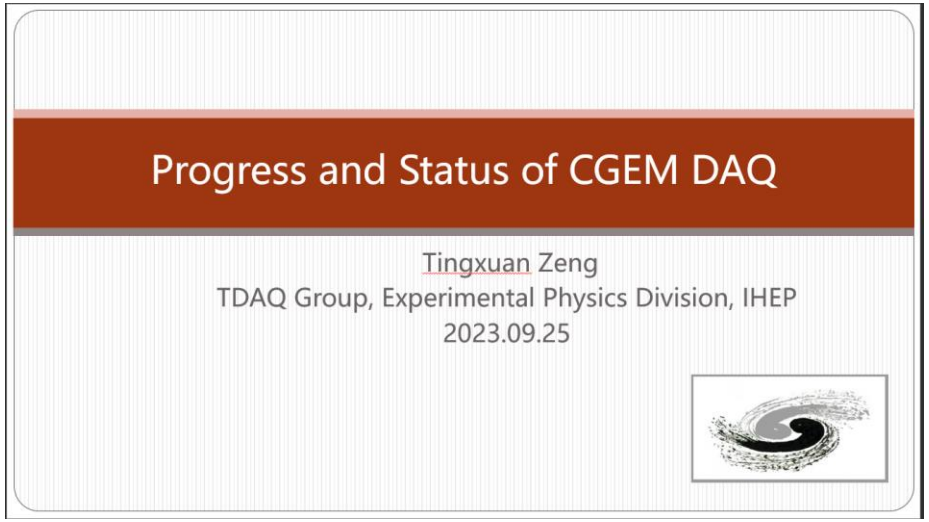
End of March/April

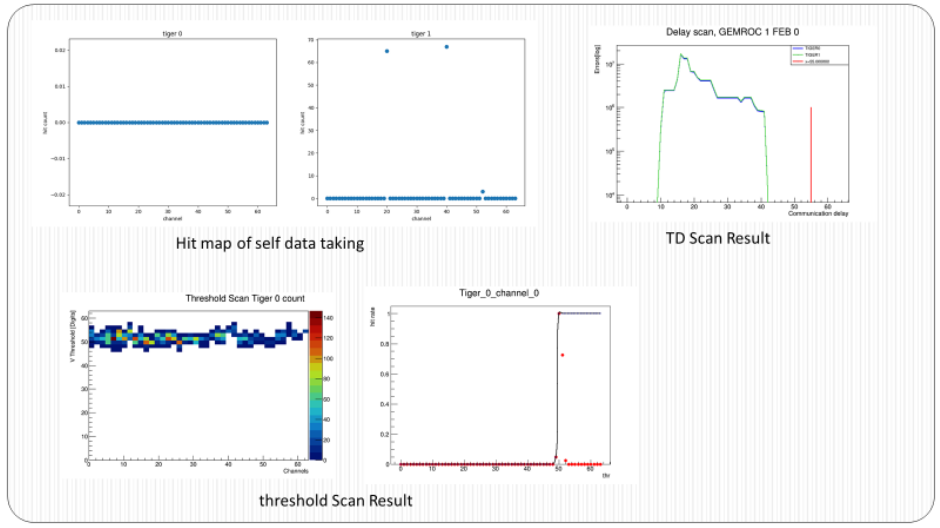
Debugging by

Angelo



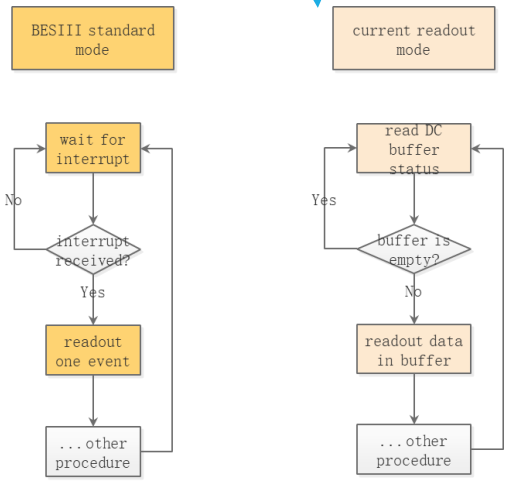
CGEM READOUT/ BESIII DAQ





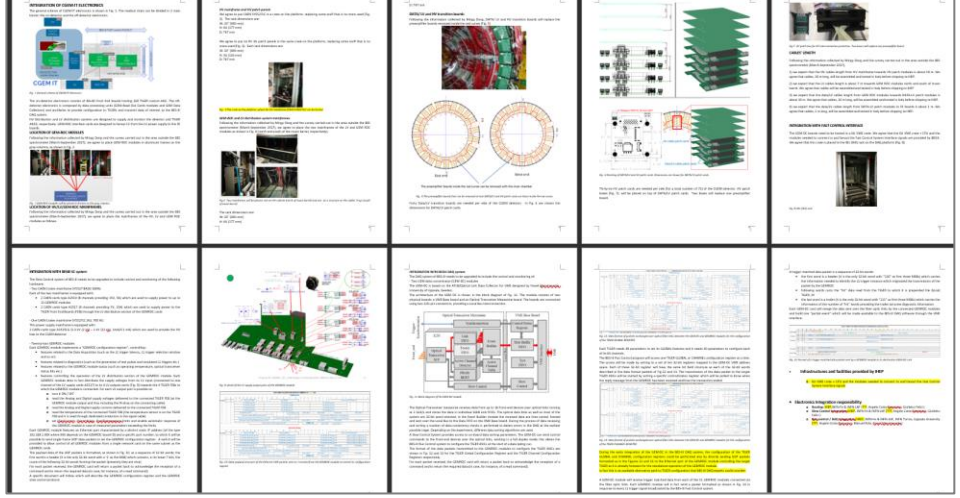
- Issue 1: lack document for Physics run mode data acquisition
- Issue 2: readout mode inconsistent with BESIII
- Issue 3: define different Run Modes for CGEM

Run Mode / Detector	Physics	Pedestal	Calibration	Monitor
MDC	√	×	√	×
EMC	√	√	√	√
MUON	√	×	×	×
TOF	√	×	×	√
TRG	√	×	×	×
CGEM	√	?	?	?



Dedicated meeting(s)

CGEM READOUT/ BESIII DAQ



4 MONTHS AGO

CGEM-IT electronics procedures

Before run

- GEMROC/TIGER configuration:
  - TIGER settings:
    - Load default settings (all the same)
    - Load specific TIGER settings
    - Load threshold settings (by channel)
    - Disable listed channels
  - GEMROC settings:
    - Load default settings
    - Set "pause mode"
- 8b/10b error status check

During run

- IVT status check
- 8b/10b error status check

Periodic procedures /on demand

- Threshold scan
- TD scan

Expert debug procedures

- GUFI controlled?

4 MONTHS AGO 14 views

CGEM DAQ discuss

Documentation

My Thesis -> Overview of the chain and details about GEMROC's and GUFI

Fabio Cossio's Thesis -> details about TIGER

The CGEM readout chain -> JINST article about the whole electronic chain

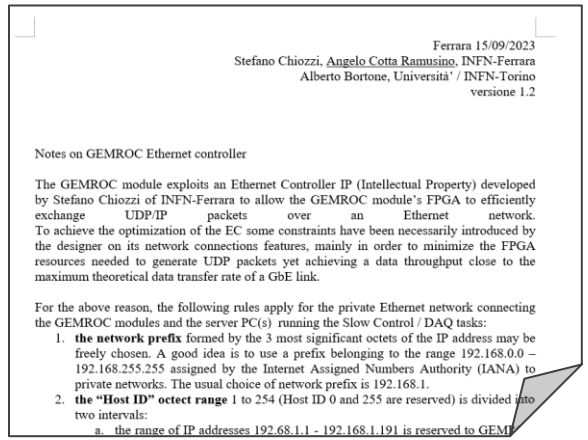
Fabio's presentation about TIGER pass: Cgem2023

UDP format file -> GEMROC packet format pass: Cgem2023

We are working on a complete wiki, expecially for GEMROCs, I will keep you updated.

1. what is the config process before physics data taking mode ? Can you provide me a document about this topic ?
   - I will provide a specific document for it.
2. what config variable and command is used by DAQ?
3. what is the meaning of each config varible?
   - You can find TIGER variables in Fabio's thesis, yc we are working on
4. what is the meaning of each config command?
   - TIGER codes:

code	name	action
0x0	CMD_WRCHCFG	Write the global configuration into TIGER register



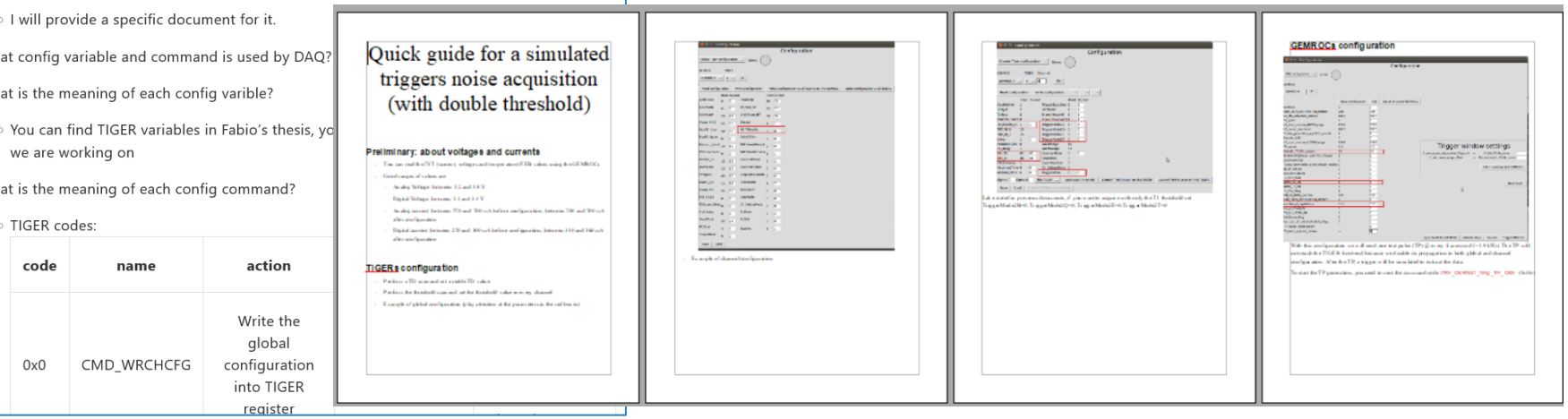
Ferrara 15/09/2023
Stefano Chiozzi, Angelo Cotta Ramusino, INFN-Ferrara
Alberto Bortone, Universita' / INFN-Torino
versione 1.2

Notes on GEMROC Ethernet controller

The GEMROC module exploits an Ethernet Controller IP (Intellectual Property) developed by Stefano Chiozzi of INFN-Ferrara to allow the GEMROC module's FPGA to efficiently exchange UDP/IP packets over an Ethernet network. To achieve the optimization of the EC some constraints have been necessarily introduced by the designer on its network connections features, mainly in order to minimize the FPGA resources needed to generate UDP packets yet achieving a data throughput close to the maximum theoretical data transfer rate of a GbE link.

For the above reason, the following rules apply for the private Ethernet network connecting the GEMROC modules and the server PC(s) running the Slow Control / DAQ tasks:

1. **the network prefix** formed by the 3 most significant octets of the IP address may be freely chosen. A good idea is to use a prefix belonging to the range 192.168.0.0 – 192.168.255.255 assigned by the Internet Assigned Numbers Authority (IANA) to private networks. The usual choice of network prefix is 192.168.1.
2. **the "Host ID" octect range** 1 to 254 (Host ID 0 and 255 are reserved) is divided into two intervals:
   a. the range of IP addresses 192.68.1.1 - 192.168.1.191 is reserved to GEM



Documentation provided or underway

CGEM READOUT

Firmware update
- UDP packets format

>> Alberto

@CGEM workshop

New packet format needed to decouple DAQ and Slow Control registers write operation
Already implemented in GUFI and DAQ test software

Before

	Operations (e.g.)	Command	Effect
DAQ Server	Thr scan counter set	LV_CFG_WR	Overwrite FEB power settings
Slow Control Server	Power ON FEBs	LV_CFG_WR	Overwrite scan settings

Now

	Operations (e.g.)	Command	Effect
DAQ Server	Thr scan counter set	LV_COUNTER_SET	No SC register overwrite
Slow Control Server	Power ON FEBs	LV_CFG_WR	No DAQ register overwrite

CGEM READOUT

Firmware update
- GEMROC addresses

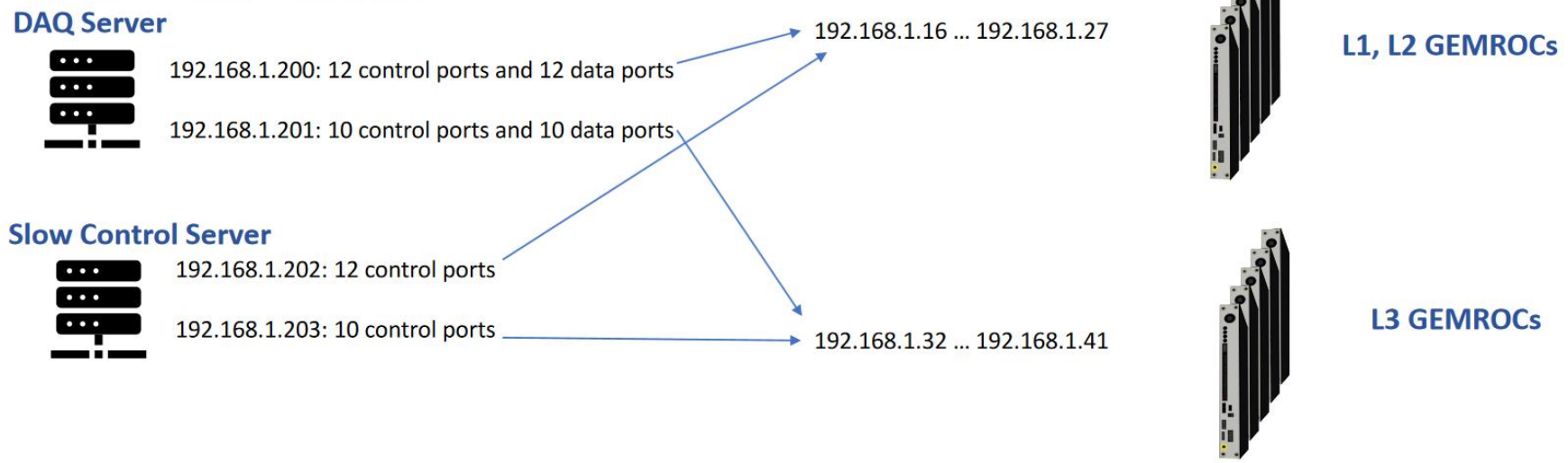
>> Alberto

@CGEM workshop

New address/port structure in order to connect 22 GEMROCs with a simple structure.

- IP addresses from 192.168.1.16 to 192.168.1.47 (determined by GEMROC ID number)
- A range of 16 ports for every operation (data, configuration ecc.), due to GEMROC Ethernet controller structure
- Two destination IP needed on the control PC in order to manage all the GEMROC.
- GUFI and DAQ test software already compatible with this patch

A possible network structure:



CGEM READOUT

Firmware update
- IVT log

New Current (I), Voltage (V) and Temperature (T) log mode:

>> Damiano

```
switch(cmd_code_4bit)
{
//  #define CMD_GEMROC_NONE 0x0
case CMD_GEMROC_LV_CFG_WR:       Update_GEMROC_CFG_LV(Number_of_packet_words);    break; // defined 0x
case CMD_GEMROC_LV_CFG_RD:       Read_GEMROC_CFG_LV(Number_of_packet_words);      break; // defined 0x
case CMD_GEMROC_LV_IVT_UPDATE:   Perform_IVT_update(Number_of_packet_words);      break; // defined 0x
case CMD_GEMROC_LV_IVT_READ:     Perform_IVT_read(Number_of_packet_words);        break; // defined 0x
case CMD_GEMROC_LV_TIMING_DELAYS_UPDATE: GEMROC_update_timing_delays(Number_of_packet_words); break;
case CMD_GEMROC_LV_REMOTE_HARD_RESET: Perform_GEMROC_HARD_RST(Number_of_packet_words); break; // def
default:    break;
}
```

GUFI 8 s

GUFI 30 s

GEMROC

```
void Perform_IVT_read(int Num_of_packet_words) // last update: cab 2023-06-06
{
    int i;
    Perform_IVT_read_and_Check_Interlock(); // cab 2023-06-06

    // acr 2018-01-07 BEGIN adding a set of control to separate Analog/Digital V and I
    U32 command_words_array[Num_of_packet_words-11] = 0;
```

```
// cab 2023-06-06 BEGIN
time(&T_CONTROL);
if (difftime(T_CONTROL,T_LAST_CHECK)>INTERLOCK_CHECK_DELAY)
{
    Perform_IVT_read_and_Check_Interlock();
}
// cab 2023-06-06 END
```

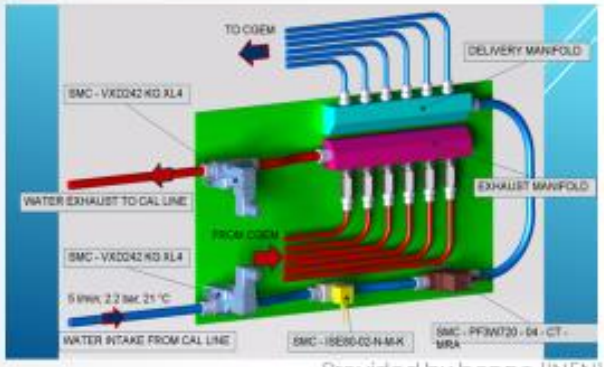
```
void Perform_IVT_read_and_Check_Interlock()
{
    Read_IVT_ADC(); // cab 2023-05-31

    Interlock_PIN_Check(); // cab 2023-05-31

    time(&T_LAST_CHECK);
}
```

CGEM / BESIII SC

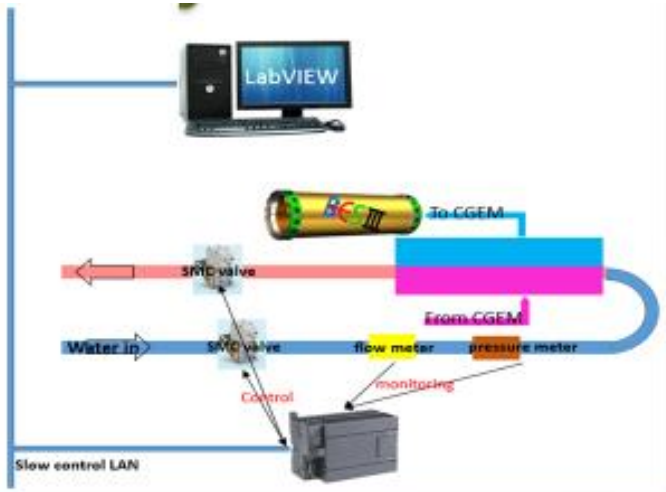
2019

CGEM COOLING

- Requirements



Provided by beppe (INFN)



Cooling control and monitoring architecture (PLC option)

- Readout design plan
  - PLC controller option
    - Two electromagnetic valves are necessary to be controlled remotely, flow and pressure need to be monitored.
  - Embedded board option
    - Two electromagnetic valves are necessary to be local controlled, flow and pressure need to be monitored.

Documentation checked

Paolo Mereu onsite
at the end of November

INTEGRATION Working Group @IHEP, end of November
Angelo, Damiano, Fabio, Giulio, GG, Manuel, Matias, Michela, Paolo

NEED TO FILL THE GAP in DAQ &SC activities asap

PERFORMANCE REVIEW.....COMING!