



# CGEM-TEGRATION

MGRECO on behalf of CGEM-IT working group

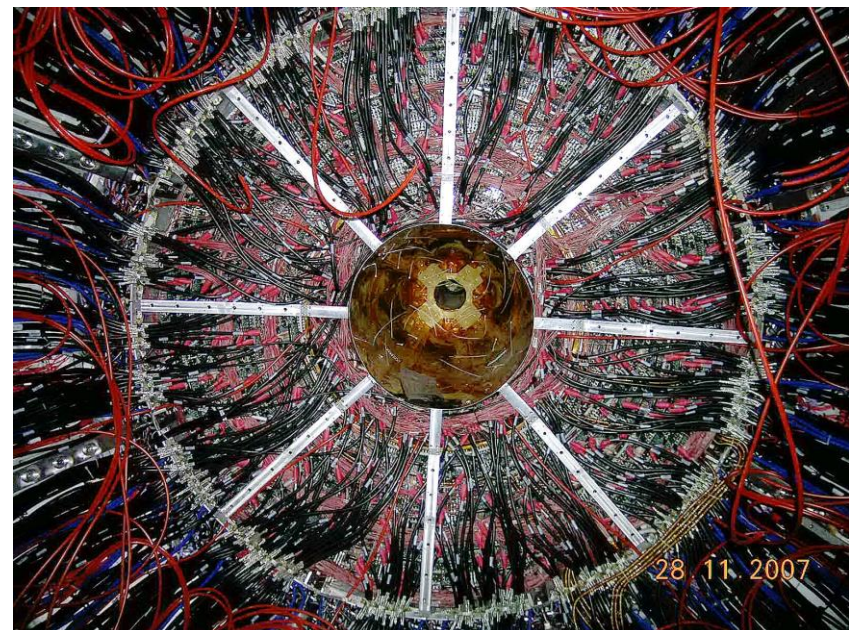
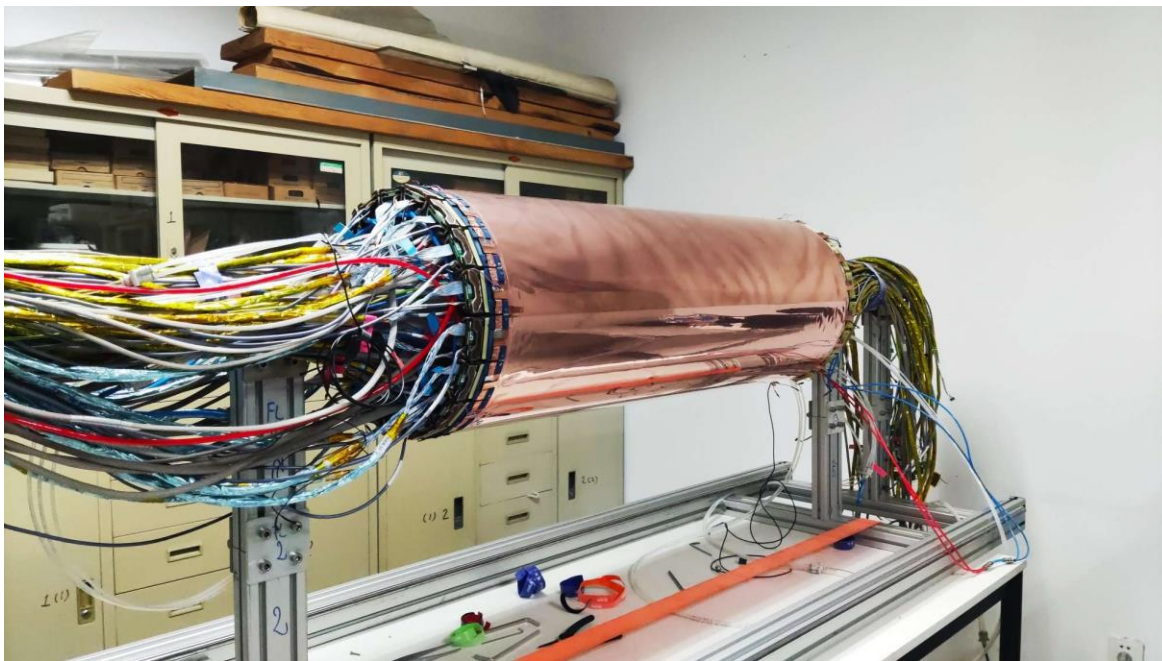


# OUTLINE

1. CGEM/BESIII
2. CGEM frontend electronics
3. CGEM readout
4. CGEM readout/BESIII DAQ
5. CGEM/BESIII Slow Control



# CGEM/BESIII





# CGEM/BESIII

## INTEGRATION issues for electronics

Placement of HV-LV-ROC Power Supply mainframes  
Placement of GEM ROC modules  
Cable Routing

Information exchange with Mingyi Dong in July



M. Greco, CGEM workshop,  
15 September 2017

BESIII

CGEM-IT

## ROC+LV/HV PS



GEM ROC PS  
on the cabinet (N)



GEM ROC PS & LV PS  
on the cable trays (S)



HV PS on the  
platform

M. Greco, CGEM workshop, September 2017

CGEM-IT

## ROC+PS

On site survey with Angelo Cotta Ramusino



ph@ A. C. Ramusino

GEM ROCs  
In frames on the gray columns  
On E/W/N/S

GEM ROC stand alone modules: 334 mmx176mmx44mm

BESIII

M. Greco, CGEM workshop, September 2017

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## ROUTING



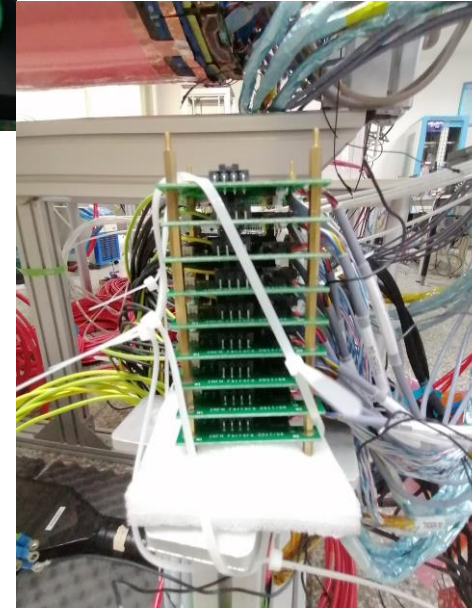
A. C. Ramusino

Signal cable length from LV-DATA  
TB to GEM ROC modules about 10 m

Cable length from GEM ROC to  
GEM ROC PS about 4 m (N)  
about 5 m (S)

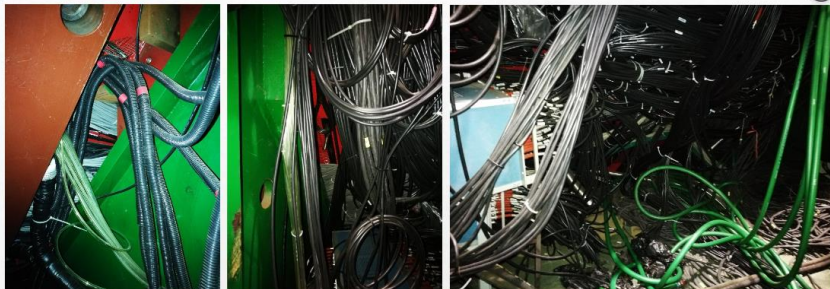


Cable length from GEM ROC to LV PS  
about 10 m (N)  
about 5 m (S)

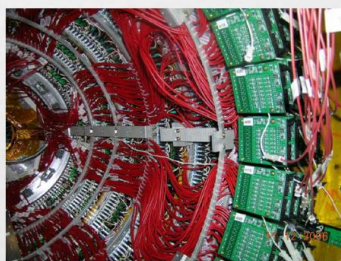




## ROUTING

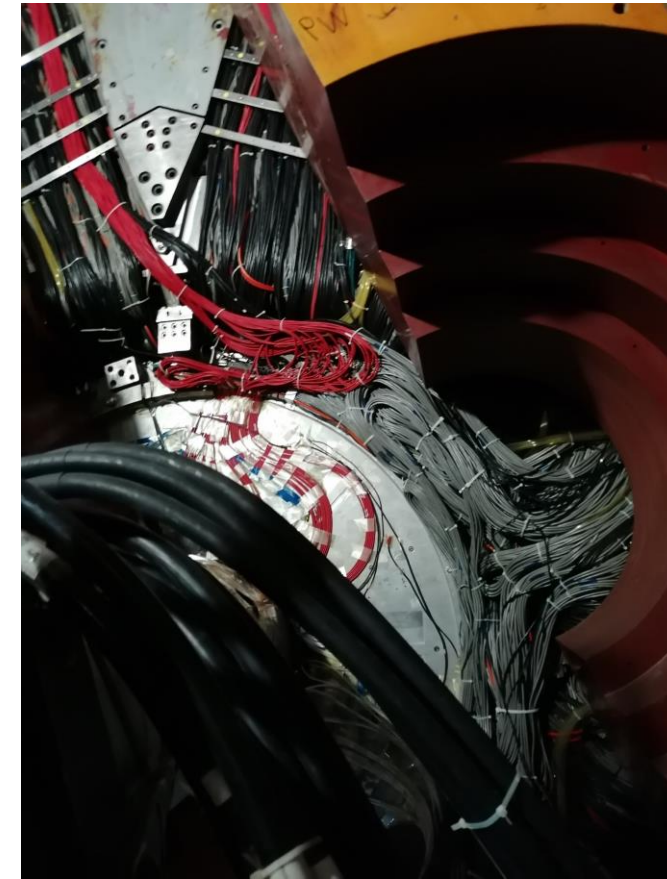
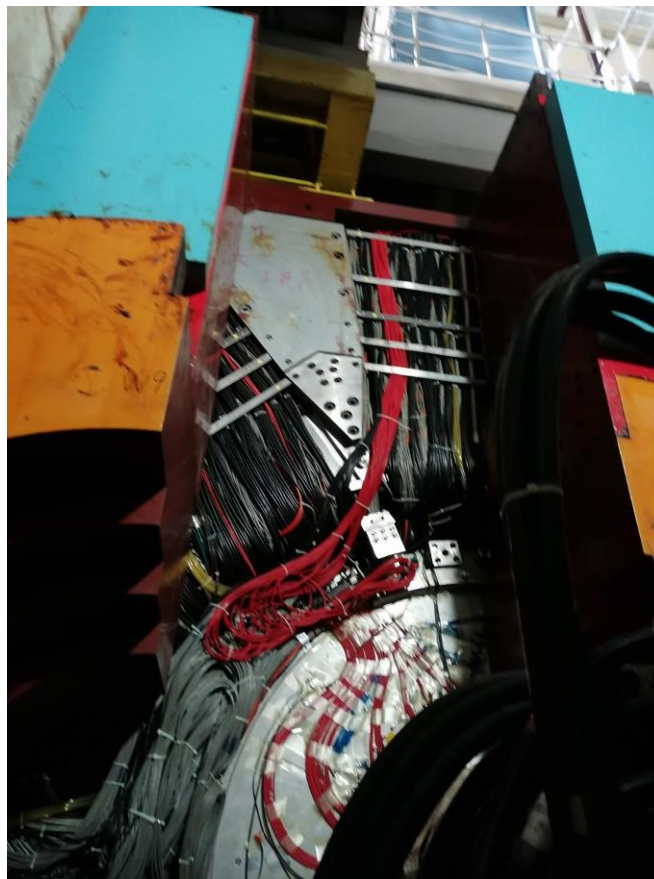


Not an easy operation



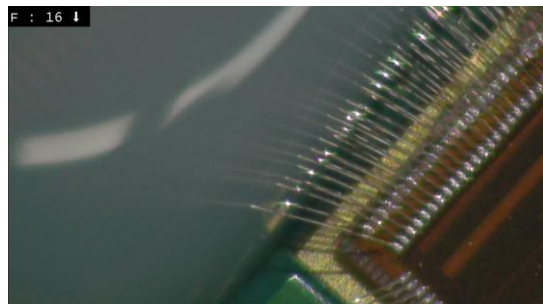
2017/2023

not an easy operation





# CGEM FRONT-END ELECTRONICS



## TIGER

All chips have been encapsulated. Few losses.  
Monitoring since July

Further FEB spares: order ongoing



# CGEM READOUT ELECTRONICS: GEMROC

22 GEMROC needed

>> talk by Angelo

16 already used for L1/L2/half L3;

21 available at Beijing +1 «malfunctioning» @Beijing

2 already mounted by ACR( to be sent with GG &Riccardo)

-Spares:

4 to be mounted by ACR ( or mounted in the meanwhile)

1 sent to Ferrara

>> talk by Ilaria Neri

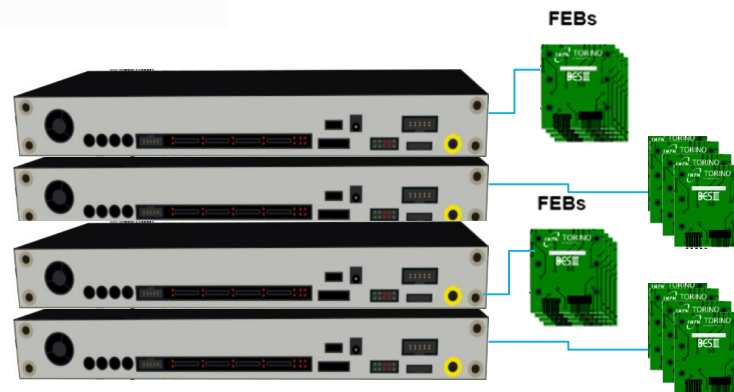
Further developments



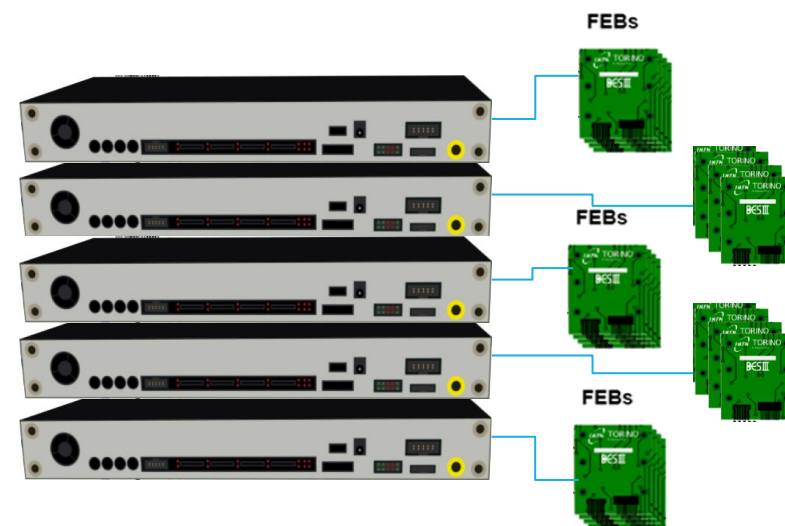
# GEMROC



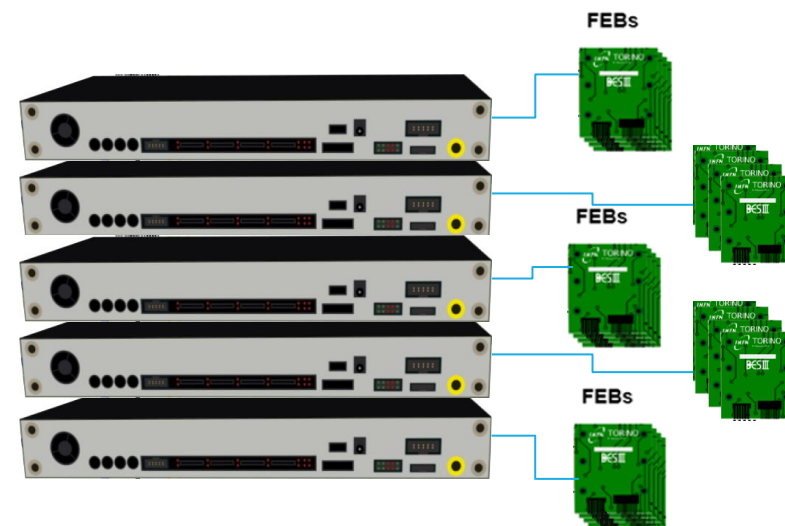
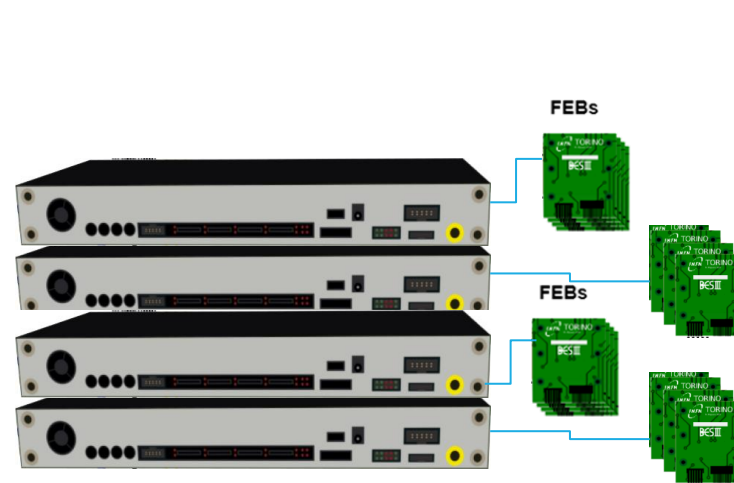
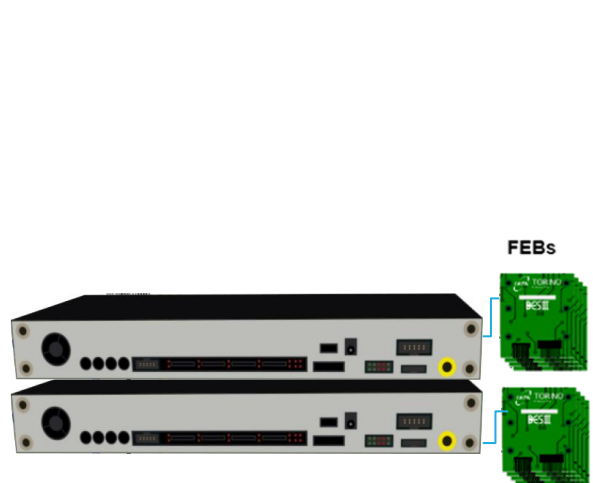
Layer 1



Layer 2



Layer 3

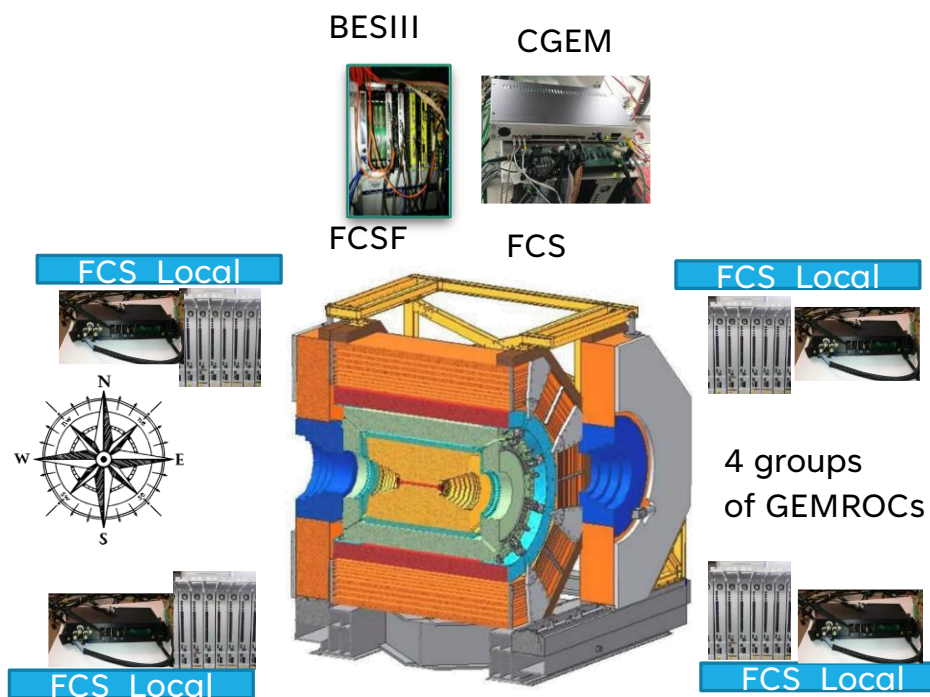




# CGEM READOUT ELECTRONICS: FANOUT

FCS: a modified GEMROC module which connects to the CLK, L1, L1\_CHK, FULL signals from the BESIII Fast Control System Fanout

>> talk by Angelo



FCS\_Local, fanout modules which connects to the CLK, L1, L1\_CHK, FULL signals from FCS

FCS\_Local

FCS backplane: 5 available ( 4 needed)

FCS Flat Cable Ports: 5 available ( 4 needed)

FCS backplane interface: under check ->checked

FCS terminator: layout refined, under production

Modules will be mounted with the help of Nicholas

# READOUT ELECTRONICS: GEMROC<>GEMDC

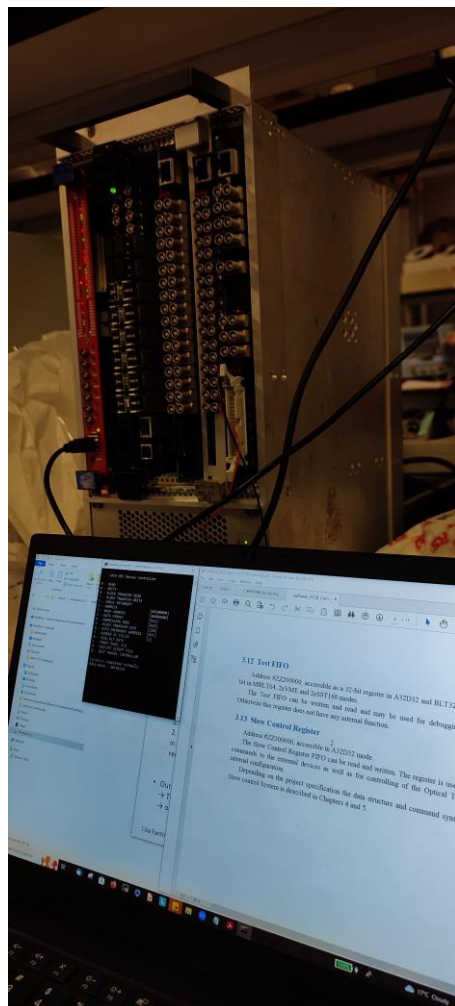
GEM DC from LNF

Pawel @ Fe

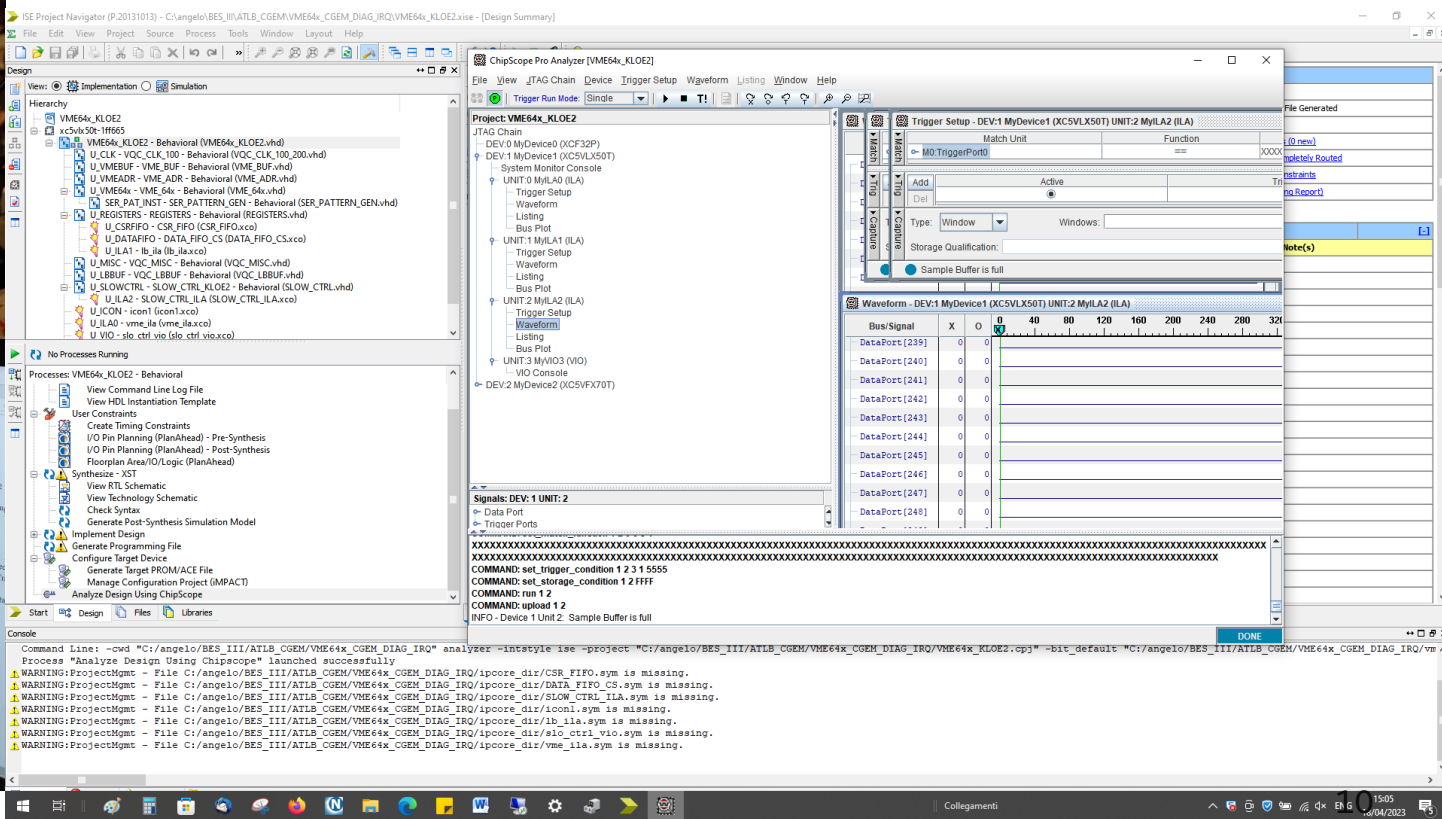
End of March/April

Debugging by

Angelo



>> talk by Angelo





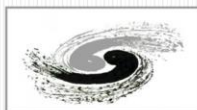
# CGEM READOUT/~~BES~~III DAQ

## Progress and Status of CGEM DAQ

Tingxuan Zeng

TDAQ Group, Experimental Physics Division, IHEP

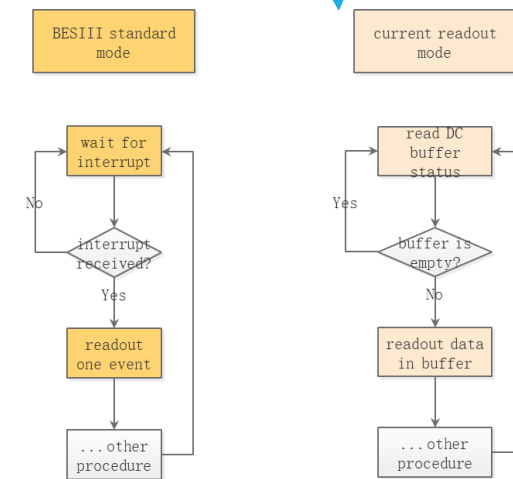
2023.09.25



- Issue 1: lack document for Physics run mode data acquisition
- Issue 2: readout mode inconsistent with BESIII
- Issue 3: define different Run Modes for CGEM

Run Mode Detector	Physics	Pedestal	Calibration	Monitor
MDC	✓	✗	✓	✗
EMC	✓	✓	✓	✓
MUON	✓	✗	✗	✗
TOF	✓	✗	✗	✓
TRG	✓	✗	✗	✗
CGEM	✓	?	?	?

Dedicated meeting(s)



# CGEM READOUT/ BESIII DAQ

4 MONTHS AGO

## CGEM-IT electronics procedures

### Before run

- GEMROC/TIGER configuration:
  - TIGER settings:
    - Load default settings (all the same)
    - Load specific TIGER settings
    - Load threshold settings (by channel)
    - Disable listed channels
  - GEMROC settings:
    - Load default settings
    - Set "pause mode"
- 8b/10b error status check

### During run

- IVT status check
- 8b/10b error status check

### Periodic procedures /on demand

- Threshold scan
- TD scan

### Expert debug procedures

- GUFi controlled?

4 MONTHS AGO

14 views

## CGEM DAQ discuss

### Documentation

[My Thesis](#) -> Overview of the chain and details about GEMROC's and GUFi

[Fabio Cossio's Thesis](#) -> details about TIGER

[The CGEM readout chain](#) -> JINST article about the whole electronic chain

[Fabio's presentation about TIGER](#) pass: Cgem2023

[UDP format file](#) -> GEMROC packet format pass: Cgem2023

We are working on a complete wiki, especially for GEMROCs, I will keep you updated.

- what is the config process before physics data taking mode ? Can you provide me a document about this topic ?
  - I will provide a specific document for it.
- what config variable and command is used by DAQ?
- what is the meaning of each config variable?
  - You can find TIGER variables in Fabio's thesis, you are working on
- what is the meaning of each config command?

code	name	action
0x0	CMD_WRCHCFG	Write the global configuration into TIGER register

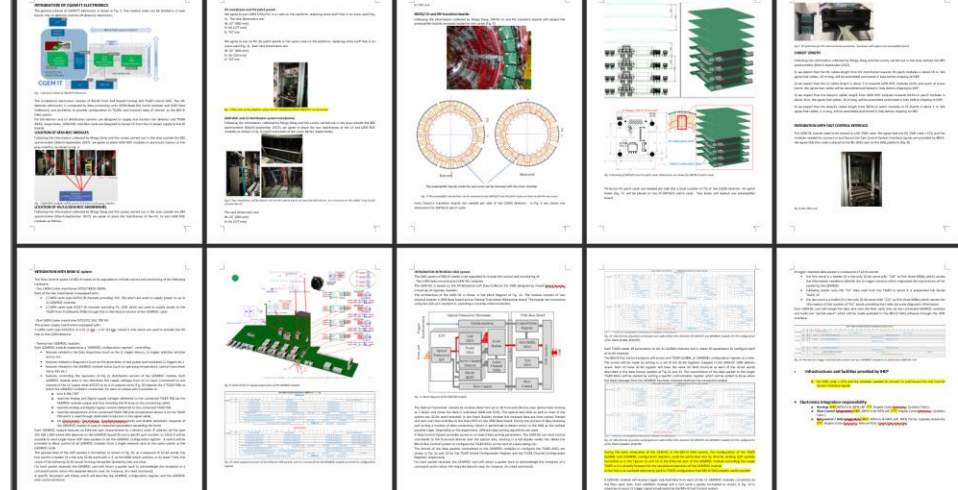
### Quick guide for a simulated triggers noise acquisition (with double threshold)

**Preliminary: about voltages and currents**

- The user must be able to control the voltage and current levels of the TIGER channels.
- Control range of voltage and current:
- Working voltage between 1.2 and 1.8 V
- Digital voltage between 1.1 and 1.5 V
- Working current between 150 and 300 mA before and after acquisition, between 100 and 300 mA after acquisition
- Digital current between 200 and 300 mA before and after acquisition, between 100 and 300 mA after acquisition

#### TIGER's configuration

- Perform a TD scan and set a valid TD value
- Perform the threshold scan and set the threshold value in the channel
- Example of global configuration to be extended at the procedure that will be used



Ferrara 15/09/2023  
Stefano Chiozzi, Angelo Cotta Ramusino, INFN-Ferrara  
Alberto Bortone, Università / INFN-Torino  
versione 1.2

#### Notes on GEMROC Ethernet controller

The GEMROC module exploits an Ethernet Controller IP (Intellectual Property) developed by Stefano Chiozzi of INFN-Ferrara to allow the GEMROC module's FPGA to efficiently exchange UDP/IP packets over an Ethernet network. To achieve the optimization of the EC some constraints have been necessarily introduced by the designer on its network connections features, mainly in order to minimize the FPGA resources needed to generate UDP packets yet achieving a data throughput close to the maximum theoretical data transfer rate of a GbE link.

For the above reason, the following rules apply for the private Ethernet network connecting the GEMROC modules and the server PC(s) running the Slow Control / DAQ tasks:

- the **network prefix** formed by the 3 most significant octets of the IP address may be freely chosen. A good idea is to use a prefix belonging to the range 192.168.0.0 – 192.168.255.255 assigned by the Internet Assigned Numbers Authority (IANA) to private networks. The usual choice of network prefix is 192.168.1.
- the **"Host ID" octet range** 1 to 254 (Host ID 0 and 255 are reserved) is divided into two intervals:
  - the range of IP addresses 192.168.1.1 - 192.168.1.191 is reserved to GEMROC

Documentation  
provided or underway



# CGEM READOUT

## Firmware update

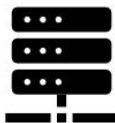

- UDP packets format

>> Alberto


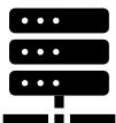
New packet format needed to decouple DAQ and Slow Control registers write operation  
Already implemented in GUF1 and DAQ test software

@CGEM workshop

Before

	Operations (e.g.)	Command	Effect
<b>DAQ Server</b> 	Thr scan counter set	LV_CFG_WR	Overwrite FEB power settings
<b>Slow Control Server</b> 	Power ON FEBs	LV_CFG_WR	Overwrite scan settings

Now

	Operations (e.g.)	Command	Effect
<b>DAQ Server</b> 	Thr scan counter set	LV_COUNTER_SET	No SC register overwrite
<b>Slow Control Server</b> 	Power ON FEBs	LV_CFG_WR	No DAQ register overwrite

# CGEM READOUT

## Firmware update

- GEMROC addresses

>> Alberto

@CGEM workshop

New address/port structure in order to connect 22 GEMROCs with a simple structure.

- IP addresses from 192.168.1.16 to 192.168.1.47 (determined by GEMROC ID number)
- A range of 16 ports for every operation (data, configuration ecc.), due to GEMROC Ethernet controller structure
- Two destination IP needed on the control PC in order to manage all the GEMROC.
- GUFi and DAQ test software already compatible with this patch

A possible network structure:

### DAQ Server



192.168.1.200: 12 control ports and 12 data ports

192.168.1.201: 10 control ports and 10 data ports

### Slow Control Server



192.168.1.202: 12 control ports

192.168.1.203: 10 control ports

192.168.1.16 ... 192.168.1.27

192.168.1.32 ... 192.168.1.41



L1, L2 GEMROCs



L3 GEMROCs



# CGEM READOUT

## Firmware update

- IVT log

New Current (I), Voltage (V) and Temperature (T) log mode:

>> Damiano

```
switch(cmd_code_4bit)
{
// #define CMD_GEMROC_NONE 0x0
case CMD_GEMROC_LV_CFG_WR:    Update_GEMROC_CFG_LV(Number_of_packet_words); break; // defined 0x
case CMD_GEMROC_LV_CFG_RD:    Read_GEMROC_CFG_LV(Number_of_packet_words); break; // defined 0x
case CMD_GEMROC_LV_IVT_UPDATE: Perform_IVT_update(Number_of_packet_words); break; // defined 0x
case CMD_GEMROC_LV_IVT_READ:  Perform_IVT_read(Number_of_packet_words); break; // defined 0x
case CMD_GEMROC_LV_TIMING_DELAYS_UPDATE: GEMROC_update_timing_delays(Number_of_packet_words); break;
case CMD_GEMROC_LV_REMOTE_HARD_RESET: Perform_GEMROC_HARD_RST(Number_of_packet_words); break; // def
default: break;
}
```



GUF 8 s



GUF 30 s



GEMROC

```
// cab 2023-06-06 BEGIN
time(&T_CONTROL);
if (difftime(T_CONTROL,T_LAST_CHECK)>INTERLOCK_CHECK_DELAY)
{
    Perform_IVT_read_and_Check_Interlock();
}
// cab 2023-06-06 END
```

```
void Perform_IVT_read(int Num_of_packet_words) // last update: cab 2023-06-06
{
    int i;
    Perform_IVT_read_and_Check_Interlock(); // cab 2023-06-06

    // acr 2018-01-07 BEGIN adding a set of control to separate Analog/Digital V and I
    U32 command_words_array[Num_of_packet_words-11] = 0;
```



```
void Perform_IVT_read_and_Check_Interlock()
{
    Read_IVT_ADC(); // cab 2023-05-31
    Interlock_PIN_Check(); // cab 2023-05-31
    time(&T_LAST_CHECK);
}
```

# CGEM / BESIII SC

2019

## The Status of CGEM Slow Control System

Speaker: Si Ma  
On behalf of IHEP DAQ Group  
2019.06.29

## Outline

- CGEM DCS architecture
- The current development status of subsystems
- Next plan

## CGEM DCS architecture

The CGEM DCS is divided into three layers the same as other detectors of BESIII:

- Frontend layer (FEL)
  - Convert signals such as temperature and pressure into digital information
  - Execute control commands sent from the LCS
- Local control layer (LCL)
  - To acquire data from the FEL and offer supervisory and control functions
  - Software based on BESIII DCS framework
- Global control layer (GCL)
  - Including a GCS, a database server and a web server

## The subsystems of CGEM DCS

- High voltage control & monitoring system
  - GEMROC control & monitoring
  - GEMROC and TIGER power supply control & monitoring
- VME control & monitoring system
- Gas control & monitoring system
- Cooling control & monitoring system

## HV subsystem

### Requirements

- Control and monitoring two A1515CG CAEN cards inside the SY352/LC mainframe

### Software development progress

- Implemented the development of local control station program
- Completed integration with the BESIII DCS framework
- It includes a high pressure elevation, configuration parameters, save data to the database, alarm functions and etc.

### HV commissioning status

- The mainframe equipped with single card has been commissioning for a week and running well

## LV subsystem

### Requirements

- For power supply:
  - Control and monitoring two A2019 cards housed in SY352 which are used to power supply to GEMROC modules
- Control and monitoring two A2017 cards housed in SY352 which are used to power supply to TIGER FEB

### Software development progress

- For GEMROC modules:
  - Monitoring TIGER FEB voltage, current and temperature
  - Setting OVC, OVI, OVT limits and enable automatic operation
- The LabVIEW software library was developed based on the GEMROC python program
- Implemented the development of local control station program
- Integration with BESIII DCS framework is in progress

### LV commissioning status

- Since GEMROC hardware platform has just been set up in our lab, debugging of the LabVIEW library with GEMROC is in progress.

## VME subsystem

### Requirements

- Control power switch
- Monitoring voltage, current, temperature and fan speed

### Software development progress

- Reuse of other VME software design and implementation of BESIII

### VME commissioning status

- Stable operation in the laboratory for nearly one month

## Gas subsystem

### Requirements

Parameter Name	Unit	Analog Signal	Range
High gas pressure	bar	4-20mA	0-10
Low gas pressure	bar	4-20mA	0-10
Gas temperature	°C	4-20mA	0-100
Gas flow rate	SLM	4-20mA	0-100
Gas humidity	%	4-20mA	0-100
Gas purity	%	4-20mA	0-100

(provided by BESIII team)

### Software design

- A Programmable Logic Controller (PLC) will be installed with sensors and controllers for gas monitoring and control.
- Because of requirements and schematics are similar to BESIII MRPC gas system, the design and implementation of PLC program refers to the MRPC gas system.

### Development status

- PLC program development is in progress.

## Cooling subsystem

### Requirements

- Monitoring temperature and pressure of cooling water
- Monitoring flow rate of cooling water
- Monitoring status of cooling water pump

### Readout design plan

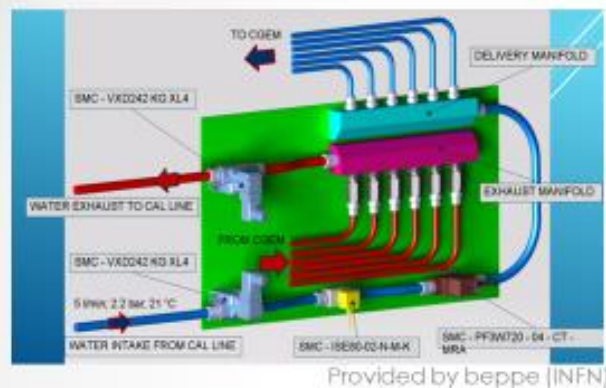
- PLC controller option
  - Two electromagnetic valves are necessary to be controlled remotely, flow and pressure need to be monitored.
- Embedded board option
  - Two electromagnetic valves are necessary to be local controlled, flow and pressure need to be monitored.

### Cooling control and monitoring architecture (PLC option)



# CGEM COOLING

## Requirements



## Readout design plan

### PLC controller option

- Two electromagnetic valves are necessary to be controlled remotely, flow and pressure need to be monitored.

### Embedded board option

- Two electromagnetic valves are necessary to be local controlled, flow and pressure need to be monitored.



Cooling control and monitoring architecture (PLC option)

Documentation checked

Paolo Mereu onsite  
at the end of November



INTEGRATION Working Group @IHEP, end of November  
Angelo, Damiano, Fabio, Giulio, GG, Manuel, Matias, Michela, Paolo

NEED TO FILL THE GAP in DAQ & SC activities asap

**PERFORMANCE REVIEW.....COMING!**