Nuclear Inst. and Methods in Physics Research, A

Development of High Voltage-CMOS sensors within the CERN-RD50 collaboration

--Manuscript Draft--

Manuscript Number:	
Article Type:	VSI:VERTEX 2021
Keywords:	CERN-RD50; depleted monolithic active pixel sensor; future hadron colliders; high voltage-CMOS technology; high voltage pixel detector; monolithic CMOS detector.
Corresponding Author:	Eva Vilella, PhD University of Liverpool Liverpool, UNITED KINGDOM
First Author:	Eva Vilella, PhD
Order of Authors:	Eva Vilella, PhD
Abstract:	This paper presents work done by the CERN-RD50 collaboration to develop and study monolithic CMOS sensors for future hadron colliders, especially in terms of radiation tolerance, time resolution and granularity. Currently CERN-RD50 is completing the performance evaluation of RD50-MPW2 and the design of RD50-MPW3, the second and third prototype sensor chips by the collaboration. The paper gives an overview of the main design aspects and performance evaluation results of RD50-MPW1 and RD50-MPW2, and details the design of RD50-MPW3. RD50-MPW2 is a small prototype with an 8 x 8 matrix of active pixels which implement analogue readout electronics only and solutions for low leakage currents. This prototype has been evaluated extensively in the lab and also at proton and ion beam facilities, before and after irradiation with neutrons up to 2x1015 neq/cm2. RD50-MPW3 is a more advanced prototype with a matrix of 64 x 64 pixels which integrate both analogue and digital readout electronics inside the sensing diodes. To alleviate routing congestion and minimise crosstalk noise, the pixels are serially configured and organised in a double column scheme. This prototype has optimised peripheral readout electronics for effective chip configuration, based on the I2C protocol, and fast data transmission.

Development of High Voltage-CMOS sensors within the CERN-RD50 collaboration

E. Vilella[a,*], on behalf of the CERN-RD50 collaboration

[a] *The University of Liverpool, Department of Physics, Liverpool L69 7ZE, UK*

Abstract

This paper presents work done by the CERN-RD50 collaboration to develop and study monolithic CMOS sensors for future hadron colliders, especially in terms of radiation tolerance, time resolution and granularity. Currently CERN-RD50 is completing the performance evaluation of RD50-MPW2 and the design of RD50-MPW3, the second and third prototype sensor chips by the collaboration. The paper gives an overview of the main design aspects and performance evaluation results of RD50-MPW1 and RD50-MPW2, and details the design of RD50-MPW3. RD50-MPW2 is a small prototype with an 8 x 8 matrix of active pixels which implement analogue readout electronics only and solutions for low leakage currents. This prototype has been evaluated extensively in the lab and also at proton and ion beam facilities, before and after irradiation with neutrons up to $2x10^{15}$ n_{eq}/cm^2. RD50-MPW3 is a more advanced prototype with a matrix of 64 x 64 pixels which integrate both analogue and digital readout electronics inside the sensing diodes. To alleviate routing congestion and minimise crosstalk noise, the pixels are serially configured and organised in a double column scheme. This prototype has optimised peripheral readout electronics for effective chip configuration, based on the I2C protocol, and fast data transmission.

* Corresponding author. Tel.: +44(0)151 794 9412; e-mail: vilella@hep.ph.liv.ac.uk. See https://rd50.web.cern.ch/rd50/db/report/authors-list.aspfor full authors list.

Keywords: CERN-RD50, depleted monolithic active pixel sensor, future hadron colliders, high voltage-CMOS technology, high voltage pixel detector, monolithic CMOS detector.

1. Introduction

This paper presents results from the RD50-MPW series of monolithic CMOS sensors, developed by the CERN-RD50 collaboration to study this technology in view of the harsh requirements imposed by future hadron colliders on tracking systems [1, 2]. The RD50-MPW sensors developed so far are in the 150 nm High Voltage-CMOS (HV-CMOS) process from LFoundry S.r.l. Parameters especially considered in this programme are radiation tolerance, time resolution and granularity.

2. Overview of monolithic CMOS sensors with CERN-RD50

RD50-MPW1, the first CMOS sensor developed by the collaboration, has a matrix of 40 rows x 78 columns of high-granularity pixels where these integrate the analogue and digital readout electronics inside their area of 50 µm x 50 µm. The analogue readout, based on conventional electronics for charge-collecting detectors, includes a Charge Sensitive Amplifier (CSA) with continuous reset, low-pass and high-pass filters, and a CMOS comparator with a 4-bit Digital-to-Analogue Converter (DAC) to tune locally small threshold voltage variations. The digital readout is based on the well-known column drain architecture (i.e. FE-I3 style) [3]. It provides two 8-bit time-stamps, one for the leading edge and another one for the trailing edge, and an 8-bit address. When a pixel registers an event, it sends the leading and trailing edge time-stamps, and its address, to the corresponding End-Of-Column (EOC) circuit at the periphery through a 24-bit bus. This bus is shared by all the pixels within a column. The 78 EOC circuits of the matrix, which function as two 16-bit parallel-in parallel-out shift-registers, are connected to two readout serialisers designed to run at a maximum speed of 640 MHz.

The Data Acquisition System (DAQ) for the RD50-MPW sensor chips builds on the general-purpose Control and Readout (CaR) board [4]. It comprises a dedicated chip carrier board, the CaR board, an FPGA Mezzanine

Card (FMC) and a Xilinx ZC706 or ZC702 evaluation board. The evaluation of fabricated RD50-MPW1 samples has revealed this chip essentially works, but also that it suffers from high leakage current in the sensing diodes, voltage drops across the pixel matrix and crosstalk noise between the lines that carry digital signals. Several RD50-MPW1 samples have been irradiated with neutrons up to $2x10^{15}$ n_{eq}/cm^2 at the TRIGA reactor in Ljubljana, Slovenia. The test structures of this chip, which consist of a small matrix of passive pixels, have been evaluated with the edge Transient Current Technique (eTCT) using the Particulars measurement system [5, 6]. The measured results show the irradiation effects are compatible with the literature.

RD50-MPW2, the successor chip, implements solutions that minimise the high leakage current observed in RD50-MPW1 and has a simple pixel matrix to test these. The solutions consist of a guard ring frame at the edge of the chip and the prevention of certain post-processing filling layers that involve conductive material. The guard ring frame has one n-type ring that acts as a current collecting ring and six p-type rings that control the termination of the lateral depletion of the sensing diodes, in addition to one p-type seal ring that protects the design from damage caused by the sawing process [7]. RD50-MPW1 has the p-type seal ring only. The matrix in RD50-MPW2 has 8 rows x 8 columns of 60 µm x 60 µm pixels with analogue readout only. The larger pixel size is due to the increase of the spacing between the p-n electrodes of the diode for a higher breakdown voltage (8 µm spacing in RD50-MPW2 as opposed to 3 µm spacing in RD50-MPW1). The matrix integrates two different flavours of readout electronics, with continuous and switched reset CSAs, optimised for fast response times to resolve particles at high rates [8].

RD50-MPW2 has been evaluated in the lab and also at proton and ion beam facilities. The leakage current of this prototype is 10^{-10} A/pixel (10^{-6} A/pixel in RD50-MPW1), the breakdown voltage 120 V (60 V in RD50-MPW1) and the time resolution less than 10 ns. The eTCT setup has been used to study the depletion region of the test structures, also integrated in RD50-MPW2 as a small matrix of passive pixels, after irradiation with neutrons up to $2x10^{15}$ n_{eq}/cm^2. The eTCT setup has also been used, for the first time, to investigate the time resolution of the active pixels in the 8 x 8 matrix [9]. The eTCT measurements show the depletion region is about 60 µm after irradiation to $2 \cdot 10^{15}$ n_{eq}/cm^2 and at 100 V substrate biasing (2.2 kΩ·cm nominal substrate resistivity), and the time resolution better than 10 ns after irradiation to $5 \cdot 10^{14}$ n_{eq}/cm^2 and also at 100 V (1.9 kΩ·cm nominal substrate resistivity). The proton test beams have been conducted at the Rutherford Cancer Centre in Northumberland, United

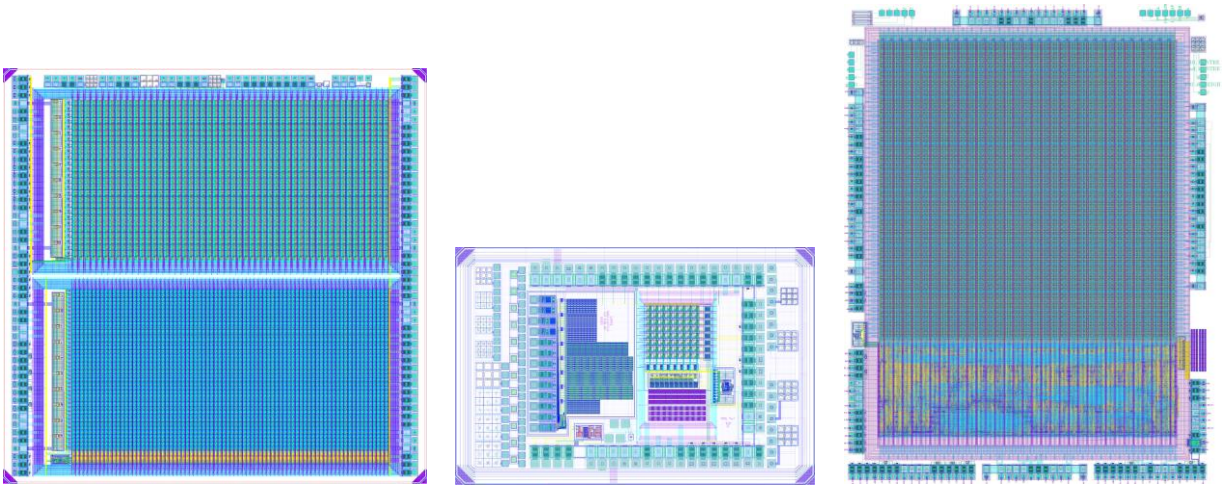
Kingdom, and MedAustron in Vienna, Austria [10, 11], and the ion test beams at the Ruđer Bošković Institute in Zagreb, Croatia. The test beam at the Northumberland Rutherford Cancer Centre focused on studying the analogue shaped output at different beam energies, while the test beam at Vienna MedAustron aimed at developing a beam telescope to test the tracking capability of RD50-MPW2. The experimental setup at Northumberland included, in addition to the CaR DAQ, scintillator triggers for coincide measurements. The data generated by the analogue shaped output was recorded for each event using a DRS4 switched capacitor array digitiser [12]. Proton beam energies between 70 and 229 MeV were used in this study. High beam energies produced analogue shaped outputs with smaller amplitudes, which indicates smaller energy deposition as expected. The telescope developed for the Vienna test beam comprises one RD50-MPW2 sample and CaR DAQ placed in the middle of two arms with two double sided silicon strip detectors each, and two scintillators at the very back of the setup. The telescope is triggered by the coincidence of the two scintillators. A new firmware was prepared to allow the synchronization of RD50-MPW2 with the other detectors of the telescope and the capability of accepting trigger signals. Time-over-threshold measurements taken in this test beam show a distribution peaking at 35 ns and are in good agreement with simulated results. The analysis of the ion test beam at the Zagreb Ruđer Bošković Institute is ongoing.

In spite of its success RD50-MPW2 has several design limitations, such as the small number of rows and columns of the pixel matrix, the lack of digital readout electronics to identify events and a very simple peripheral readout that makes certain type of measurements too slow or not possible. To give a specific example of the consequences of these limitations, in RD50-MPW2 only one pixel at a time can be read out and this has restricted the evaluation programme.

CERN-RD50 is developing a new prototype, RD50-MPW3, which integrates a larger and more advanced pixel matrix with new and optimised peripheral readout electronics to further study monolithic CMOS sensors. Figure 1 shows the layout views of the RD50-MPW monolithic CMOS sensors.

3. RD50-MPW3 design

RD50-MPW3 overcomes the limitations of RD50-MPW2 by extending the number of pixels in the matrix (64 columns x 64 rows), incorporating in the pixel area digital readout electronics based on the column drain architecture and adding optimised peripheral readout electronics for effective pixel configuration and fast data



(a) **(b)** **(c)**

Fig. 1. Layout views of RD50-MPW1 (a), RD50-MPW2 (b) and RD50-MPW3. The dimensions of these prototype sensor chips are 5 mm x 5 mm, 3.2 mm x 2.1 mm and 5.1 mm x 6.6 mm respectively.

transmission. RD50-MPW3 includes as well a few dedicated test structures, mostly to characterise the diode I-V, depletion region and parasitic capacitance. RD50-MPW3 is being fabricated in three different substrate resistivities, which are the standard resistivity (10 Ω·cm) and two high resistivities of 1.9 and 3 kΩ·cm.

3.1. Pixel electronics

The RD50-MPW3 in-pixel digital readout is a highly improved version of that developed for RD50-MPW1. It incorporates logic to mask noisy pixels, replaces the priority circuit that referees the order in which hits are read out for a less area-consuming alternative, and allows pausing the digitisation of new hits until the readout of a column is complete. Each pixel contains as well a new 8-bit SRAM shift register, which enables serial configuration and stores a per pixel-trimming to compensate for threshold voltage variations (four bits), a flag to mask noisy pixels (one bit), and data to enable or disable the calibration circuit (one bit), the amplifier output monitor (one bit) and the comparator output monitor (one bit). The configuration shift registers are programmed during the chip initialisation and hold the values indefinitely until the chip is reprogrammed or powered down. The analogue readout electronics reuse those developed for the continuous reset pixel of RD50-MPW2, as the lab and test beam evaluations concluded their performance is satisfactory. Details about the diode implementation are available in [1]. Figure 2

shows a simplified version of the pixel schematic. Figure 3 shows a mixed-mode simulation using the post-layout view of a pixel that receives a test pulse from the calibration circuit.

3.2. Double pixel scheme

RD50-MPW3 implements a double column scheme for the first time in the RD50-MPW prototypes, which

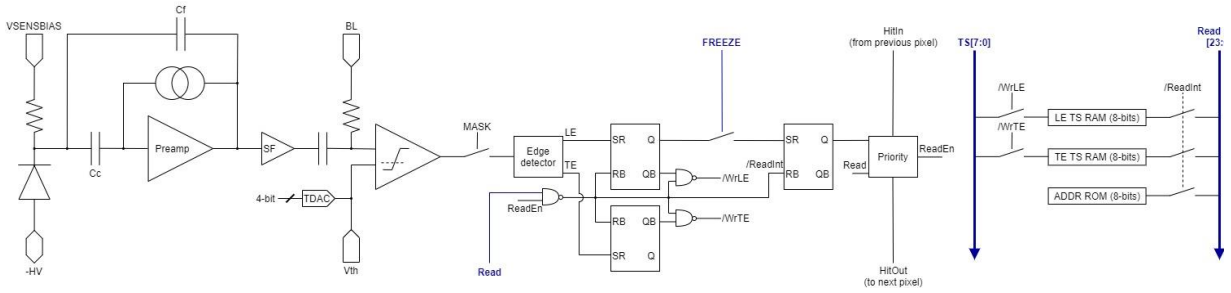


Fig. 2. Simplified schematic view of the RD50-MPW3 pixel including both the analogue and digital readout electronics.

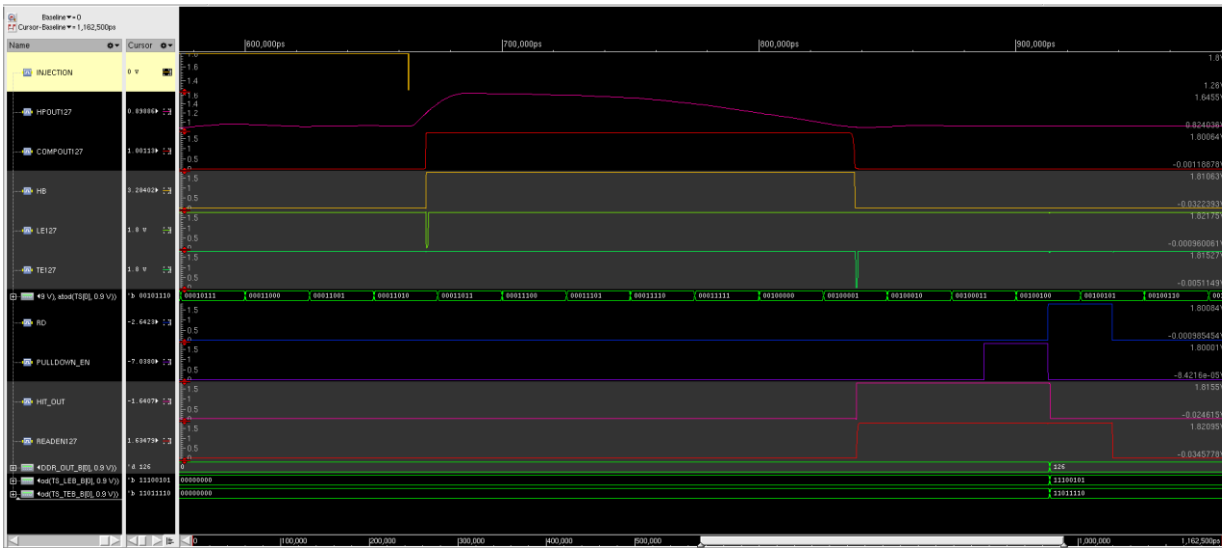


Fig. 3. Mixed-mode simulation using the post-layout view of a pixel: INJECTION is the test pulse from the calibration circuit; HPOUT the shaped signal at the comparator input; COMPOUT the comparator output; LE and TE the leading and trailing edges sensed by the edge detector; TS the time-stamp; RD and PULLDOWN_EN digital signals sent to the pixel to store the pixel address and time-stamps in the corresponding EOC; HIT_OUT the output of the priority circuit connected to the following pixel in the double column; and READEN the output of the priority circuit connected to the digital readout of the pixel. The last three waveforms correspond to the pixel address, and leading and trailing edge time-stamps.

together with the also new 8-bit SRAM shift register for serial configuration, alleviates the routing congestion and facilitates means to minimise the crosstalk noise. The double column scheme almost halves the number of necessary metal routing lines, as the pixels within a double column share most of the many metal routing lines they require. To enable that, the layout of the pixels is horizontally mirrored in every double column (i.e. analogue readout on one side and digital readout on the other side for one of the two columns, and vice versa for the other). To further prevent the generation of crosstalk noise, there is one metal routing line connected to ground between every two long metal routing lines that carry fast digital signals. The width of these metal lines, which are in metal 4, and the spacing between them is the minimum allowed by the design rules. The connections between the two pixels in a double pixel are in metal 3. To avoid noise coupling between the analogue and digital domains, the analogue and digital grounds are separated with a trench made of shallow n-well and deep n-isolation (called NISO in this process). The pixel size in RD50-MPW3 is 62 µm x 62 µm. This represents a small increase of the pixel size in RD50-MPW2 (60 µm x 60 µm), however it is necessary to accommodate all the new features here described while maintaining the breakdown voltage achieved in the previous prototype (8 µm spacing between the p-n electrodes of the diode for a 120 V breakdown voltage). Figure 4 shows the layout view of a double pixel. To avoid voltage drops in the power distribution, the pixel matrix incorporates a grid of wide metal lines in the highest possible metal layers (horizontal lines in metal 5, and vertical lines in metal 6). The metal grid is visible in the layout view of the double pixel. The pixels have four independent power supplies, as the various sub-circuits in each pixel are powered separately, in addition to two ground domains.

3.3. Peripheral electronics

The peripheral electronics, which configure the pixels and control the data readout, consist of new and optimised EOC circuits and a slow control system based on the I2C protocol for external communication using an internal Wishbone bus. There is one EOC circuit for every two double column of pixels. The EOCs use a First Input First Output (FIFO) memory to store, temporarily, the data generated by the pixels within a double column (i.e. leading and trailing edge time-stamps, and pixel address). This reduces the dead time, as pixels with hits are read out immediately as long as the FIFO is not full. The generated data is packed into frames, zero-suppressed and serialised at a maximum rate of 640 Mb/s over Low Voltage Differential Signal (LVDS) lines. To facilitate data

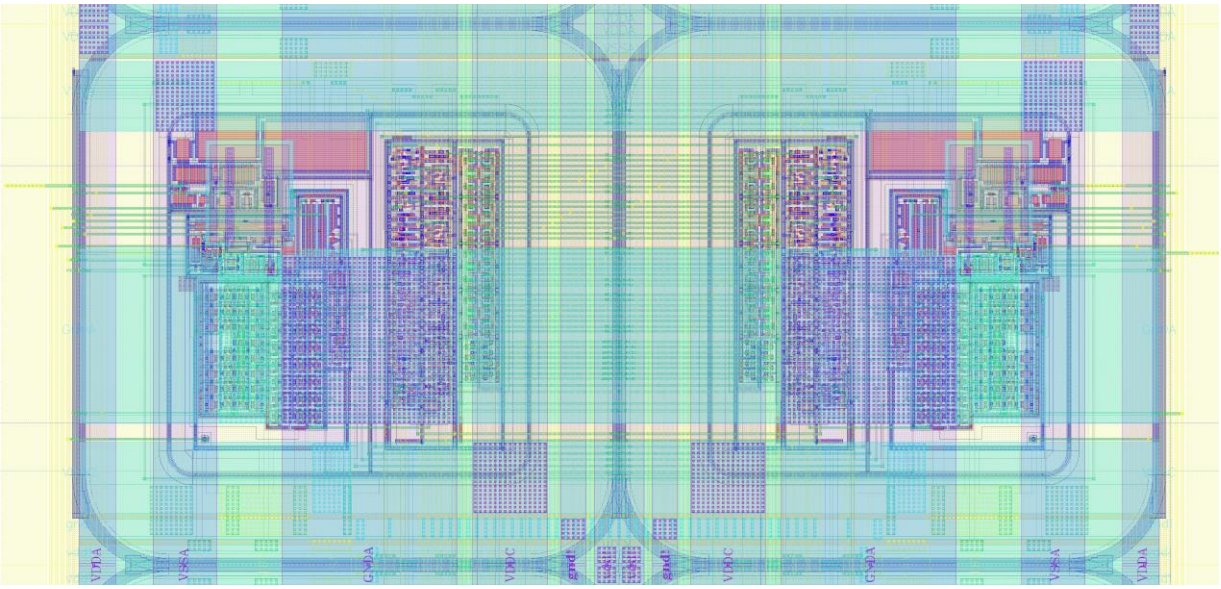


Fig. 4. Layout view of a double pixel. Explanations are given in the text.

transmission, the pixel matrix implements 8b/10b Aurora encoding. To assure fast and reliable synchronisation and communication with the readout FPGA, the chip sends an idle pattern when there is no data present. Figure 5 shows a block diagram of the peripheral readout electronics.

4. Conclusion

This paper describes work done by the CERN-RD50 collaboration to study and develop the RD50-MPW series of monolithic CMOS sensors in the 150 nm HV-CMOS process from LFoundry S.r.l. RD50-MPW2 has been designed and extensively evaluated both in the lab and also at proton and ion beam facilities. The leakage current of this prototype is 10^{-10} A/pixel (10^{-6} A/pixel in RD50-MPW1), the breakdown voltage 120 V (60 V in RD50-MPW1) and the time resolution less than 10 ns. The eTCT measurements show the depletion region is about 60 µm after irradiation to $2 \cdot 10^{15}$ n_{eq}/cm^2 and at 100 V substrate biasing (2.2 kΩ·cm nominal substrate resistivity), and the time resolution better than 10 ns after irradiation to $5 \cdot 10^{14}$ n_{eq}/cm^2 and also at 100 V (1.9 kΩ·cm nominal substrate resistivity). Test beam measurements show high beam energies produce analogue shaped outputs with smaller amplitudes, which indicates smaller energy deposition as expected, and also that the time-over-threshold has a distribution peaking at 35 ns matching simulated results. RD50-MPW3 is a more advanced prototype, with a matrix

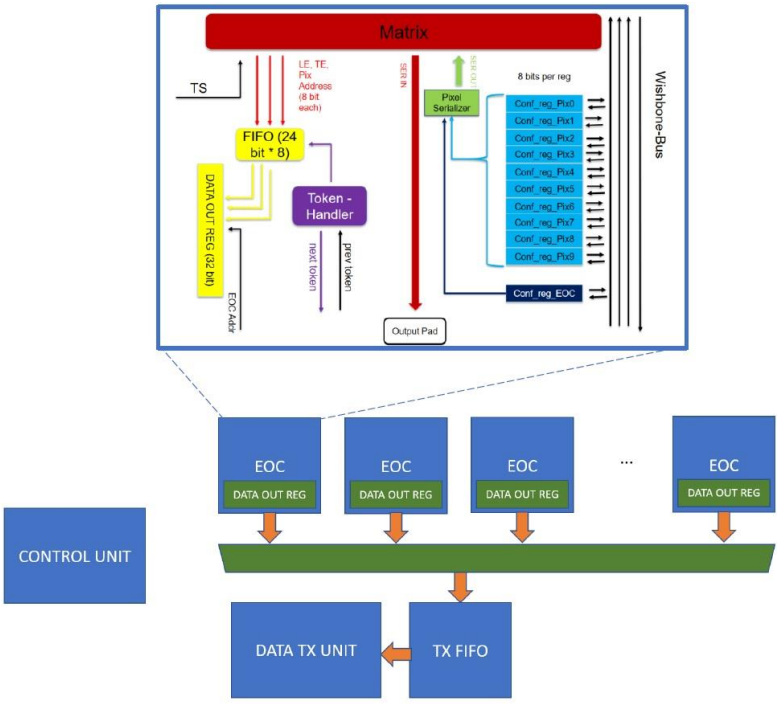


Fig. 5. Simplified block diagram of the peripheral readout electronics of RD50-MPW3.

of 64 x 64 pixels which integrate both analogue and digital readout electronics inside the sensing diodes, and optimised peripheral readout electronics for effective chip configuration and fast data transmission. This chip is currently being fabricated.

Acknowledgments

This work has been partly performed in the framework of the CERN-RD50 collaboration. It has received funding from UK Research and Innovation (UKRI) under the grant reference MR/S016449/1.

References

[1] E. Vilella, Recent depleted CMOS developments within the CERN-RD50 framework, PoS (Vertex2019) 019.

[2] R. Marco, Latest depleted CMOS sensor developments in the CERN-RD50 collaboration, JPS Conf. Proc. 34 010008 (2021).

[3] I. Peric et al., The FEI3 readout chip for the ATLAS pixel detector, Nucl. Instrum. Methods Phys. Res., Sect. A 565 (2006) 178.

[4] H. Liu et al., Development of a modular test system for the silicon sensor R&D of the ATLAS Upgrade, arXiv:1603.07950v4 [physics.ins-det].

[5] G. Kramberger et al., Investigation of irradiated silicon detectors by Edge-TCT, IEEE Trans. Nucl. Sci., Vol. 57 (2010) 2294.

[6] Particulars, Advanced measurement systems, Ltd. www.particulars.si

[7] J. Liu, Study of a monolithic pixel detector for the ATLAS tracker at the High Luminosity LHC, PhD thesis, Aix-Marseille University, Marseille, 2016.

[8] C. Zhang et al., Development of RD50-MPW2: a high-speed monolithic HV-CMOS prototype chip within the CERN-RD50 collaboration, PoS (TWEPP 2019) 045.

[9] B. Hiti et al., Characterisation of analogue front end and time walk in CMOS active pixel sensor, to be published in J. Instrum.13 (2021).

[10] S. Powell et al., The RD50-MPW2 High Voltage-CMOS sensor chip DAQ and preliminary testbeam results, submitted to J. Instrum. (2021).

[11] P. Sieberer et al., Readout system and testbeam results of the RD50-MPW2 HV-CMOS pixel chip, submitted to J. Phys. Conf. Ser. (2021).

[12] S. Ritt, Design and performance of the 6 GHz waveform digitizing chip DRS4, 2008 IEEE Nuclear Science Symposium Conference Record, 2008, pp. 1512-1515, doi: 10.1109/NSSMIC.2008.4774700.

Dr. Eva Vilella-Figueras
UKRI Research Fellow
The University of Liverpool
Department of Physics
Oliver Lodge Laboratory
Oxford Street
Liverpool L69 7ZE
T +44 (0) 151 794 9412
E vilella@hep.ph.liv.ac.uk

22nd November 2021

Cover letter

Dear VERTEX 2021 proceedings editor,

We have submitted our contribution entitled ***Development of High Voltage-CMOS sensors within the CERN-RD50 collaboration***, which we would like to publish in NIMA Proceedings. The paper presents results from the RD50-MPW series of monolithic CMOS sensor chips, developed by the CERN-RD50 collaboration to study this technology in view of the harsh requirements imposed by future hadron colliders on tracking systems. The paper gives an overview of the main design aspects and performance evaluation results of RD50-MPW1 and RD50-MPW2, and details the design of RD50-MPW3.

We hope the reviewers and you will find our article suitable for publication in NIMA Proceedings.

We look forward to hearing from you.

Sincerely,

Dr. Eva Vilella-Figueras

UKRI Research Fellow