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Development of High Voltage-CMOS sensors within the CERN-RD50 collaboration

--Manuscript Draft--

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Abstract:	This paper presents work done by the CERN-RD50 collaboration to develop and study monolithic CMOS sensors for future hadron colliders, especially in terms of radiation tolerance, time resolution and granularity. Currently CERN-RD50 is completing the performance evaluation of RD50-MPW2 and has recently submitted RD50-MPW3, the second and third prototype sensor chips designed by the collaboration. The paper gives an overview of the main design aspects and performance evaluation results of the first two prototype chips RD50-MPW1 and RD50-MPW2, and details the design of the latest prototype RD50-MPW3. RD50-MPW2 is a small prototype with an 8 x 8 matrix of active pixels which implement analogue readout electronics only and solutions for low leakage currents. This prototype has been evaluated in the laboratory and also at proton and ion beam facilities, before and after irradiation with neutrons up to 2•10 15 n eq /cm 2 . RD50-MPW3 is a more advanced prototype with a matrix of 64 x 64 pixels which integrate both analogue and digital readout electronics inside the sensing diodes. To alleviate routing congestion and minimise crosstalk noise, the pixels are serially configured and organised in a double column scheme. This prototype has optimised peripheral readout electronics for effective chip configuration, based on the I2C protocol, and fast data transmission.

15 February 2022

Prof. Daniela Bortoletto
Overseeing Editor
Nuclear Instruments and Methods in Physics Research, A

Dear Editor,

We have received your letter of 11 January 2022, informing us of the status of our manuscript "Development of High Voltage-CMOS sensors within the CERN-RD50 collaboration" (Ref. No.: NIMA_PROCEEDINGS-D-21-00007). We are thankful to the reviewer for their considerate and thoughtful comments of this submission. We have significantly revised the manuscript in all sections to address their comments and to improve clarity. We have also included additional data to address expressed concerns. We have reorganised the references. We have attached *a redlined version* of the revised manuscript for convenience, with text additions in red and removed text in red too but crossed, and *a standard all text in black version* as well. Next we respond to the comments made by the reviewer point by point.

Sincerely,

Dr. Eva Vilella-Figueras
UKRI Research Fellow
The University of Liverpool

Reviewer #1 had concerns and suggestions for improvement which we address here.

GENERAL COMMENTS

1) Scientific content of the paper:

1.1) HV-CMOS sensors feature large charge collecting electrodes which impact the achievable granularity; in comparison, small electrode sensors, which do not rely on HV, perform significantly better on this aspect. Moreover, the latter also achieve a radiation tolerance similar to the one mentioned in this paper. The motivation for developing HV-CMOS sensors does therefore not clearly appear in the paper; the latter would gain in relevance if the added value of the HV-CMOS approach would be (shortly) reminded to the reader.

Response: The *hit efficiency of HV-CMOS sensors neutron-irradiated up to a fluence of* $1 \cdot 10^{15}$ n_{eq}/cm^2 *is 99.7%* (see arXiv:1611.02669v3 [physics.ins-det] from M. Benoit et al.), whereas that of LV-CMOS sensors irradiated up to the same fluence is below the 99.5% requirement imposed by physics experiments (see e.g. MALTA monolithic Pixel sensors in TowerJazz 180 nm technology by C. Solans). The motivation of CERN-RD50 is to develop radiation hard semiconductor devices for very high luminosity colliders, where very high radiation levels are expected. We believe that, today, HV-CMOS sensors offer better radiation tolerance and are in the best position to fulfill the requirements of future hadron machines. Concerning granularity, in our programme within CERN-RD50 we have demonstrated that *very small pixels in HV-CMOS processes are possible (50 µm x 50 µm in RD50-MPW1 and similar sizes in subsequent sensor chips)* and other groups have achieved similar or even better results. In addition to all this, HV-CMOS sensors are fabricated in purely commercial processes without any modification as opposed to LV-CMOS sensors.

Action: The justification for developing HV-CMOS sensors is beyond the scope of the paper, and we prefer to avoid this kind of discussion.

1.2) No figure of the pixel thermal noise and of the picsel-to-picsel response dispersion, detection efficiency, a.s.o. is provided (e.g. from the MedAustron data taking); as a consequence, *the claim that the RD50-MPW2 prototype was "extensively" tested seems exaggerated*.

Response: RD50-MPW2 has a very small matrix with 8 x 8 active pixels only, and its very simple readout interface allows reading one pixel at a time only. In spite of these limitations, RD50-MPW2 has been as “extensively” tested as enabled by the features of the prototype. Details about the *laboratory evaluation* of this pixel chip are provided in *reference [10]*, such as *ToT distribution*, *threshold variation* and *noise* when using a test pulse to stimulate the pixels, as well as the *number of hits detected when using a Sr-90 radioactive source*. The main goal of the *test beams* conducted at the Rutherford and MedAustron facilities was to evaluate the experimental setups, newly developed

to enable synchronisation with other detectors and accept triggers, together with the sensor chip and a particle beam as well as to obtain initial measurement results. The *ToT measurements* obtained at these test beams are in good agreement with simulated results. The description of the setups and the results are in *reference [12]*. Since submission of the present manuscript, reference [12] has been made publicly available. The analysis of the ion test beam at the Zagreb Ruđer Bošković Institute is ongoing.

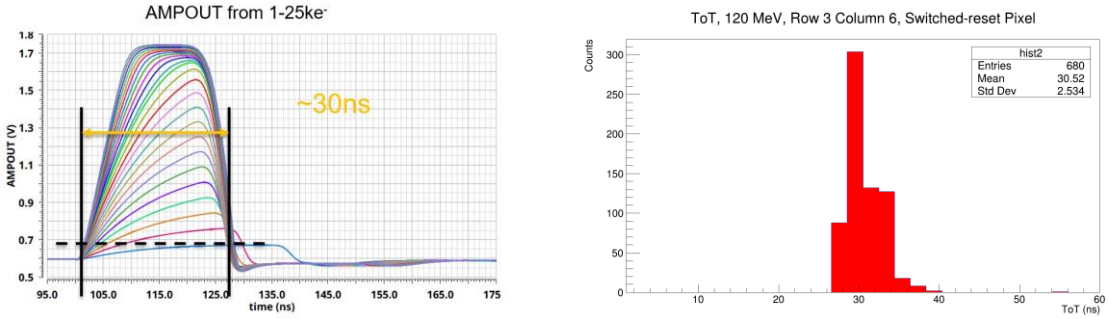
Action: To avoid confusion, we have removed the claim "extensively". The manuscript reads now "This prototype has been evaluated ~~extensively~~ in the laboratory and also at proton and ion beam facilities".

1.3) The paper shows no figure with *beam test results*. If space allows, a measured distribution expressing the tracking capability, e.g. T.o.T. distribution, would be useful.

Response: Section 2 reviews the main design aspects and experimental characterisation of the first two CMOS sensors developed by the collaboration, RD50-MPW1 and RD50-MPW2. The aim of this section is to give a snapshot of the status of the R&D work done by the collaboration on CMOS sensors so far, and to illustrate the background on which our current prototype, RD50-MPW3, lies. The experimental evaluation results given in this section have been published elsewhere, and the references are provided in the manuscript.

Action: We thank the reviewer for this suggestion. We have added one sentence at the very beginning of section 2 to stress the aim of this section, "This section reviews the main design aspects and performance evaluation results of RD50-MPW1 and RD50-MPW2 to illustrate the background on which the current prototype, RD50-MPW3, lies.". *We have rewritten the description of the test beam setups and results obtained to address the reviewer concerns*. As suggested, *we have added as well one figure with the ToT distribution measured at the Rutherford test beam*. Please see figure 2 in the manuscript and also below. This part of the manuscript now reads "The proton test beams have been conducted at the Rutherford Cancer Centre in Northumberland, United Kingdom, and MedAustron in Vienna, Austria [12], and the ion test beam at the Ruđer Bošković Institute in Zagreb, Croatia. The main goal of the proton test beams was to evaluate the experimental setups, newly developed to enable synchronisation with other detectors and accept triggers, together with the sensor chip and a particle beam as well as to obtain initial measurement results. Both setups consist of a telescope made of one RD50-MPW2 sample and the CaR DAQ placed between two scintillators. At the Rutherford setup the trigger is taken from the comparator output of the sensor chip, the two scintillators are used to discard noise events and the data generated by the amplified and discriminated outputs are recorded using a DRS4 switched capacitor array digitiser [13]. At the MedAustron setup the telescope is triggered by the coincidence of the two scintillators and the data

is recorded using a test beam firmware based on a First-In, First-Out (FIFO) memory that captures the Time-over-Threshold (ToT). Beam energies of 120 MeV (Rutherford) and 252.7 MeV (MedAustron) were used. The ToT was characterised at both test beams with the switched reset pixel flavour, for which a value around 30 ns is expected regardless of the charge collected by the pixel according to design simulations. While the switched reset pixel does not provide information about the signal amplitude, it was chosen for these measurements to validate the test beam setups. The measured ToT distribution peaks at 30 ns (Rutherford) and 35 ns (MedAustron). Figure 2 shows the simulation of the analogue pixel output, from which the simulated ToT was calculated, and the ToT distribution measured at Rutherford.". As mentioned before, the nature of RD50-MPW2 makes certain measurements very challenging. One example are tracking studies, as the very high statistics required to obtain reliable results with the one pixel only that can be measured at a time is in contradiction with the low maximum rate of the telescope used in the test beam. We expect to conduct detailed tracking studies with RD50-MPW3. To further improve the quality of the paper, *we have added one table that summarises the main measurement results of RD50-MPW2*, including test beam results. Please see table I in the manuscript and also below.



(a) **(b)**

Fig. 2. The simulation of the analogue output gives a ToT of about 30 ns (a) and ToT measurement results show a distribution peaking at 30 ns.

Table 1

Main performance parameters of RD50-MPW2. All the values are measured at 100 V substrate biasing with 1.9 kΩ·cm substrate resistivity samples (except were specified). CR stands for Continuous Reset pixel and SR for Switched Reset pixel. NC stands for Not Characterised.

Parameter	Value (before irradiation)	Value ($5 \cdot 10^{14}$ n_{eq}/cm^2, neutrons)	Value ($2 \cdot 10^{15}$ n_{eq}/cm^2, neutrons)
Breakdown voltage [V]	120	126[d]	136[e]
Leakage current [nA/pixel]	0.1	50[d]	60[e]
Depletion depth [µm][a]	110	90	60
ENC [e^-]	50	NC	NC
Time-walk (CR) [ns][b]	9	9	NC
ToT (CR) [ns][b]	110	120	NC
ToT (SR) [ns][c]	30	NC	NC

[a]Measured with a > 2 kΩ·cm sample. A depletion depth of 118 µm was measured with a 1.9 kΩ·cm RD50-MPW1 sample at a 100 V substrate biasing (estimated depletion depth from measurements, as breakdown voltage is around 56 V in this prototype).

[b]Measured at 200 e^- threshold voltage and 8 ke^- collected charge using an eTCT setup. Continuous reset pixels were chosen for this study as the comparator output signal scales with the signal size and can be used to measure the amount of input charge.

[c]Measured at proton test beams. Switched reset pixels were chosen as these have higher gain than continuous reset pixels.

[d]Measured after irradiation to $1 \cdot 10^{14}$ n_{eq}/cm^2. The values after $5 \cdot 10^{14}$ n_{eq}/cm^2 are expected to be very similar.

[e]Measured after irradiation to $1 \cdot 10^{15}$ n_{eq}/cm^2. The values after $2 \cdot 10^{15}$ n_{eq}/cm^2 are expected to be very similar.

2) Presentation of the paper:

We have corrected the faults of English as suggested. Below we provide answers to those comments that we thought required clarification.

DETAILED COMMENTS

Section 2:

2.1) l.46 "... with the literature." --> "... with those found in the literature [REF ???]" ==> This sentence is very vague, poorly informative; *some reference(s) may be useful*

Response: We thank the reviewer for pointing this out. We did not include any *references* in the original manuscript because they were not yet available at submission, but *have been published since*.

Action: We have added reference [7] to our manuscript.

[7] I. Mandić et al., Study of neutron irradiation effects in Depleted CMOS structures, arXiv:2112.10738v1 [physics.ins-det].

2.2) l.63 to l.66: the text is twice a bit confusing: two different fluence and resistivity values are mentioned, which have no obvious justifications:

-) l.65 The fluence for which the time resolution is provided (5.10^14 neq/cm²) is 4 times smaller than the "nominal" value of 2.10^15 announced earlier in the text: why ? What happens with the time resolution for the nominal fluence ?

-) l.64 and 65: two different measured values of the resistivity are provided, apparently for the same substrate; does it reflect non-uniformities in the substrate resistivity ? How well is the resistivity known ?

Response: RD50-MPW2 samples *in all the four resistivity substrates* in which this sensor chip was fabricated *(10 Ω·cm, 0.5 – 1.1 kΩ·cm, 1.9 kΩ·cm and > 2 kΩ·cm)* were irradiated with neutrons from *1·10^{13} n$_{eq}$/cm^2 to 2·10^{15} n$_{eq}$/cm^2 fluence in 6 different steps* (1·10^{13}, 3·10^{13}, 2·10^{14}, 5·10^{14}, 1·10^{15} and 2·10^{15} n$_{eq}$/cm^2). The large number of irradiated samples were distributed to several RD50 institutes for evaluation. *The measurements were done based on availability of samples and instrumentation at the RD50 institutes*. For the *depletion depth*, characterised using the *small matrix of passive pixels* also integrated in this chip, *0.5 – 1.1 kΩ·cm and > 2 kΩ·cm samples irradiated to all the 6 steps* and an eTCT setup available at Ljubljana were used. Although the depletion depth in the 1.9 kΩ·cm resistivity was not characterised for RD50-MPW2 samples, it had been studied already using RD50-MPW1 samples fabricated in the same 1.9 kΩ·cm resistivity. Please see reference [7] for the details. For the *time-walk*, characterised with the *8 x 8 matrix of active pixels*, a *one 1.9 kΩ·cm sample irradiated to 5·10^{14} n$_{eq}$/cm^2* and eTCT setup at Ljubljana were used.

Action: We thank the reviewer for this comment and agree that the original text was confusing. As explained before, we have added one sentence to clarify that RD50-MPW2 was fabricated in a few different substrate resistivities "RD50-MPW2 was fabricated in the standard resistivity of 10 Ω·cm and in three high resistivity substrates with nominal values of 500 Ω·cm – 1.1 kΩ, 1.9 kΩ·cm and > 2 kΩ·cm.". We have rewritten much of the explanation about the depletion depth and time-walk measurements. It now reads "The eTCT measurements showed the depletion depth is 110 µm, while the time-walk is better than 10 ns at 200 e$^-$ threshold voltage and from 2 ke$^-$ collected charge and above. Both parameters were measured at 100 V substrate biasing and before irradiation. After irradiation to 5·10^{14} n$_{eq}$/cm^2 the depletion depth is 90 µm and the time-walk is kept at approximately the same value as before irradiation. After irradiation to 2·10^{15} n$_{eq}$/cm^2, the depletion depth~~region~~ is 60 µm.". We have updated the Conclusion section as well.

2.3) l.71 "... for coincide measurements ..." ==> The sentence has syntax weaknesses and is unclear: *which measurements should be coinciding*

Response: We appreciate the sentence in the original manuscript was not clear enough. *Please see the answer to point 1.3)*.

2.4) l.73 "High beam energies ..." ==> To which energies does the text refer ?

Response: We have made progress with the analysis of the test beam data since the submission of the first version of the present manuscript. We have shifted the focus of our analysis to *ToT measurements*. *Please see the answer to point 1.3)*.

Section 3:

2.5) l.98 "... that referees the ..." ==> NOT CLEAR

Response: The priority circuit determines the order in which hits within a double column are read out. The criteria for that order was implemented at design stage. The priority circuit works as a "referee".

Action: We thank the reviewer for pointing out this is confusing. *We have replaced the word "referees" for "determines"*. We hope this is clearer.

2.6) l.106 Which *satisfactory performances* is the text refering to ? compared to ?

Response: The performance of RD50-MPW2 is satisfactory as *it meets the goals we wanted to achieve with this prototype*, which are to improve the current-to-voltage characteristics we saw in RD50-MPW1 and to have an active pixel matrix that implements these improvements.

Action: We thank reviewer for this observation. We have rephrased the original text "… as the lab and test beam evaluations concluded their performance is satisfactory" as "… as the laboratory and test beam evaluations showed~~concluded~~ their performance matches design specifications~~is satisfactory~~".

2.7) Caption of fig.3: "... edge detector ..." --> not defined

Response: This is obviously a mistake and we thank the reviewer for noting this. The edge detector is typically used in the first stage of the FE-I3 style digital readout electronics to sense the rising and falling edges of the comparator. Other electronics later assign time-stamps to these edges.

Action: We have improved the figure caption from the original "LE and TE the leading and trailing edges sensed by the edge detector" to "LE and TE the leading and trailing edges sensed by the digital readout electronics~~edge detector~~". We hope this clarifies things.

Section 4: Conclusion

2.8) l.143 "... RD50-MPW2 has been ... extensively evaluated ..." ==> Such a statement calls for more information than provided in this paper, e.g. figures of merit in terms of pixel noise, pixel-to-pixel dispersions, etc., are missing to support the statement as it is formulated.

Response: *Please see our answer to point 1.2)*.

2.9) l.145 - 148 "The eTCT ... resistivity)." ==> The sentence calls for clarification, (see comments of l.63 - 66)

Response: *Please see our answer to point 2.2)*.

Development of High Voltage-CMOS sensors within the CERN-RD50 collaboration

E. Vilella[a,*], on behalf of the CERN-RD50 collaboration

[a] *The University of Liverpool, Department of Physics, Liverpool L69 7ZE, UK*

Abstract

This paper presents work done by the CERN-RD50 collaboration to develop and study monolithic CMOS sensors for future hadron colliders, especially in terms of radiation tolerance, time resolution and granularity. Currently CERN-RD50 is completing the performance evaluation of RD50-MPW2 and has recently submitted~~the design of~~ RD50-MPW3, the second and third prototype sensor chips designed by the collaboration. The paper gives an overview of the main design aspects and performance evaluation results of the first two prototype chips RD50-MPW1 and RD50-MPW2, and details the design of the latest prototype RD50-MPW3. RD50-MPW2 is a small prototype with an 8 x 8 matrix of active pixels which implement analogue readout electronics only and solutions for low leakage currents. This prototype has been evaluated ~~extensively~~ in the laboratory and also at proton and ion beam facilities, before and after irradiation with neutrons up to $2 \cdot 10^{15}$ n_{eq}/cm^2. RD50-MPW3 is a more advanced prototype with a matrix of 64 x 64 pixels which integrate both analogue and digital readout electronics inside the sensing diodes. To alleviate routing congestion and minimise crosstalk noise, the pixels are serially configured and organised in a double

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column scheme. This prototype has optimised peripheral readout electronics for effective chip configuration, based on the I2C protocol, and fast data transmission.

Keywords: CERN-RD50, depleted monolithic active pixel sensor, future hadron colliders, high voltage-CMOS technology, high voltage pixel detector, monolithic CMOS detector.

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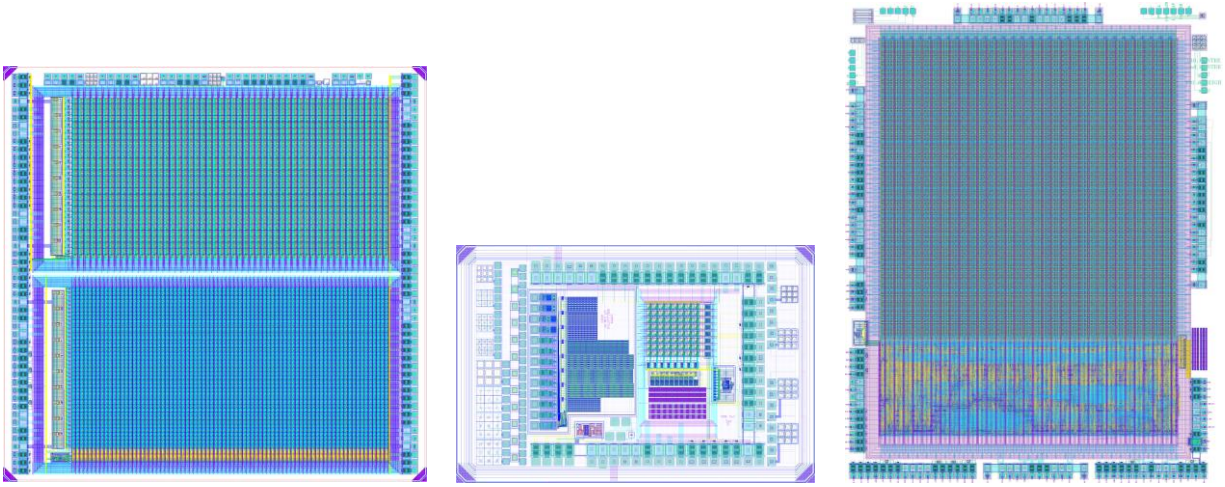
1. Introduction

This paper presents results from the RD50-MPW series of monolithic CMOS sensors, developed by the CERN-RD50 collaboration to study this technology in view of the harsh requirements imposed by future hadron colliders on tracking systems [1~~, 2~~]. The RD50-MPW sensors developed so far are in the 150 nm High Voltage-CMOS (HV-CMOS) process from LFoundry S.r.l. Parameters especially considered in this programme are radiation tolerance, time resolution and granularity.

2. Design and characterisation of RD50-MPW1 and RD50-MPW2~~Overview of monolithic CMOS sensors with CERN-RD50~~

This section reviews the main design aspects and performance evaluation results of RD50-MPW1 and RD50-MPW2 to illustrate the background on which our current prototype, RD50-MPW3, lies. Figure 1 shows the layout views of these three sensor chips. RD50-MPW1 has a matrix of 40 rows x 78 columns of high-granularity pixels where these integrate the analogue and digital readout electronics inside their area of 50 µm x 50 µm. The analogue readout, based on conventional electronics for charge-collecting detectors, includes a Charge Sensitive Amplifier (CSA) with continuous reset, low-pass and high-pass filters, and a CMOS comparator with a 4-bit Digital-to-Analogue Converter (DAC) to tune locally small threshold voltage variations. The digital readout is based on the well-known column drain architecture (i.e. FE-I3 style) [2~~3~~]. It provides two 8-bit time-stamps, one for the leading edge and another one for the trailing edge, and an 8-bit address. When a pixel registers an event, it sends the leading



(a) **(b)** **(c)**

Fig. 1. Layout views of RD50-MPW1 (a), RD50-MPW2 (b) and RD50-MPW3 (c). The dimensions of these prototype sensor chips are 5 mm x 5 mm, 3.2 mm x 2.1 mm and 5.1 mm x 6.6 mm respectively.

and trailing edge time-stamps, and its address, to the corresponding End-Of-Column (EOC) circuit at the periphery through a 24-bit bus. This bus is shared by all the pixels within a column. The 78 EOC circuits of the matrix, which function as two 16-bit parallel-in parallel-out shift-registers, are connected to two readout serialisers designed to run at a maximum speed of 640 MHz. RD50-MPW1 was fabricated in two high resistivity substrates with nominal values of 500 Ω·cm – 1.1 kΩ·cm and 1.9 kΩ·cm.

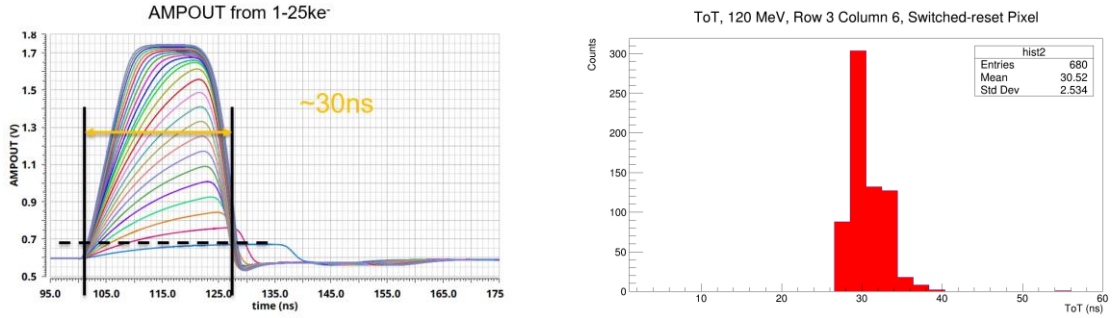
The Data Acquisition System (DAQ) for the RD50-MPW sensor chips builds on the general-purpose Control and Readout (CaR) board [34]. It comprises a dedicated chip carrier board, the CaR board, an FPGA Mezzanine Card (FMC) and a Xilinx ZC706 or ZC702 evaluation board. The evaluation of fabricated RD50-MPW1 samples has revealed this chip essentially works, but also that it suffers from high leakage current in the sensing diodes, voltage drops across the pixel matrix and crosstalk noise between the lines that carry digital signals [4]. Several RD50-MPW1 samples have been irradiated with neutrons up to $2 \cdot 10^{15}$ n_{eq}/cm^2 at the TRIGA reactor in Ljubljana, Slovenia. The test structures of this chip, which consist of a small matrix of passive pixels, have been evaluated with the edge Transient Current Technique (eTCT) using the Particulars measurement system [5, 6]. The measurement~~measured~~ results show the irradiation effects are compatible with those found in the literature [7].

RD50-MPW2, the successor chip, implements solutions to~~that~~ minimise the high leakage current observed in RD50-MPW1 and has a simple pixel matrix to test these. The solutions consist of a guard ring frame at the edge of

the chip and the prevention of certain post-processing filling layers that involve conductive material. The guard ring frame has one n-type ring that acts as a current collecting ring and six p-type rings that control the termination of the lateral depletion of the sensing diodes, in addition to one p-type seal ring that protects the design from damage caused by the sawing process [8]. RD50-MPW1 has the p-type seal ring only. The matrix in RD50-MPW2 has 8 rows x 8 columns of 60 µm x 60 µm pixels with analogue readout only. The larger pixel size is due to the increase of the spacing between the p-n electrodes of the diode for a higher breakdown voltage (8 µm spacing in RD50-MPW2 as opposed to 3 µm spacing in RD50-MPW1). The matrix integrates two different flavours of readout electronics, with continuous and switched reset CSAs, optimised for short~~fast~~ response times to resolve particles at high rates [9]. RD50-MPW2 was fabricated in the standard resistivity of 10 Ω·cm and in three high resistivity substrates with nominal values of 500 Ω·cm – 1.1 kΩ, 1.9 kΩ·cm and > 2 kΩ·cm.

RD50-MPW2 has been evaluated in the laboratory and also at proton and ion beam facilities. The prototype exhibited a leakage current of ~~this prototype is 10^{-10}~~100 pA/pixel (~~10^{-6}~~1 µA/pixel in RD50-MPW1), ~~a~~the breakdown voltage of 120 V (56 V in RD50-MPW1) and an Equivalent Noise Charge (ENC) better than 2 mV [10]. Given the capacitance of 2.8 fF of the calibration circuit for injecting a test charge into the amplifier, the ENC is therefore better than 50 e^-~~and the time resolution less than 10 ns~~. The eTCT setup has been used to study the depletion depth~~region~~ of the test structures, ~~also~~ integrated in RD50-MPW2 as a small matrix of passive pixels, after irradiation with neutrons to several fluence up to $2 \cdot 10^{15}$ n_{eq}/cm^2 [7]. The ~~eTCT~~ setup was also~~has also been~~ used, for the first time, to investigate the time-walk~~time resolution~~ of the ~~active pixels in the~~ 8 x 8 active pixel matrix [11]. The eTCT measurements showed the depletion depth is 110 µm, while the time-walk is better than 10 ns at 200 e^- threshold voltage and from 2 ke^- collected charge and above. Both parameters were measured at 100 V substrate biasing and before irradiation. After irradiation to $5 \cdot 10^{14}$ n_{eq}/cm^2 the depletion depth is 90 µm and the time-walk is kept at approximately the same value as before irradiation. After irradiation to $2 \cdot 10^{15}$ n_{eq}/cm^2, the depletion depth~~region~~ is 60 µm.~~about 60 µm after irradiation to $2 \cdot 10^{15}$ n_{eq}/cm^2 and at 100 V substrate biasing (2.2 kΩ·cm nominal substrate resistivity), and the time resolution better than 10 ns after irradiation to $5 \cdot 10^{14}$ n_{eq}/cm^2 and also at 100 V (1.9 kΩ·cm nominal substrate resistivity).~~ The proton test beams have been conducted at the Rutherford Cancer Centre in Northumberland, United Kingdom, and MedAustron in Vienna, Austria [12], and the ion test beam at the Ruđer Bošković Institute in Zagreb, Croatia. The main goal of the proton test beams was to evaluate the experimental setups,

newly developed to enable synchronisation with other detectors and accept triggers, together with the sensor chip and a particle beam as well as to obtain initial measurement results. Both setups consist of a telescope made of one RD50-MPW2 sample and the CaR DAQ placed between two scintillators. At the Rutherford setup the trigger is taken from the comparator output of the sensor chip, the two scintillators are used to discard noise events and the data generated by the amplified and discriminated outputs are recorded using a DRS4 switched capacitor array digitiser [13]. At the MedAustron setup the telescope is triggered by the coincidence of the two scintillators and the data is recorded using a test beam firmware based on a First-In, First-Out (FIFO) memory that captures the Time-over-Threshold (ToT). Beam energies of 120 MeV (Rutherford) and 252.7 MeV (MedAustron) were used. The ToT was characterised at both test beams with the switched reset pixel flavour, for which a value around 30 ns is expected regardless of the charge collected by the pixel according to design simulations. While the switched reset pixel does not provide information about the signal amplitude, it was chosen for these measurements to validate the test beam setups. The measured ToT distribution peaks at 30 ns (Rutherford) and 35 ns (MedAustron). Figure 2 shows the simulation of the analogue pixel output, from which the simulated ToT was calculated, and the ToT distribution measured at Rutherford. ~~The test beam at the Northumberland Rutherford Cancer Centre focused on studying the analogue shaped output at different beam energies, while the test beam at Vienna MedAustron aimed at developing a beam telescope to test the tracking capability of RD50-MPW2. The experimental setup at Northumberland included, in addition to the CaR DAQ, scintillator triggers for coincide measurements. The data generated by the analogue shaped output was recorded for each event using a DRS4 switched capacitor array digitiser [12]. Proton beam energies between 70 and 229 MeV were used in this study. High beam energies produced analogue shaped outputs with smaller amplitudes, which indicates smaller energy deposition as expected. The telescope developed for the Vienna test beam comprises one RD50-MPW2 sample and CaR DAQ placed in the middle of two arms with two double sided silicon strip detectors each, and two scintillators at the very back of the setup. The telescope is triggered by the coincidence of the two scintillators. A new firmware was prepared to allow the synchronization of RD50-MPW2 with the other detectors of the telescope and the capability of accepting trigger signals. Time-over-threshold measurements taken in this test beam show a distribution peaking at 35 ns and are in good agreement with simulated results.~~The analysis of the ion test beam at the Zagreb Ruđer Bošković Institute is ongoing. Table 1 summarises the main performance parameters of RD50-MPW2.



(a) **(b)**

Fig. 2. The simulation of the analogue output gives a ToT of about 30 ns (a) and ToT measurement results show a distribution peaking at 30 ns.

In spite of its success RD50-MPW2 has several design limitations, such as the small number of rows and columns of the pixel matrix, the lack of digital readout electronics to identify events and a very simple peripheral readout that makes certain types of measurements too slow or not possible. To give a specific example of the consequences of these limitations, in RD50-MPW2 only one pixel at a time can be read out and this has restricted its~~the~~ evaluation programme. The collaboration is currently~~CERN RD50 is~~ developing a new prototype, RD50-MPW3, which integrates a larger and more advanced pixel matrix with new and optimised peripheral readout electronics to further study monolithic CMOS sensors. ~~Figure 1 shows the layout views of the RD50-MPW monolithic CMOS sensors.~~

3. Design of RD50-MPW3 ~~design~~

RD50-MPW3 overcomes the limitations of RD50-MPW2 by extending the number of pixels in the matrix (64 columns x 64 rows), incorporating in the pixel area digital readout electronics based on the column drain architecture and adding optimised peripheral readout electronics for effective pixel configuration and fast data transmission. RD50-MPW3 includes as well a few dedicated test structures, mostly to characterise the diode current-to-voltage characteristics~~I-V~~, depletion depth~~region~~ and parasitic capacitance. RD50-MPW3 is being fabricated in three different substrate resistivities, which are the standard resistivity (10 Ω·cm) and two high resistivities of 1.9 kΩ·cm and 3 kΩ·cm.

Table 1

Main performance parameters of RD50-MPW2. All the values are measured at 100 V substrate biasing with 1.9 kΩ·cm substrate resistivity samples (except were specified). CR stands for Continuous Reset pixel and SR for Switched Reset pixel. NC stands for Not Characterised.

Parameter	Value (before irradiation)	Value ($5 \cdot 10^{14}$ n_{eq}/cm^2, neutrons)	Value ($2 \cdot 10^{15}$ n_{eq}/cm^2, neutrons)
Breakdown voltage [V]	120	126[d]	136[e]
Leakage current [nA/pixel]	0.1	50[d]	60[e]
Depletion depth [µm][a]	110	90	60
ENC [e^-]	50	NC	NC
Time-walk (CR) [ns][b]	9	9	NC
ToT (CR) [ns][b]	110	120	NC
ToT (SR) [ns][c]	30	NC	NC

[a]Measured with a > 2 kΩ·cm sample. A depletion depth of 118 µm was measured with a 1.9 kΩ·cm RD50-MPW1 sample at a 100 V substrate biasing (estimated depletion depth from measurements, as breakdown voltage is around 56 V in this prototype).

[b]Measured at 200 e^- threshold voltage and 8 ke^- collected charge using an eTCT setup. Continuous reset pixels were chosen for this study as the comparator output signal scales with the signal size and can be used to measure the amount of input charge.

[c]Measured at proton test beams. Switched reset pixels were chosen as these have higher gain than continuous reset pixels.

[d]Measured after irradiation to $1 \cdot 10^{14}$ n_{eq}/cm^2. The values after $5 \cdot 10^{14}$ n_{eq}/cm^2 are expected to be very similar.

[e]Measured after irradiation to $1 \cdot 10^{15}$ n_{eq}/cm^2. The values after $2 \cdot 10^{15}$ n_{eq}/cm^2 are expected to be very similar.

3.1. Pixel electronics

The RD50-MPW3 in-pixel digital readout is a highly improved version of that developed for RD50-MPW1. It incorporates logic to mask noisy pixels, replaces the priority circuit that determines~~referees~~ the order in which hits are read out for a more compact~~less area consuming~~ alternative based on an OR chain, and allows pausing the digitisation of new hits until the readout of a column is complete. Each pixel contains as well a new 8-bit SRAM shift register, which enables serial configuration and stores a per pixel-trimming to compensate ~~for~~ threshold voltage variations (four bits), a flag to mask noisy pixels (one bit), and data to enable or disable the calibration circuit (one bit), the amplifier output monitor (one bit) and the comparator output monitor (one bit). The configuration shift

registers are programmed during the chip initialisation and hold the values indefinitely until the chip is reprogrammed or powered down. The analogue readout electronics reuse those developed for the continuous reset pixel of RD50-MPW2, as the laboratory and test beam evaluations showed~~concluded~~ their performance matches design specifications~~is satisfactory~~. Details about the diode implementation are available in [~~41~~]. Figure ~~32~~ shows a simplified version of the pixel schematic. Figure ~~43~~ shows a mixed-mode simulation using the post-layout view of a pixel that receives a test pulse from the calibration circuit.

3.2. Double pixel scheme

RD50-MPW3 implements a double column scheme for the first time in the RD50-MPW prototypes, which together with the also new 8-bit SRAM shift register for serial configuration, alleviates the routing congestion and facilitates means to minimise the crosstalk noise. Most of the routing area is occupied by a 24-bit bus with 8-bit Gray encoded time-stamps of the leading and trailing edges of the discriminator output as well the 8-bit address of the pixel. The double column scheme almost halves the number of necessary metal routing lines, as the pixels within a double column share most of the many metal routing lines they require. To enable that, the layout of the pixels is horizontally mirrored in every double column (i.e. analogue readout on one side and digital readout on the other side for one of the two columns, and vice versa for the other). To further prevent the generation of crosstalk noise, there is one metal routing line connected to ground between every two long metal routing lines that carry fast digital signals. The width of these metal lines, which are in metal 4, and the spacing between them is the minimum allowed by the design rules. The connections between the two pixels in a double pixel are in metal 3. To avoid noise coupling between the analogue and digital domains, the analogue and digital grounds are separated with a trench made of shallow n-well and deep n-isolation (called NISO in this process). The pixel size in RD50-MPW3 is 62 µm x 62 µm. This represents a small increase of the pixel size in RD50-MPW2 (60 µm x 60 µm), however it is necessary to accommodate all the new features here described while maintaining the breakdown voltage achieved in the previous prototype (8 µm spacing between the p-n electrodes of the diode for a 120 V breakdown voltage). Figure ~~54~~ shows the layout view of a double pixel. To avoid voltage drops in the power distribution, the pixel matrix incorporates a grid of wide metal lines in the highest possible metal layers (horizontal lines in metal 5, and vertical lines in metal

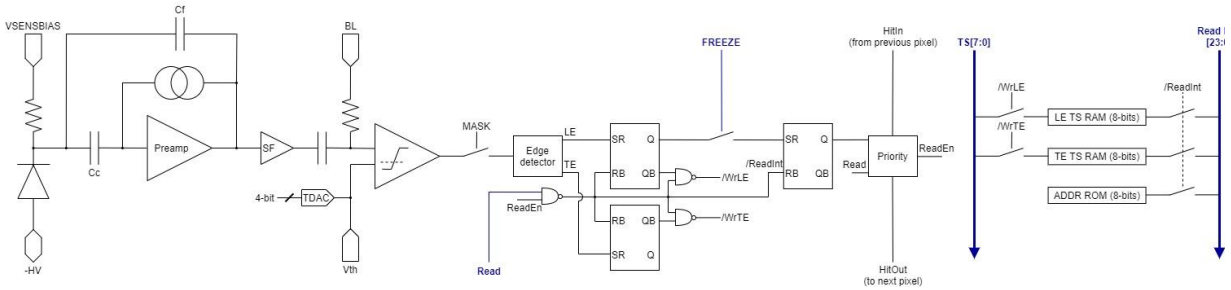


Fig. 32. Simplified schematic view of the RD50-MPW3 pixel including both the analogue and digital readout electronics.

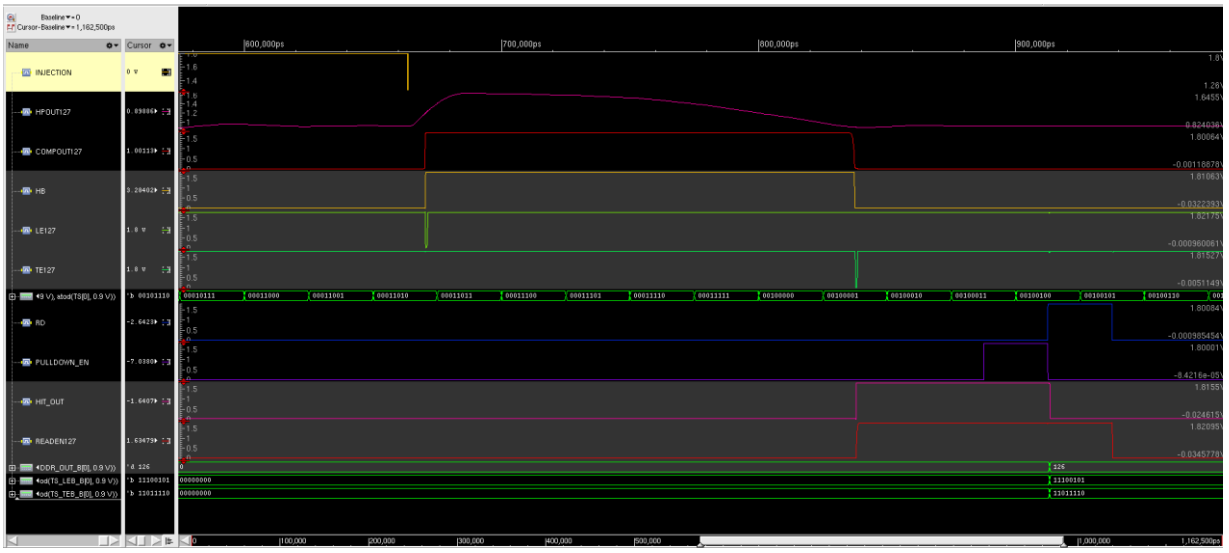


Fig. 43. Mixed-mode simulation using the post-layout view of a pixel: INJECTION is the test pulse from the calibration circuit; HPOUT the shaped signal at the comparator input; COMPOUT the comparator output; LE and TE the leading and trailing edges sensed by the digital readout electronics~~edge detector~~; TS the time-stamp; RD and PULLDOWN_EN digital signals sent to the pixel to store the pixel address and time-stamps in the corresponding EOC; HIT_OUT the output of the priority circuit connected to the following pixel in the double column; and READEN the output of the priority circuit connected to the digital readout of the pixel. The last three waveforms correspond to the pixel address, and leading and trailing edge time-stamps.

6). The metal grid is visible in the layout view of the double pixel. The pixels have four independent power domains~~supplies~~, as the various sub-circuits in each pixel are powered separately, in addition to two ground domains.

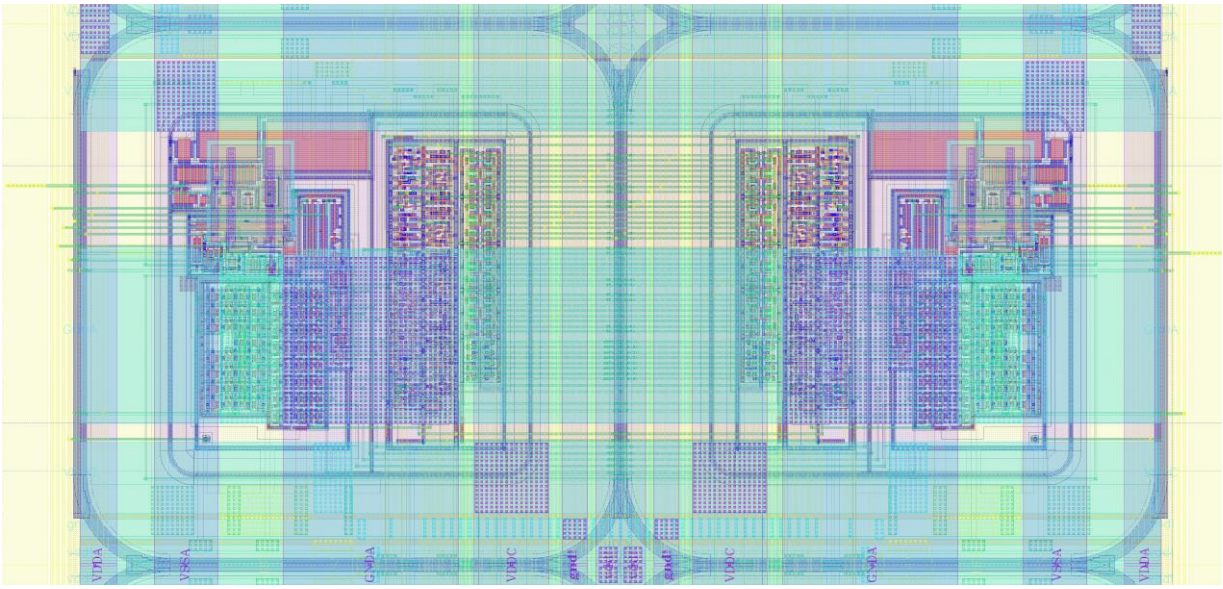


Fig. 54. Layout view of a double pixel. Explanations are given in the text.

3.3. Peripheral electronics

The peripheral electronics, which configure the pixels and control the data readout, consist of new and optimised EOC circuits, a Control Unit (CU) and a slow control system based on the I2C protocol for external communication using an internal Wishbone bus. There is one EOC circuit for every two double column of pixels. The EOCs are handled by the CU. They use a ~~First Input First Output (~~FIFO~~)~~ memory to store, temporarily, the data generated by the pixels within a double column (i.e. leading and trailing edge time-stamps, and pixel address). This reduces the dead time, as pixels with hits are read out immediately as long as the FIFO is not full. The generated data is packed into frames, zero-suppressed and serialised at a maximum rate of 640 Mb/s, by a data transmission unit over Low Voltage Differential Signal (LVDS) lines. ~~To facilitate data transmission, the pixel matrix implements 8b/10b Aurora encoding. To assure fast and reliable synchronisation and communication with the readout FPGA, the chip sends an idle pattern when there is no data present.~~ The readout of the pixel matrix is triggerless. All the peripheral blocks are configured through Control Status Registers (CSRs), which are connected to a Wishbone bus and read/written using an I2C interface. Figure ~~65~~ shows a block diagram of the peripheral readout electronics.

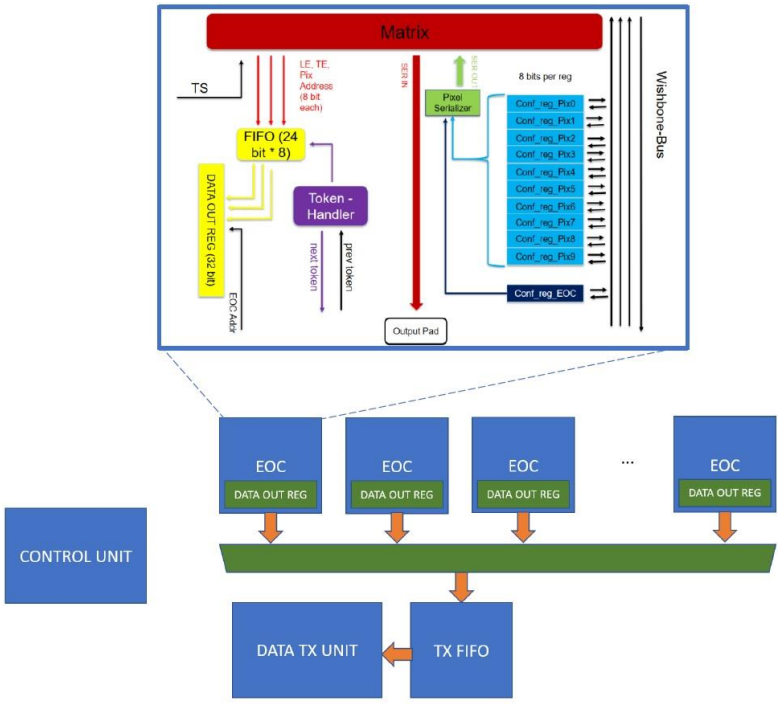


Fig. ~~65~~. Simplified block diagram of the peripheral readout electronics of RD50-MPW3.

4. Conclusion

This paper describes work done by the CERN-RD50 collaboration to study and develop the RD50-MPW series of monolithic CMOS sensors in the 150 nm HV-CMOS process from LFoundry S.r.l. RD50-MPW2 has been designed and ~~extensively~~ evaluated both in the laboratory and also at proton and ion beam facilities. The prototype exhibited a leakage current of ~~this prototype is 10^{-10}~~100 pA/pixel ~~(10^{-6} 1 µA/pixel in RD50-MPW1)~~, ~~a~~the breakdown voltage of 120 V ~~(56 V in RD50-MPW1)~~ and an Equivalent Noise Charge (ENC) better than 50 e^-. The eTCT measurements showed the depletion depth is 110 µm, and the time-walk is better than 10 ns at 200 e^- threshold voltage and from 2 ke^- collected charge and above. After irradiation to $5 \cdot 10^{14}$ n_{eq}/cm^2 the depletion depth is 90 µm and the time-walk is kept at approximately the same value as before irradiation. After irradiation to $2 \cdot 10^{15}$ n_{eq}/cm^2, the depletion depth~~region~~ is 60 µm.~~show the depletion region is about 60 µm after irradiation to $2 \cdot 10^{15}$ n_{eq}/cm^2 and at 100 V substrate biasing (2.2 kΩ·cm nominal substrate resistivity), and the time resolution better than 10 ns after irradiation to $5 \cdot 10^{14}$ n_{eq}/cm^2 and also at 100 V (1.9 kΩ·cm nominal substrate resistivity)~~. The test beam measurement results

show a ToT distribution peaking around 30 ns and are in good agreement with simulated results. ~~Test beam measurements show high beam energies produce analogue shaped outputs with smaller amplitudes, which indicates smaller energy deposition as expected, and also that the time-over-threshold has a distribution peaking at 35 ns matching simulated results.~~ RD50-MPW3 is a more advanced prototype, with a matrix of 64 x 64 pixels which integrate both analogue and digital readout electronics inside the sensing diodes, and optimised peripheral readout electronics for effective chip configuration and fast data transmission. This chip is currently being fabricated.

Acknowledgments

This work has been partly performed in the framework of the CERN-RD50 collaboration. It has received funding from UK Research and Innovation (UKRI) under the grant reference MR/S016449/1, and from the European Union's Horizon 2020 Research and Innovation programme under grant agreement 101004761 (AIDAinnova).

References

[1] M. Benedikt et al., Future Circular Collider, Vol. 3: The Hadron Collider (FCC-hh), CERN-ACC-2018-0058 (2018).

[2] I. Peric et al., The FEI3 readout chip for the ATLAS pixel detector, Nucl. Instrum. Methods Phys. Res., Sect. A 565 (2006) 178.

[3] H. Liu et al., Development of a modular test system for the silicon sensor R&D of the ATLAS Upgrade, arXiv:1603.07950v4 [physics.ins-det].

[4] E. Vilella, Recent depleted CMOS developments within the CERN-RD50 framework, PoS (Vertex2019) 019.

[5] G. Kramberger et al., Investigation of irradiated silicon detectors by Edge-TCT, IEEE Trans. Nucl. Sci., Vol. 57 (2010) 2294.

[6] Particulars, Advanced measurement systems, Ltd. www.particulars.si

[7] I. Mandić et al., Study of neutron irradiation effects in Depleted CMOS structures, arXiv:2112.10738v1 [physics.ins-det].

[8] J. Liu, Study of a monolithic pixel detector for the ATLAS tracker at the High Luminosity LHC, PhD thesis, Aix-Marseille University, Marseille, 2016.

[9] C. Zhang et al., Development of RD50-MPW2: a high-speed monolithic HV-CMOS prototype chip within the CERN-RD50 collaboration, PoS (TWEPP 2019) 045.

[10] R. Marco, Latest depleted CMOS sensor developments in the CERN-RD50 collaboration, JPS Conf. Proc. 34 010008 (2021).

[11] B. Hiti et al., Characterisation of analogue front end and time walk in CMOS active pixel sensor, 2021 JINST 16 P12020~~to be published in J. Instrum.13 (2021)~~.

[12] P. Sieberer et al., Readout system and testbeam results of the RD50-MPW2 HV-CMOS pixel chip, arXiv:2201.08585v1 [physics.ins-det]~~submitted to J. Phys. Conf. Ser. (2021)~~.

[13] S. Ritt, Design and performance of the 6 GHz waveform digitizing chip DRS4, 2008 IEEE Nuclear Science Symposium Conference Record, 2008, pp. 1512-1515, doi: 10.1109/NSSMIC.2008.4774700.

Development of High Voltage-CMOS sensors within the CERN-RD50 collaboration

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Abstract

This paper presents work done by the CERN-RD50 collaboration to develop and study monolithic CMOS sensors for future hadron colliders, especially in terms of radiation tolerance, time resolution and granularity. Currently CERN-RD50 is completing the performance evaluation of RD50-MPW2 and has recently submitted RD50-MPW3, the second and third prototype sensor chips designed by the collaboration. The paper gives an overview of the main design aspects and performance evaluation results of the first two prototype chips RD50-MPW1 and RD50-MPW2, and details the design of the latest prototype RD50-MPW3. RD50-MPW2 is a small prototype with an 8 x 8 matrix of active pixels which implement analogue readout electronics only and solutions for low leakage currents. This prototype has been evaluated in the laboratory and also at proton and ion beam facilities, before and after irradiation with neutrons up to $2 \cdot 10^{15}$ n_{eq}/cm^2. RD50-MPW3 is a more advanced prototype with a matrix of 64 x 64 pixels which integrate both analogue and digital readout electronics inside the sensing diodes. To alleviate routing congestion and minimise crosstalk noise, the pixels are serially configured and organised in a double column scheme. This prototype

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has optimised peripheral readout electronics for effective chip configuration, based on the I2C protocol, and fast data transmission.

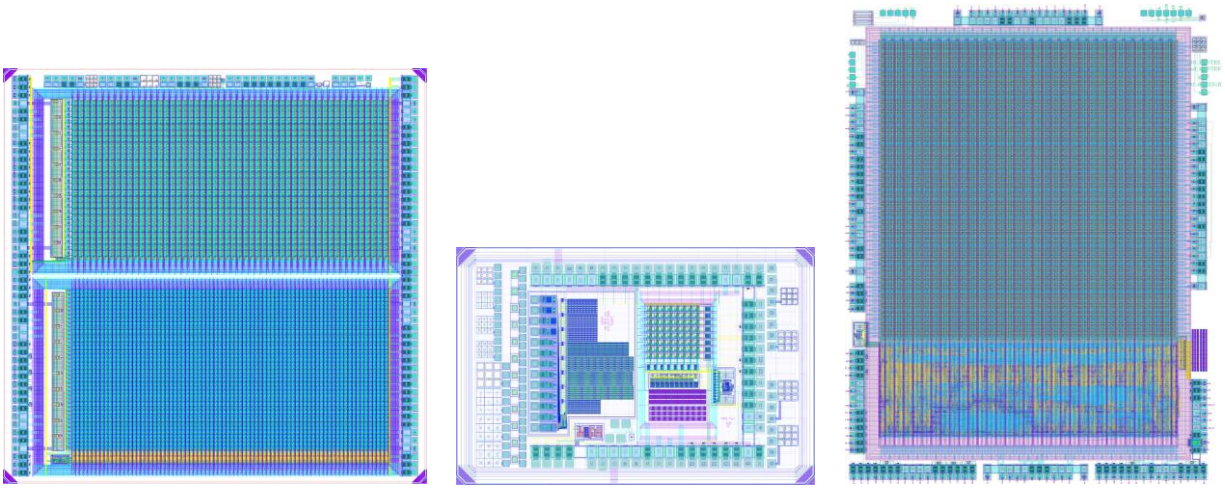
Keywords: CERN-RD50, depleted monolithic active pixel sensor, future hadron colliders, high voltage-CMOS technology, high voltage pixel detector, monolithic CMOS detector.

1. Introduction

This paper presents results from the RD50-MPW series of monolithic CMOS sensors, developed by the CERN-RD50 collaboration to study this technology in view of the harsh requirements imposed by future hadron colliders on tracking systems [1]. The RD50-MPW sensors developed so far are in the 150 nm High Voltage-CMOS (HV-CMOS) process from LFoundry S.r.l. Parameters especially considered in this programme are radiation tolerance, time resolution and granularity.

2. Design and characterisation of RD50-MPW1 and RD50-MPW2

This section reviews the main design aspects and performance evaluation results of RD50-MPW1 and RD50-MPW2 to illustrate the background on which the current prototype, RD50-MPW3, lies. Figure 1 shows the layout views of these three sensor chips. RD50-MPW1 has a matrix of 40 rows x 78 columns of high-granularity pixels where these integrate the analogue and digital readout electronics inside their area of 50 µm x 50 µm. The analogue readout, based on conventional electronics for charge-collecting detectors, includes a Charge Sensitive Amplifier (CSA) with continuous reset, low-pass and high-pass filters, and a CMOS comparator with a 4-bit Digital-to-Analogue Converter (DAC) to tune locally small threshold voltage variations. The digital readout is based on the well-known column drain architecture (i.e. FE-I3 style) [2]. It provides two 8-bit time-stamps, one for the leading edge and another one for the trailing edge, and an 8-bit address. When a pixel registers an event, it sends the leading



(a) **(b)** **(c)**

Fig. 1. Layout views of RD50-MPW1 (a), RD50-MPW2 (b) and RD50-MPW3 (c). The dimensions of these prototype sensor chips are 5 mm x 5 mm, 3.2 mm x 2.1 mm and 5.1 mm x 6.6 mm respectively.

and trailing edge time-stamps, and its address, to the corresponding End-Of-Column (EOC) circuit at the periphery through a 24-bit bus. This bus is shared by all the pixels within a column. The 78 EOC circuits of the matrix, which function as two 16-bit parallel-in parallel-out shift-registers, are connected to two readout serialisers designed to run at a maximum speed of 640 MHz. RD50-MPW1 was fabricated in two high resistivity substrates with nominal values of 500 Ω·cm – 1.1 kΩ·cm and 1.9 kΩ·cm.

The Data Acquisition System (DAQ) for the RD50-MPW sensor chips builds on the general-purpose Control and Readout (CaR) board [3]. It comprises a dedicated chip carrier board, the CaR board, an FPGA Mezzanine Card (FMC) and a Xilinx ZC706 or ZC702 evaluation board. The evaluation of fabricated RD50-MPW1 samples has revealed this chip essentially works, but also that it suffers from high leakage current in the sensing diodes, voltage drops across the pixel matrix and crosstalk noise between the lines that carry digital signals [4]. Several RD50-MPW1 samples have been irradiated with neutrons up to $2 \cdot 10^{15}$ n_{eq}/cm^2 at the TRIGA reactor in Ljubljana, Slovenia. The test structures of this chip, which consist of a small matrix of passive pixels, have been evaluated with the edge Transient Current Technique (eTCT) using the Particulars measurement system [5, 6]. The measurement results show the irradiation effects are compatible with those found in the literature [7].

RD50-MPW2, the successor chip, implements solutions to minimise the high leakage current observed in RD50-MPW1 and has a simple pixel matrix to test these. The solutions consist of a guard ring frame at the edge of the chip

and the prevention of certain post-processing filling layers that involve conductive material. The guard ring frame has one n-type ring that acts as a current collecting ring and six p-type rings that control the termination of the lateral depletion of the sensing diodes, in addition to one p-type seal ring that protects the design from damage caused by the sawing process [8]. RD50-MPW1 has the p-type seal ring only. The matrix in RD50-MPW2 has 8 rows x 8 columns of 60 µm x 60 µm pixels with analogue readout only. The larger pixel size is due to the increase of the spacing between the p-n electrodes of the diode for a higher breakdown voltage (8 µm spacing in RD50-MPW2 as opposed to 3 µm spacing in RD50-MPW1). The matrix integrates two different flavours of readout electronics, with continuous and switched reset CSAs, optimised for short response times to resolve particles at high rates [9]. RD50-MPW2 was fabricated in the standard resistivity of 10 Ω·cm and in three high resistivity substrates with nominal values of 500 Ω·cm – 1.1 kΩ, 1.9 kΩ·cm and > 2 kΩ·cm.

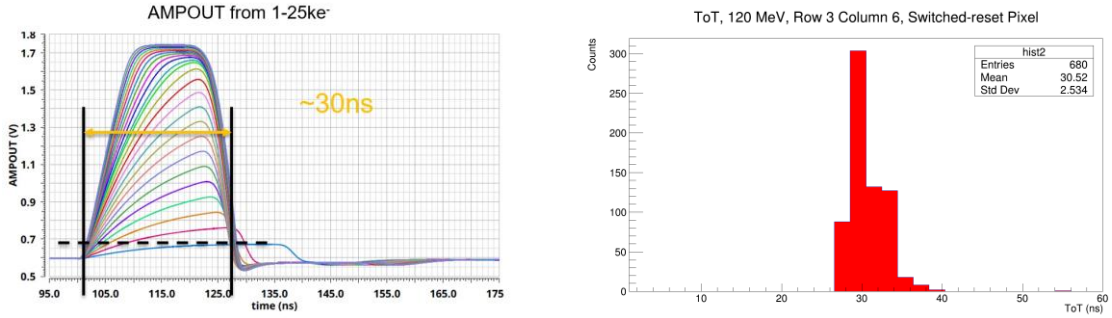
RD50-MPW2 has been evaluated in the laboratory and also at proton and ion beam facilities. The prototype exhibited a leakage current of 100 pA/pixel (1 µA/pixel in RD50-MPW1), a breakdown voltage of 120 V (56 V in RD50-MPW1) and an Equivalent Noise Charge (ENC) better than 2 mV [10]. Given the capacitance of 2.8 fF of the calibration circuit for injecting a test charge into the amplifier, the ENC is therefore better than 50 e^-. The eTCT setup has been used to study the depletion depth of the test structures, integrated in RD50-MPW2 as a small matrix of passive pixels, after irradiation with neutrons to several fluence up to $2 \cdot 10^{15}$ n_{eq}/cm^2 [7]. The setup was also used, for the first time, to investigate the time-walk of the 8 x 8 active pixel matrix [11]. The eTCT measurements showed the depletion depth is 110 µm, while the time-walk is better than 10 ns at 200 e^- threshold voltage and from 2 ke^- collected charge and above. Both parameters were measured at 100 V substrate biasing and before irradiation. After irradiation to $5 \cdot 10^{14}$ n_{eq}/cm^2 the depletion depth is 90 µm and the time-walk is kept at approximately the same value as before irradiation. After irradiation to $2 \cdot 10^{15}$ n_{eq}/cm^2, the depletion depth is 60 µm. The proton test beams have been conducted at the Rutherford Cancer Centre in Northumberland, United Kingdom, and MedAustron in Vienna, Austria [12], and the ion test beam at the Ruđer Bošković Institute in Zagreb, Croatia. The main goal of the proton test beams was to evaluate the experimental setups, newly developed to enable synchronisation with other detectors and accept triggers, together with the sensor chip and a particle beam as well as to obtain initial measurement results. Both setups consist of a telescope made of one RD50-MPW2 sample and the CaR DAQ placed between two scintillators. At the Rutherford setup the trigger is taken from the comparator output of the sensor chip, the two scintillators are used to

discard noise events and the data generated by the amplified and discriminated outputs are recorded using a DRS4 switched capacitor array digitiser [13]. At the MedAustron setup the telescope is triggered by the coincidence of the two scintillators and the data is recorded using a test beam firmware based on a First-In, First-Out (FIFO) memory that captures the Time-over-Threshold (ToT). Beam energies of 120 MeV (Rutherford) and 252.7 MeV (MedAustron) were used. The ToT was characterised at both test beams with the switched reset pixel flavour, for which a value around 30 ns is expected regardless of the charge collected by the pixel according to design simulations. While the switched reset pixel does not provide information about the signal amplitude, it was chosen for these measurements to validate the test beam setups. The measured ToT distribution peaks at 30 ns (Rutherford) and 35 ns (MedAustron). Figure 2 shows the simulation of the analogue pixel output, from which the simulated ToT was calculated, and the ToT distribution measured at Rutherford. The analysis of the ion test beam at the Zagreb Ruđer Bošković Institute is ongoing. Table 1 summarises the main performance parameters of RD50-MPW2.

In spite of its success RD50-MPW2 has several design limitations, such as the small number of rows and columns of the pixel matrix, the lack of digital readout electronics to identify events and a very simple peripheral readout that makes certain types of measurements too slow or not possible. To give a specific example of the consequences of these limitations, in RD50-MPW2 only one pixel at a time can be read out and this has restricted its evaluation programme. The collaboration is currently developing a new prototype, RD50-MPW3, which integrates a larger and more advanced pixel matrix with new and optimised peripheral readout electronics to further study monolithic CMOS sensors.

3. Design of RD50-MPW3

RD50-MPW3 overcomes the limitations of RD50-MPW2 by extending the number of pixels in the matrix (64 columns x 64 rows), incorporating in the pixel area digital readout electronics based on the column drain architecture and adding optimised peripheral readout electronics for effective pixel configuration and fast data transmission. RD50-MPW3 includes as well a few dedicated test structures, mostly to characterise the diode current-to-voltage characteristics, depletion depth and parasitic capacitance. RD50-MPW3 is being fabricated in three different substrate resistivities, which are the standard resistivity (10 Ω·cm) and two high resistivities of 1.9 kΩ·cm and 3 kΩ·cm.



(a) **(b)**

Fig. 2. The simulation of the analogue output gives a ToT of about 30 ns (a) and ToT measurement results show a distribution peaking at 30 ns.

Table 1

Main performance parameters of RD50-MPW2. All the values are measured at 100 V substrate biasing with 1.9 kΩ·cm substrate resistivity samples (except were specified). CR stands for Continuous Reset pixel and SR for Switched Reset pixel. NC stands for Not Characterised.

Parameter	Value (before irradiation)	Value ($5 \cdot 10^{14}$ n_{eq}/cm^2, neutrons)	Value ($2 \cdot 10^{15}$ n_{eq}/cm^2, neutrons)
Breakdown voltage [V]	120	126[d]	136[e]
Leakage current [nA/pixel]	0.1	50[d]	60[e]
Depletion depth [µm][a]	110	90	60
ENC [e^-]	50	NC	NC
Time-walk (CR) [ns][b]	9	9	NC
ToT (CR) [ns][b]	110	120	NC
ToT (SR) [ns][c]	30	NC	NC

[a]Measured with a > 2 kΩ·cm sample. A depletion depth of 118 µm was measured with a 1.9 kΩ·cm RD50-MPW1 sample at a 100 V substrate biasing (estimated depletion depth from measurements, as breakdown voltage is around 56 V in this prototype).

[b]Measured at 200 e^- threshold voltage and 8 ke^- collected charge using an eTCT setup. Continuous reset pixels were chosen for this study as the comparator output signal scales with the signal size and can be used to measure the amount of input charge.

[c]Measured at proton test beams. Switched reset pixels were chosen as these have higher gain than continuous reset pixels.

[d]Measured after irradiation to $1 \cdot 10^{14}$ n_{eq}/cm^2. The values after $5 \cdot 10^{14}$ n_{eq}/cm^2 are expected to be very similar.

[e]Measured after irradiation to $1 \cdot 10^{15}$ n_{eq}/cm^2. The values after $2 \cdot 10^{15}$ n_{eq}/cm^2 are expected to be very similar.

The RD50-MPW3 in-pixel digital readout is a highly improved version of that developed for RD50-MPW1. It incorporates logic to mask noisy pixels, replaces the priority circuit that determines the order in which hits are read out for a more compact alternative based on an OR chain, and allows pausing the digitisation of new hits until the readout of a column is complete. Each pixel contains as well a new 8-bit SRAM shift register, which enables serial configuration and stores a per pixel-trimming to compensate threshold voltage variations (four bits), a flag to mask noisy pixels (one bit), and data to enable or disable the calibration circuit (one bit), the amplifier output monitor (one bit) and the comparator output monitor (one bit). The configuration shift registers are programmed during the chip initialisation and hold the values indefinitely until the chip is reprogrammed or powered down. The analogue readout electronics reuse those developed for the continuous reset pixel of RD50-MPW2, as the laboratory and test beam evaluations showed their performance matches design specifications. Details about the diode implementation are available in [4]. Figure 3 shows a simplified version of the pixel schematic. Figure 4 shows a mixed-mode simulation using the post-layout view of a pixel that receives a test pulse from the calibration circuit.

3.2. Double pixel scheme

RD50-MPW3 implements a double column scheme for the first time in the RD50-MPW prototypes, which together with the also new 8-bit SRAM shift register for serial configuration, alleviates the routing congestion and facilitates means to minimise the crosstalk noise. Most of the routing area is occupied by a 24-bit bus with 8-bit Gray encoded time-stamps of the leading and trailing edges of the discriminator output as well the 8-bit address of the pixel. The double column scheme almost halves the number of necessary metal routing lines, as the pixels within a double column share most of the many metal routing lines they require. To enable that, the layout of the pixels is horizontally mirrored in every double column (i.e. analogue readout on one side and digital readout on the other side for one of the two columns, and vice versa for the other). To further prevent the generation of crosstalk noise, there is one metal routing line connected to ground between every two long metal routing lines that carry fast digital signals. The width of these metal lines, which are in metal 4, and the spacing between them is the minimum allowed by the design rules. The connections between the two pixels in a double pixel are in metal 3. To avoid noise coupling between the analogue and digital domains, the analogue and digital grounds are separated with a trench made of shallow n-well and deep n-isolation (called NISO in this process). The pixel size in RD50-MPW3 is 62 µm x 62 µm.

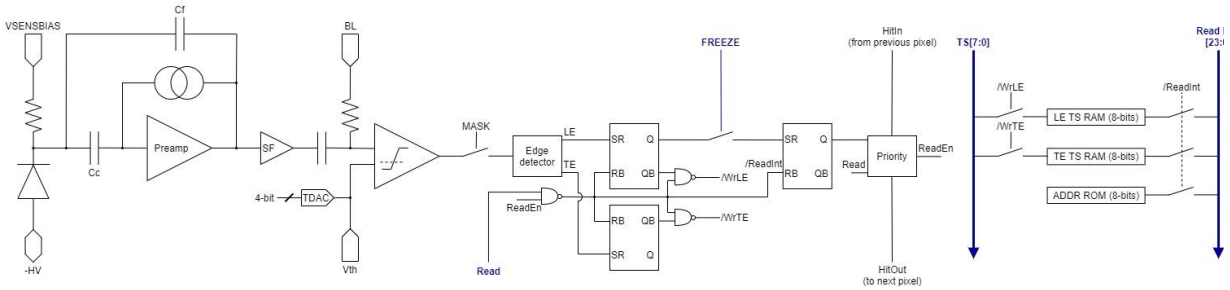


Fig. 3. Simplified schematic view of the RD50-MPW3 pixel including both the analogue and digital readout electronics.

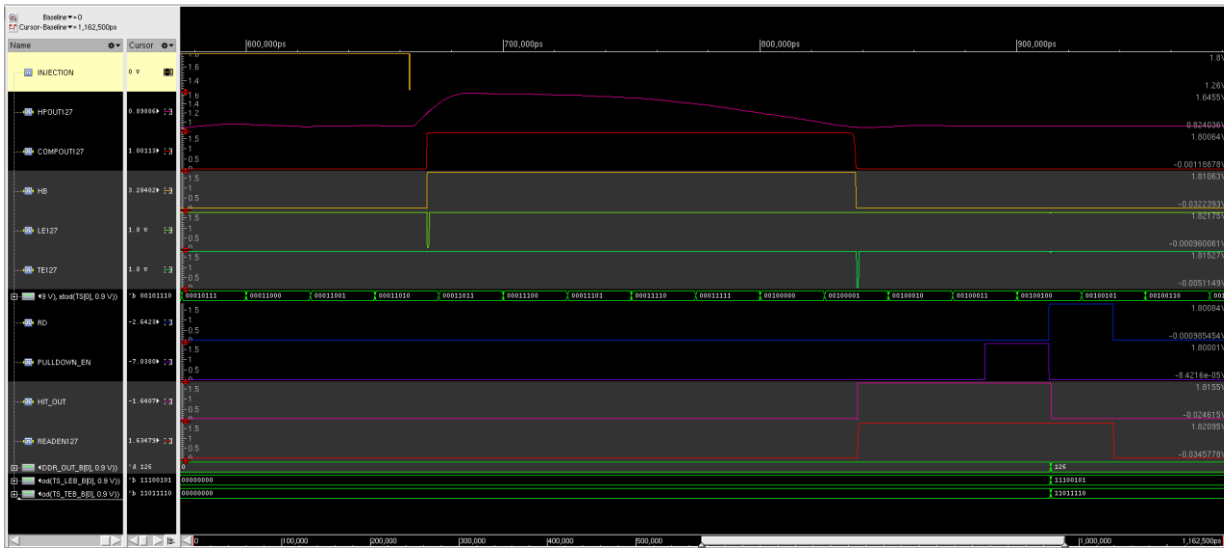


Fig. 4. Mixed-mode simulation using the post-layout view of a pixel: INJECTION is the test pulse from the calibration circuit; HPOUT the shaped signal at the comparator input; COMPOUT the comparator output; LE and TE the leading and trailing edges sensed by the digital readout electronics; TS the time-stamp; RD and PULLDOWN_EN digital signals sent to the pixel to store the pixel address and time-stamps in the corresponding EOC; HIT_OUT the output of the priority circuit connected to the following pixel in the double column; and READEN the output of the priority circuit connected to the digital readout of the pixel. The last three waveforms correspond to the pixel address, and leading and trailing edge time-stamps.

This represents a small increase of the pixel size in RD50-MPW2 (60 µm x 60 µm), however it is necessary to accommodate all the new features here described while maintaining the breakdown voltage achieved in the previous prototype (8 µm spacing between the p-n electrodes of the diode for a 120 V breakdown voltage). Figure 5 shows the layout view of a double pixel. To avoid voltage drops in the power distribution, the pixel matrix incorporates a grid of wide metal lines in the highest possible metal layers (horizontal lines in metal 5, and vertical lines in metal 6). The

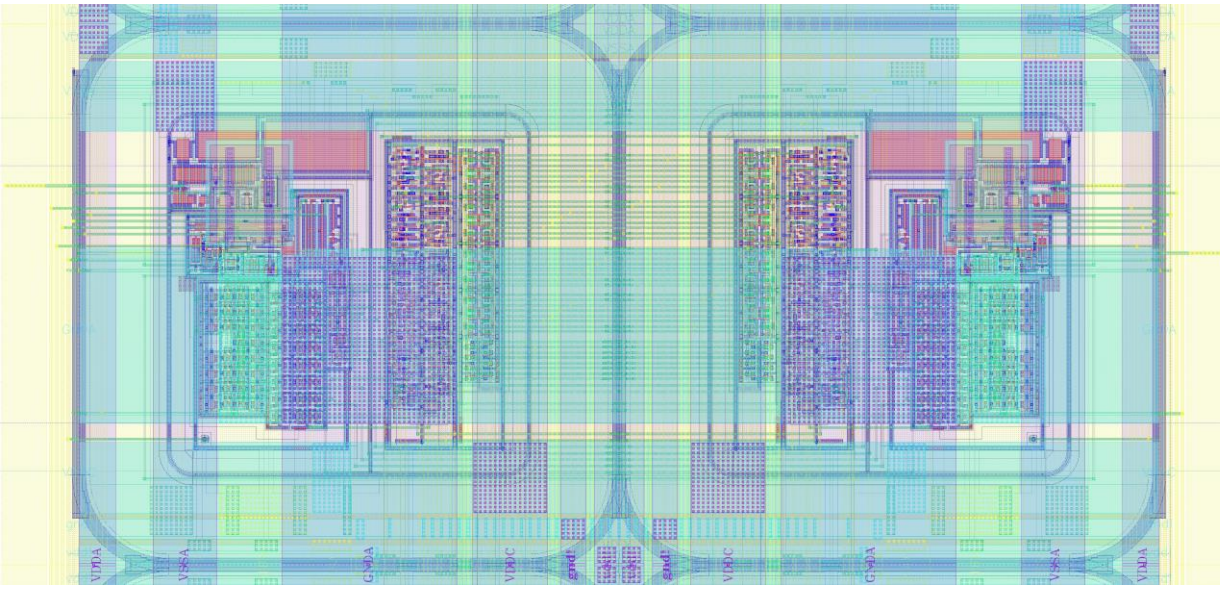


Fig. 5. Layout view of a double pixel. Explanations are given in the text.

metal grid is visible in the layout view of the double pixel. The pixels have four independent power domains, as the various sub-circuits in each pixel are powered separately, in addition to two ground domains.

3.3. Peripheral electronics

The peripheral electronics, which configure the pixels and control the data readout, consist of new and optimised EOC circuits, a Control Unit (CU) and a slow control system based on the I2C protocol for external communication using an internal Wishbone bus. There is one EOC circuit for every two double column of pixels. The EOCs are handled by the CU. They use a FIFO memory to store, temporarily, the data generated by the pixels within a double column (i.e. leading and trailing edge time-stamps, and pixel address). This reduces the dead time, as pixels with hits are read out immediately as long as the FIFO is not full. The generated data is packed into frames, zero-suppressed and serialised at a maximum rate of 640 Mb/s, by a data transmission unit over Low Voltage Differential Signal (LVDS) lines. The readout of the pixel matrix is triggerless. All the peripheral blocks are configured through Control Status Registers (CSRs), which are connected to a Wishbone bus and read/written using an I2C interface. Figure 6 shows a block diagram of the peripheral readout electronics.

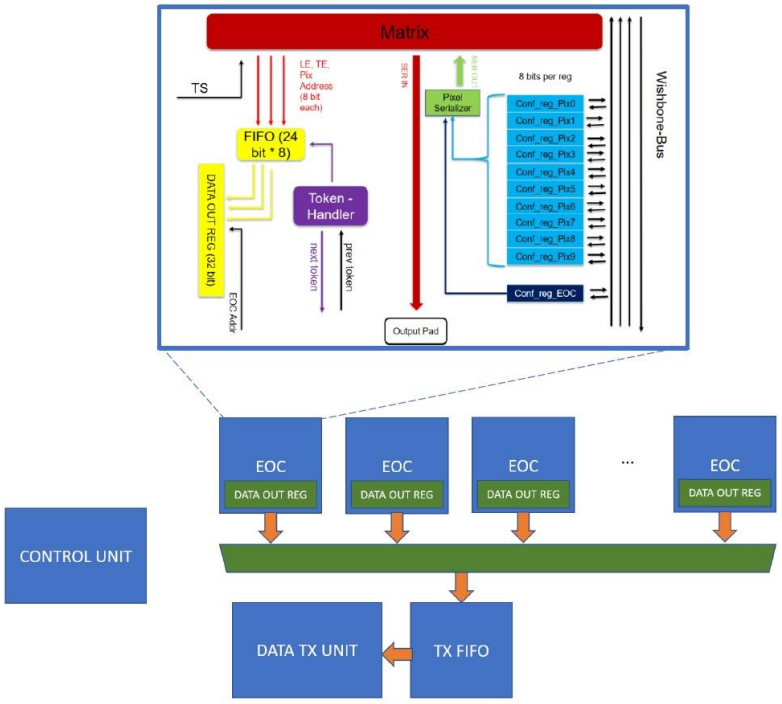


Fig. 6 Simplified block diagram of the peripheral readout electronics of RD50-MPW3.

4. Conclusion

This paper describes work done by the CERN-RD50 collaboration to study and develop the RD50-MPW series of monolithic CMOS sensors in the 150 nm HV-CMOS process from LFoundry S.r.l. RD50-MPW2 has been designed and evaluated both in the laboratory and also at proton and ion beam facilities. The prototype exhibited a leakage current of 100 pA/pixel, a breakdown voltage of 120 V and an Equivalent Noise Charge (ENC) better than 50 e^-. The eTCT measurements showed the depletion depth is 110 µm, and the time-walk is better than 10 ns at 200 e^- threshold voltage and from 2 ke^- collected charge and above. After irradiation to $5 \cdot 10^{14}$ n_{eq}/cm^2 the depletion depth is 90 µm and the time-walk is kept at approximately the same value as before irradiation. After irradiation to $2 \cdot 10^{15}$ n_{eq}/cm^2, the depletion depth is 60 µm. The test beam measurement results show a ToT distribution peaking around 30 ns and are in good agreement with simulated results. RD50-MPW3 is a more advanced prototype, with a matrix of 64 x 64 pixels which integrate both analogue and digital readout electronics inside the sensing diodes, and optimised

peripheral readout electronics for effective chip configuration and fast data transmission. This chip is currently being fabricated.

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References

[1] M. Benedikt et al., Future Circular Collider, Vol. 3: The Hadron Collider (FCC-hh), CERN-ACC-2018-0058 (2018).

[2] I. Peric et al., The FEI3 readout chip for the ATLAS pixel detector, Nucl. Instrum. Methods Phys. Res., Sect. A 565 (2006) 178.

[3] H. Liu et al., Development of a modular test system for the silicon sensor R&D of the ATLAS Upgrade, arXiv:1603.07950v4 [physics.ins-det].

[4] E. Vilella, Recent depleted CMOS developments within the CERN-RD50 framework, PoS (Vertex2019) 019.

[5] G. Kramberger et al., Investigation of irradiated silicon detectors by Edge-TCT, IEEE Trans. Nucl. Sci., Vol. 57 (2010) 2294.

[6] Particulars, Advanced measurement systems, Ltd. www.particulars.si

[7] I. Mandić et al., Study of neutron irradiation effects in Depleted CMOS structures, arXiv:2112.10738v1 [physics.ins-det].

[8] J. Liu, Study of a monolithic pixel detector for the ATLAS tracker at the High Luminosity LHC, PhD thesis, Aix-Marseille University, Marseille, 2016.

[9] C. Zhang et al., Development of RD50-MPW2: a high-speed monolithic HV-CMOS prototype chip within the CERN-RD50 collaboration, PoS (TWEPP 2019) 045.

[10] R. Marco, Latest depleted CMOS sensor developments in the CERN-RD50 collaboration, JPS Conf. Proc. 34 010008 (2021).

[11] B. Hiti et al., Characterisation of analogue front end and time walk in CMOS active pixel sensor, 2021 JINST 16 P12020.

[12] P. Sieberer et al., Readout system and testbeam results of the RD50-MPW2 HV-CMOS pixel chip, arXiv:2201.08585v1 [physics.ins-det].

[13] S. Ritt, Design and performance of the 6 GHz waveform digitizing chip DRS4, 2008 IEEE Nuclear Science Symposium Conference Record, 2008, pp. 1512-1515, doi: 10.1109/NSSMIC.2008.4774700.