# Characterization of Monolithic Active Pixel Sensors for future collider Experiment

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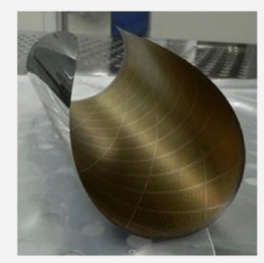
## Abstract

*In high-energy physics experiments, Monolithic Active Pixel Sensors (MAPS) have become crucial components of vertex and tracking detectors over the past decade due to the integration of readout circuitry with the detection volume in a single chip. The low material budget requirement to achieve precise tracking and vertexing capabilities for upgrade of HEP experiments, such as ALICE at LHC and future experimental facilities like ePIC at EIC, leads to a direct attention towards an ultra-thin (a few tens of μm), bent, wafer-scale silicon sensors produced with stitching technology.*
*Recent ongoing activities performed at the INFN and UniBa Laboratory in Bari will be described. The characterization of analogue silicon pixel sensors of 65 nm CMOS technology using electrical test pulsing and $^{55}$Fe as a soft X-ray source will be discussed. Furthermore, a study on timing performance will be presented.*


Bent wafer-scale sensor

## The 65 nm CMOS Analogue Pixel Test Structure

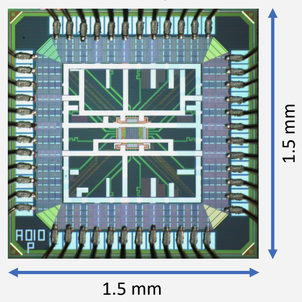
The APTS is a prototype test structure based on TPSCo CMOS 65 nm ISC technology.
CMOS pixels sensors with small collection electrode are characterized by a small sensor capacitance and consequently a high signal-to-noise ratio. From the monolithic design itself, a low material budget is reached allowing to a better resolution at low transverse momentum.

### Chip Characteristics:

- **matrix sizes:** 6×6 pixels
- **pixel pitch:** 10, 15, 20, 25 μm
- **Output drivers**: Operational Amplifier
- **Readout**: direct analogue of the 4x4 central submatrix[1]
- **Coupling**: DC/AC
- **Biasing**: 0 ÷ -5V (DC) - 0 ÷ 50V (AC)

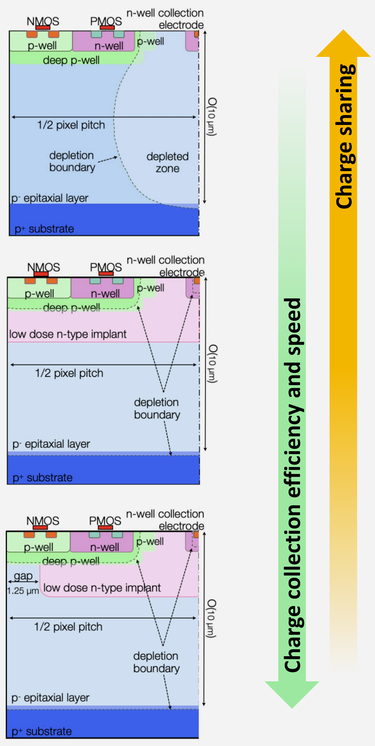
[1]The others 20 are dummy pixels allowing to minimize the distorsion of the electric field.

APTS Chip




### Pixel designs[1]:

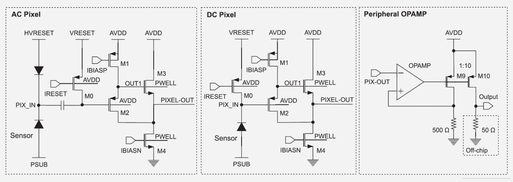
- **Standard**:
  - n-well collection electrode on a low resistivity p-type substrate.
  - In-pixel circuits placed outside the collection electrode and inside a deep p-well: full CMOS circuitry enabled.
  - Balloon-shaped depletion zone.
- **Modified**:
  - A deep low-dose n-type implant under the full pixel area creates a planar junction.
  - With some substrate reverse bias applied, a full depletion of the epitaxial layer is achieved allowing charge collection by drift.
- **Modified with gap (MwG)**:
  - A gap of 2.5 μm has been created at the pixel boundaries.
  - Reduction of the charge sharing among neighbouring pixels is expected due to an enhanced lateral electric field.



Schematics of the pixel design

### Readout chain[2]:

- **AC coupling:**
  - A capacitor is introduced between the sensing node and input transistor gate.
  - The sensing node is reset via a diode.
  - Substrate tied to the ground.
- **DC coupling:**
  - The sensing node is directly connected to the input transistor gate.
  - The sensing node is reset by a PMOS transistor.
  - A negative bias is applied to the substrate and to the bulk of NMOS transistors.



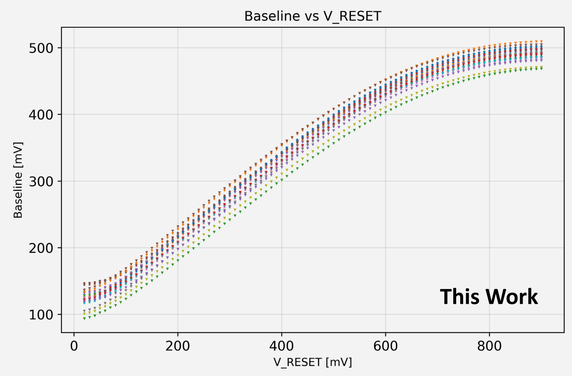
Schematics of the readout chain

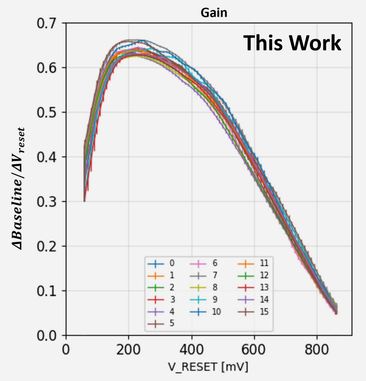
Operational Amplifier (OpAmp):
maximize speed capability to characterize charge collection time in the sub-nanosecond range.

## Laboratory Measurements

The chip testing is performed as follow:

**Electronic calibration** → Best Working point → **Radioactive measurements with $^{55}$Fe X-rays source**

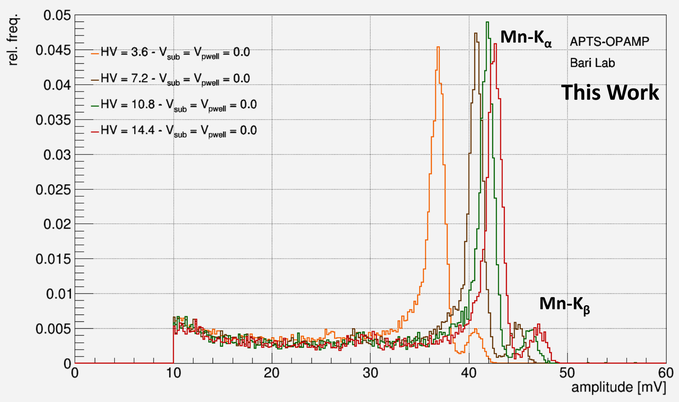



- Stable values of $\Delta Baseline/\Delta V_{reset}$ represent the best circuitry response.
- Pulsing by electronic charge injection into the circuitry to simulate diode data collection.

X-Ray emission close to MIP for direct chip characterization in terms of best amplitude signal and minimum fall time.

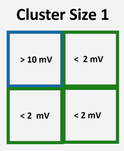
- Mn-$K_\alpha$ (5.9 keV) and Mn-$K_\beta$ (6.5 keV) peaks used as absolute energy calibration.

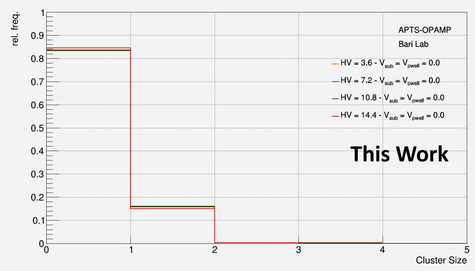


$^{55}$Fe Energy Spectrum Cluster size 1 measured with a MwG AC coupled sensor at different bias level

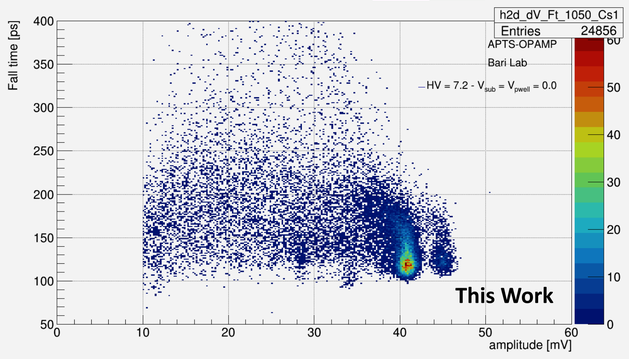
- **Modified with gap:**
  - High statistics for Cluster size 1 events
  - Slow events are suppressed
  - More than 80% of Cluster size 1 events: low charge sharing

Cluster Size 1



Cluster size distribution for MwG AC coupled sensor at different bias level



Fall-time vs Amplitude distribution for MwG AC coupled sensor at 7.2V as bias level

## Experimental Setup at INFN and UniBa Laboratory - Bari

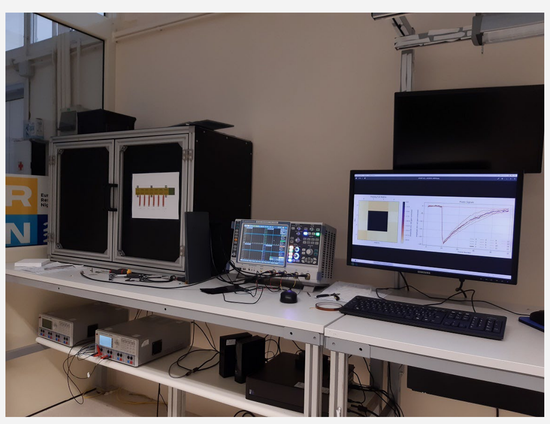
Multi Layer Reticle MLR1
First sensor prototypes in 65 nm process used to validate the technology in collaboration with CERN EP R&D.

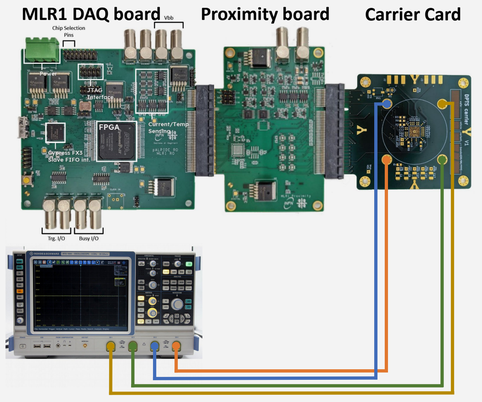
**MLR1 DAQ board** (FPGA-based):
- Powering and biasing the chip.
- Hosting the ADCs that sample the 16 pixels at 4MSa/s.

**Proximity and carried card:**
- Designed specifically for each chip flavour.

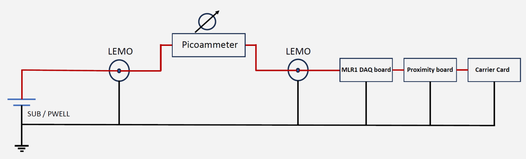
**Oscilloscope Rohde & Schwarz RTO RTO 1044:**
- Bandwidth: 4GHz - Sampling Rate: 20GSa/s
- Sampling the 2x2 inner pixel matrix for timing studies

**Picoammeter Keithley 6487:**
- VI measurement of leakage currents in the substrate

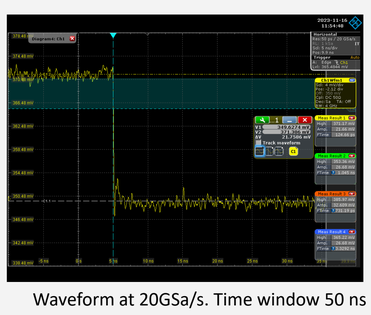

Silicon Lab @ University of Bari and INFN



Schematics of the experimental setup



Schematics of the leakage currents measurement


Waveform at 20GSa/s. Time window 50 ns

## Experimental facilities for outgassing studies in vacuum

Future vertex detectors will be mounted close to the beampipe where the order of vacuum will be about $10^{-10}$ mbar. Thus, it is very important to study the outgassing properties of the vertex detectors components.

**Three ways to perform outgassing measurement:**
- Comparing the vacuum level with and without sample
- Comparing residual atmosphere of vacuum chamber with and without sample using Residual Gas Analyzer (RGA)
- Comparing the Total Mass Loss (TML) of sample before and after pumping


Particular of the setup for sample transportation under vacuum


Experimental Setup for outgassing studies @ University of Bari and INFN

**Samples to test:**
- 3D printed aluminium nitride (AIN) samples disks
- $Al_2O_3$ samples disk: 3D printed alumina samples disks
- 3D printed AlSi samples disks
- Carbon (LAYPUS) Substrate of the cold plate
- Carbon Fleece of the cold plate
- Carbon foam All comp high density
- Carbon foam All comp low density
- Carbon foam ERG duocel
- Optical Fiber with connector
- NASA Epoxy
- Si wafer
- Wire bonded Si wafer
- FPC

## References

- [1] Rinella et Al., *Characterisation of analogue Monolithic Active Pixel Sensor test structures implemented in a 65 nm CMOS imaging process, arXiv, Instrumentation and Detectors, (2024) 2403.08952*
- [2] W. Deng et Al., *Design of an analog monolithic pixel sensor prototype in TPSCo 65 nm CMOS imaging technology, Journal of Instrumentation*, 18 (2023) C01065