SPADs and SiPMs in CMOS technology

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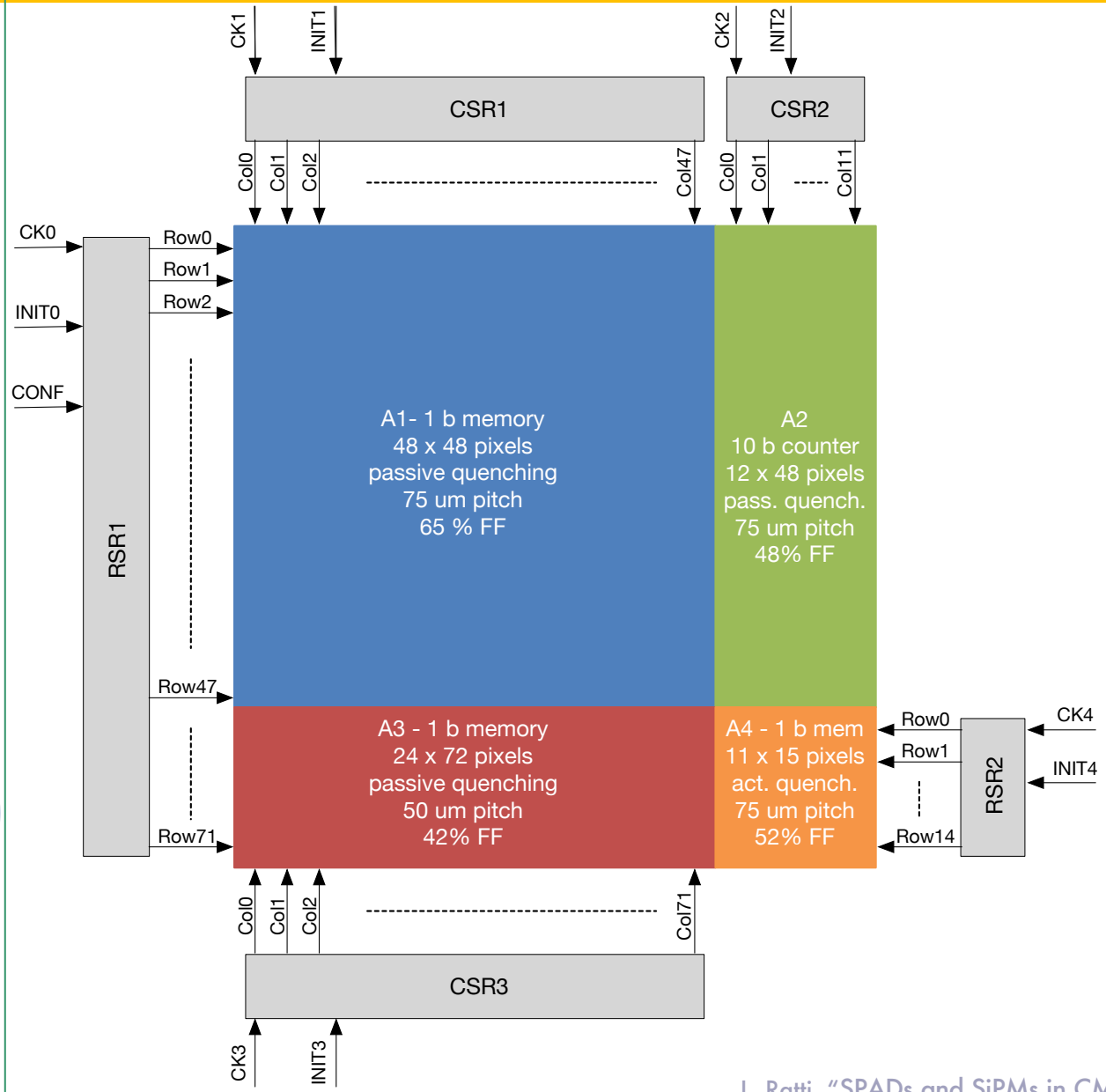
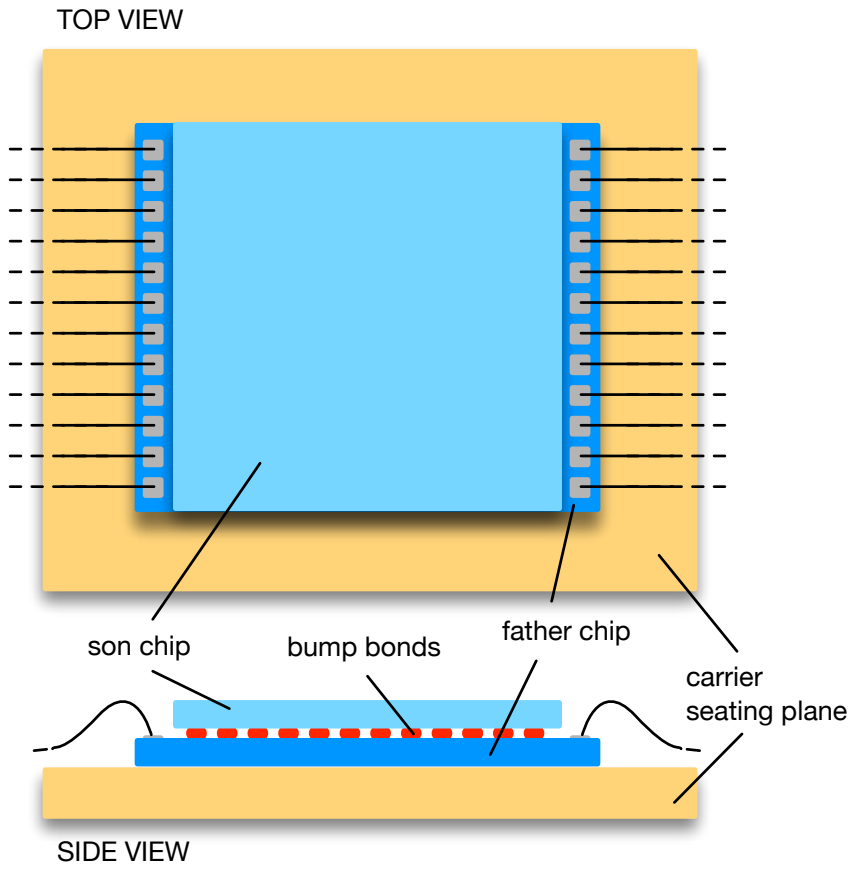
APIX2/ASAP experiment - APIX2LF chip





- 150 nm CMOS technology
- SPAD arrays available for characterization in single- and dual-layer configuration

Dual layer SPAD arrays

- DCR mitigation through vertical interconnection of two SPAD layers to produce a coincidence signal

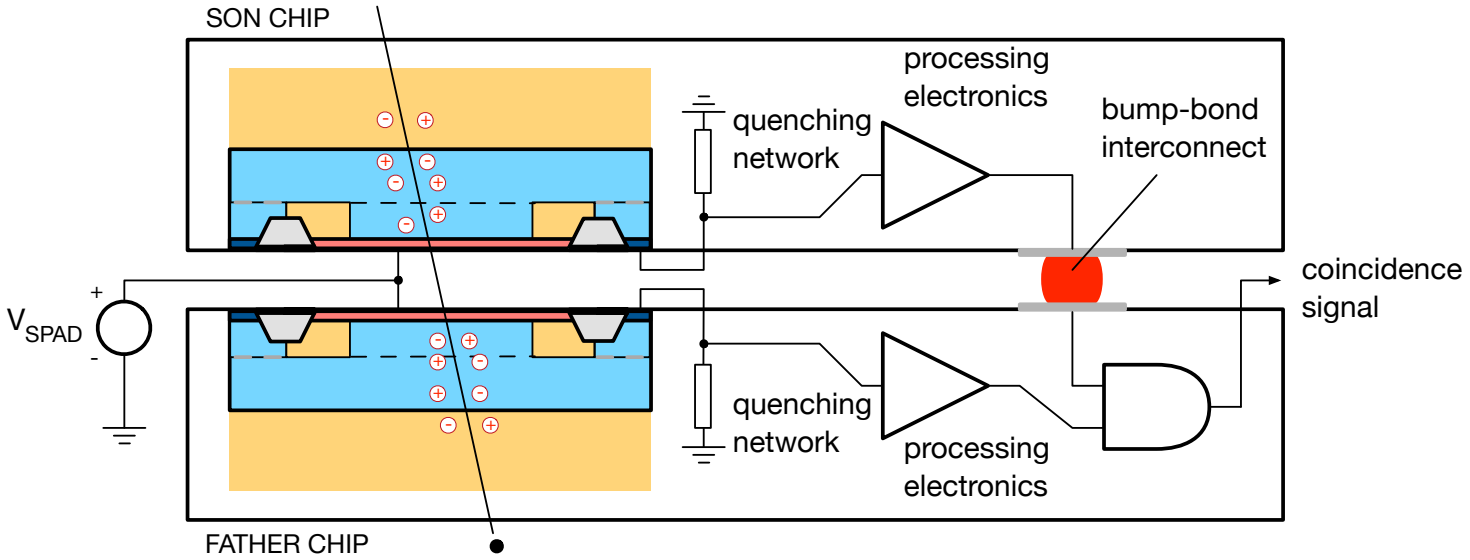
coincidence DCR rate

top layer DCR

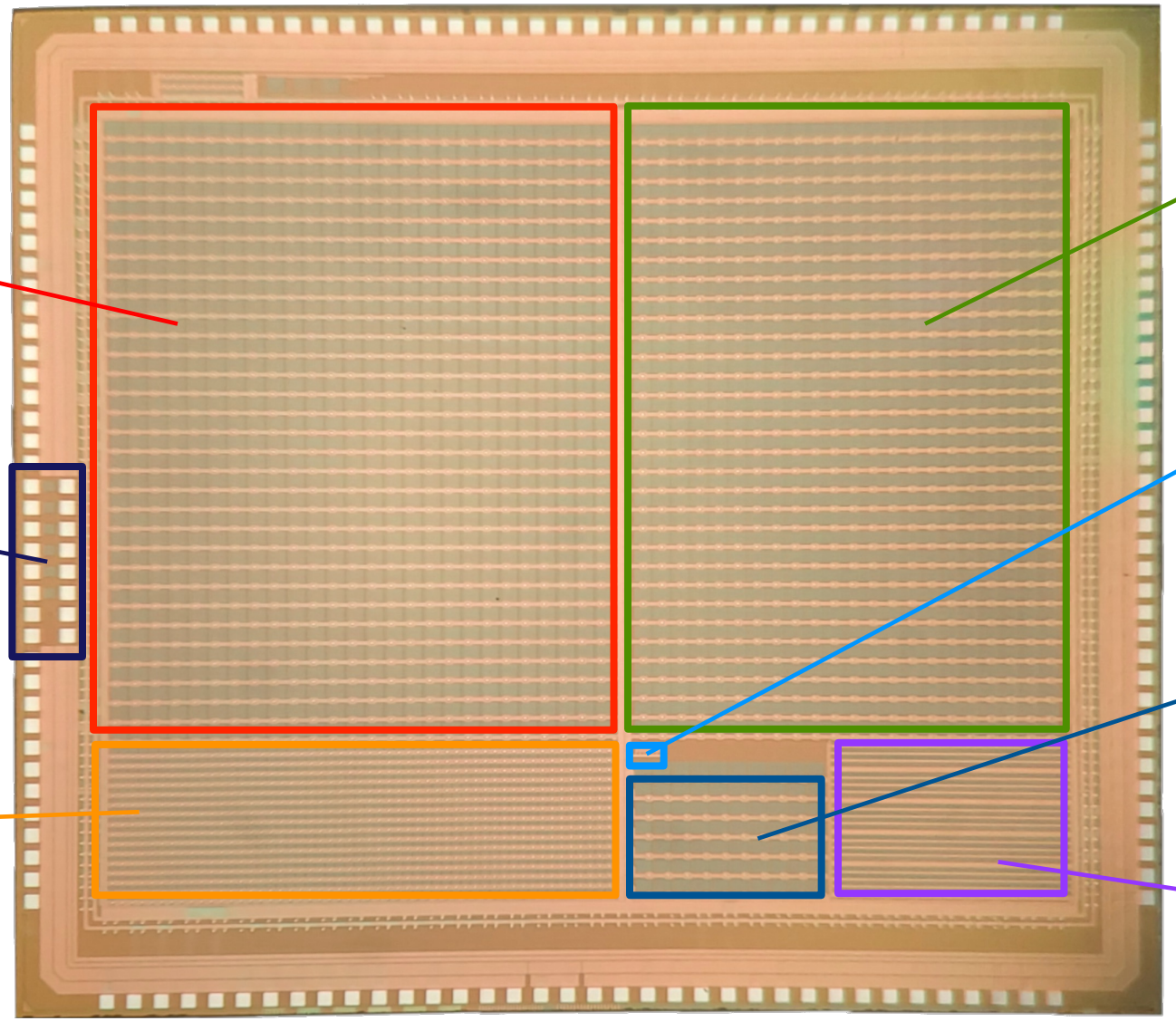
coincidence window

$$R_{COINC}=2R_TR_B\Delta t$$

bottom layer DCR



ASAP110LF chip – a technology characterization platform



100 um pitch,
passive quenching,
1 bit, FF=67%
(32x26)

single SPADs

50 um pitch,
passive quenching,
1 bit, FF=48%
(16x52)

100 um pitch,
passive quenching,
10 bit, FF=64%
(32x22)

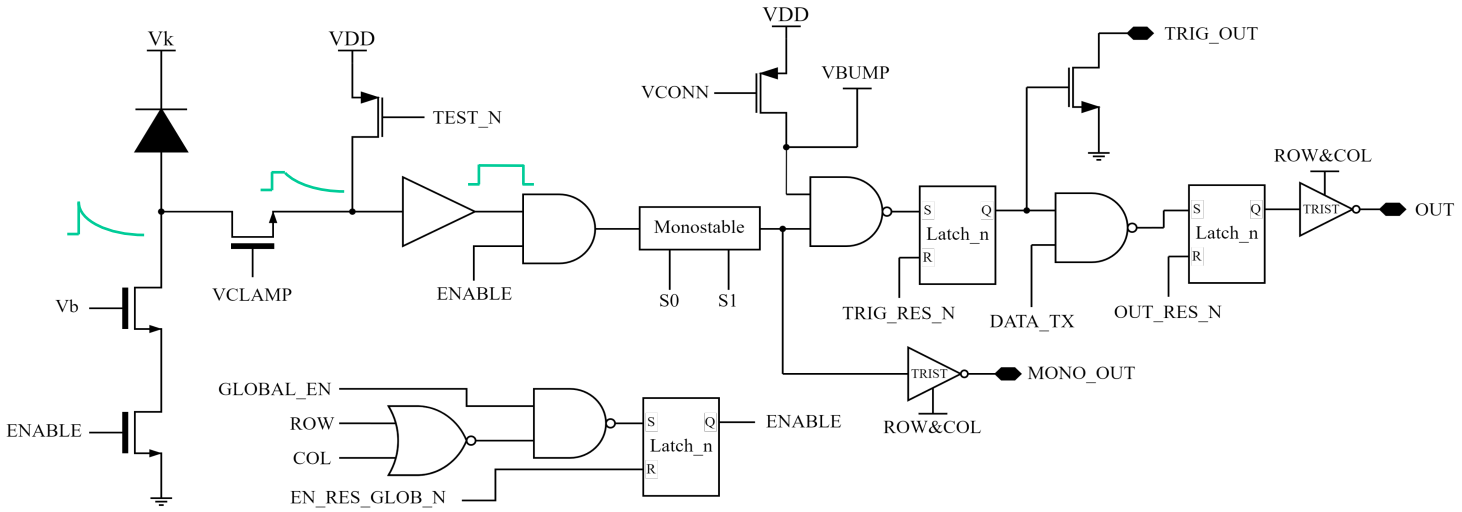
10b/20b TDC and
ring oscillator

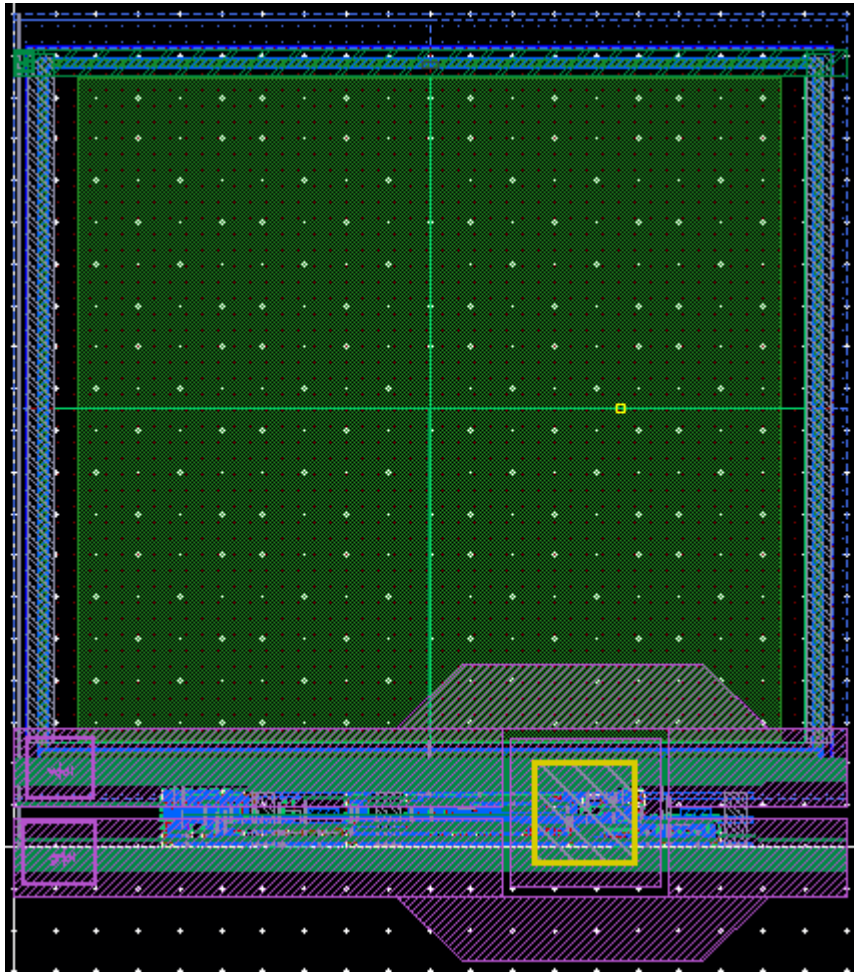
100 um pitch,
active quenching,
1 bit, FF=67%
(7x10)

Mini-SiPMs (4x4),
170 um x 105 um,
FF=41% (5x12)

ASAP110LF chip – Array 1

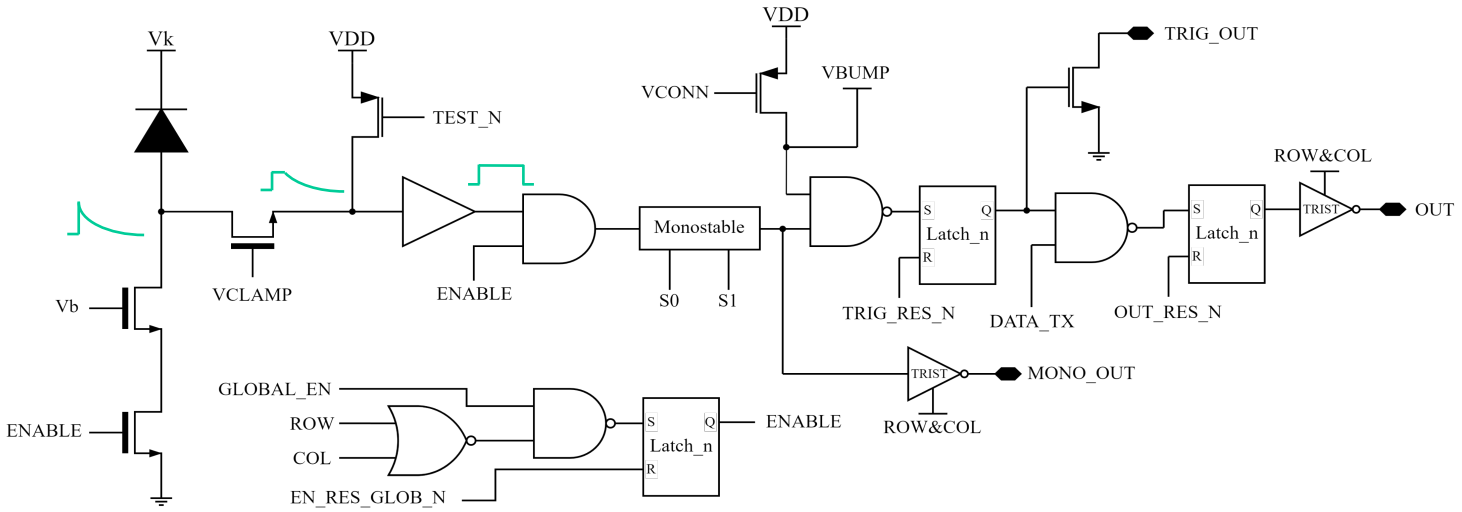
- The avalanche is quenched by a passive network made of transistors.
- An enable network has been implemented.
- The monostable circuit modifies the duration of the detection pulse to preset values (400 ps, 750 ps, 2 ns, transparent mode).
- A two-stage memory is used.

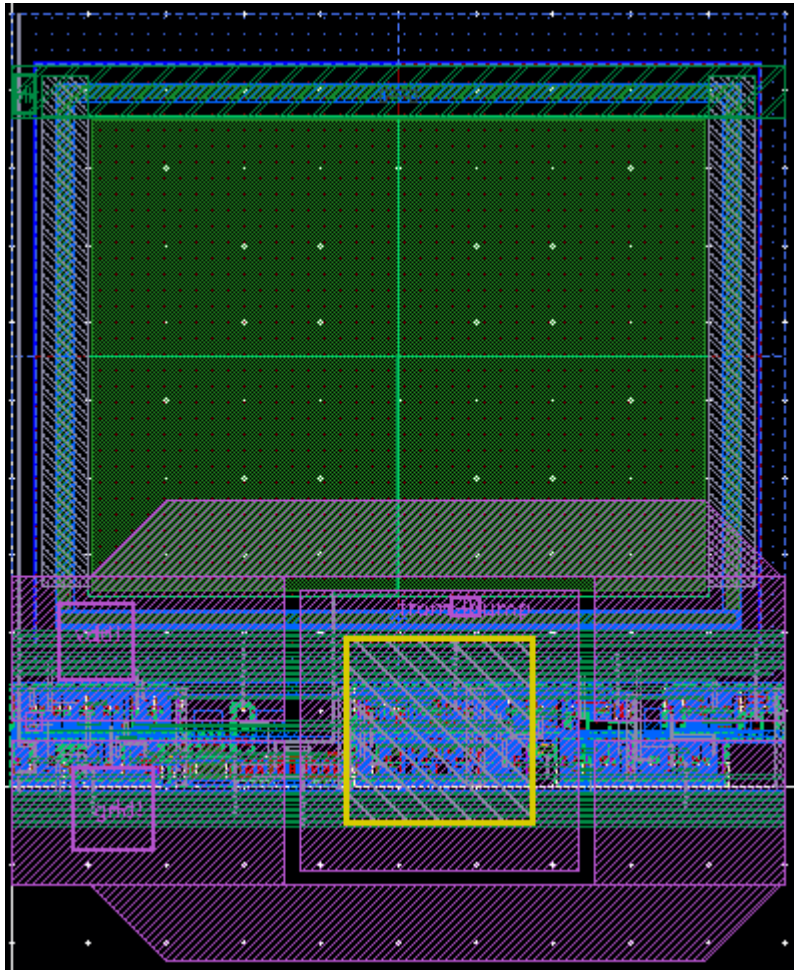




ASAP110LF chip – Array 2

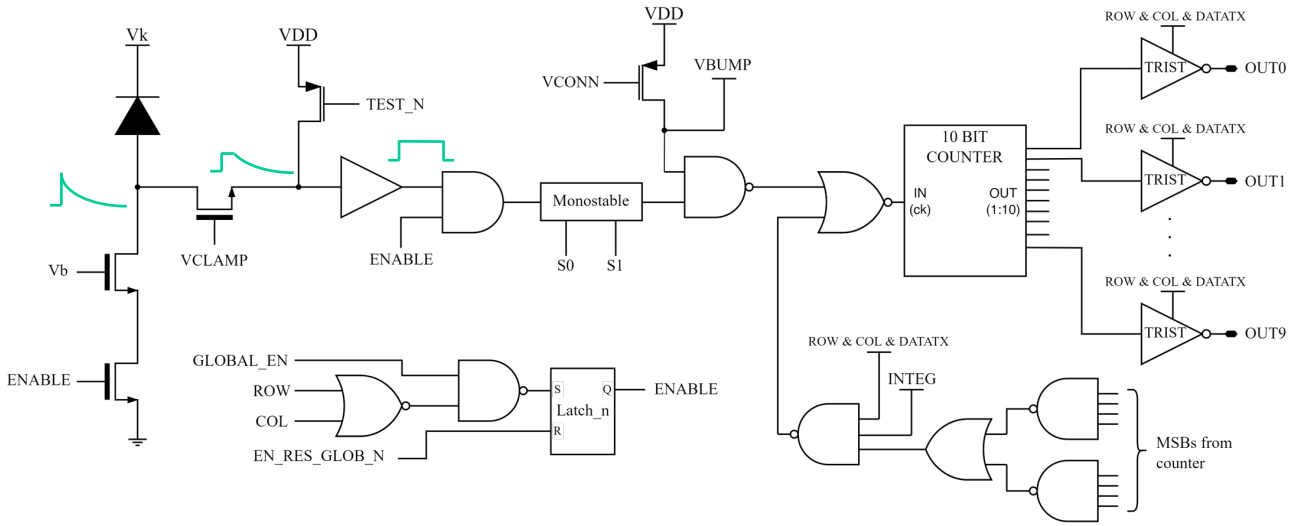
- The avalanche is quenched by a passive network made of transistors.
- An enable network has been implemented.
- The monostable circuit modifies the duration of the detection pulse to preset values (400 ps, 750 ps, 2 ns, transparent mode).
- A two-stage memory is used.

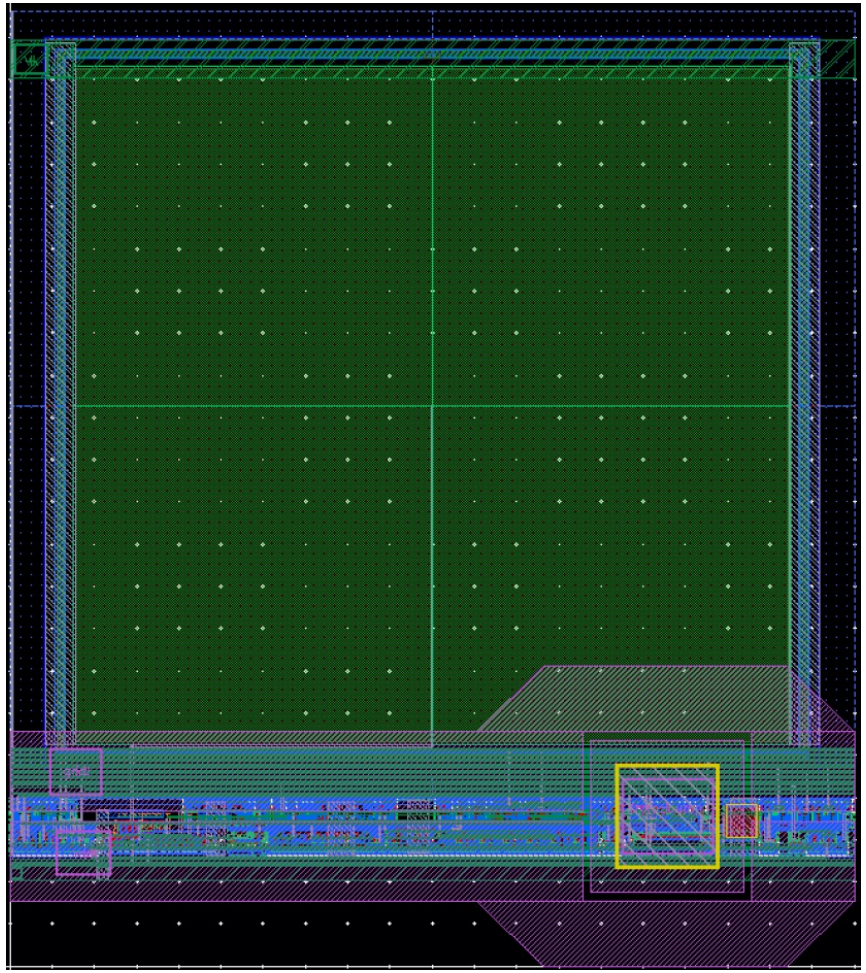




ASAP110LF chip – Array 3

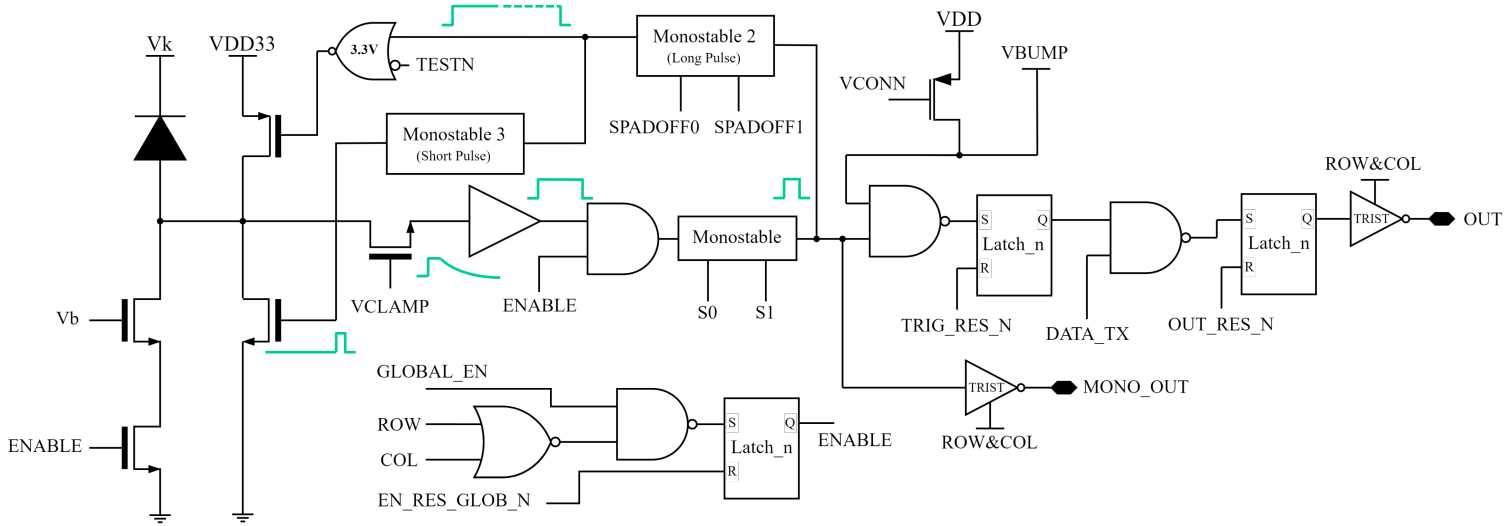
- A front-end network similar to the previous ones is used here.
- A 10 bit asyncronous counter automatically counts the detection pulses. The count result is provided to the output pads through tristate inverters.
- A feedback logic circuit controls the counter operation, depending on specific input bits.

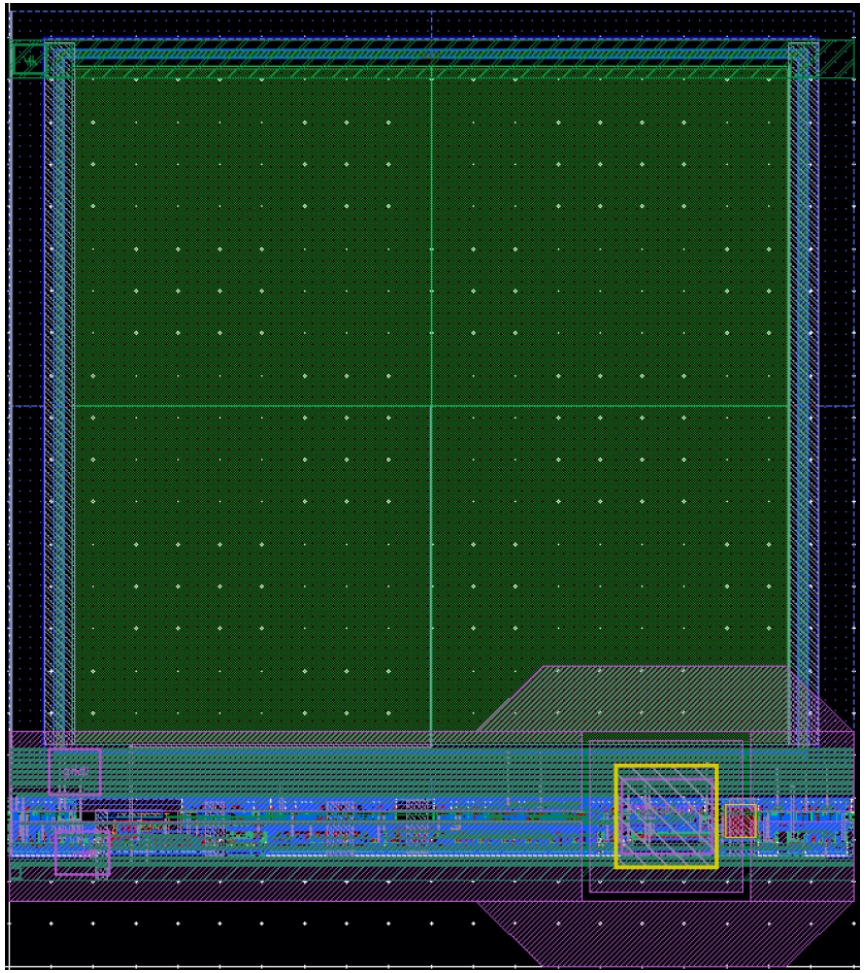




ASAP110LF chip – Array 4

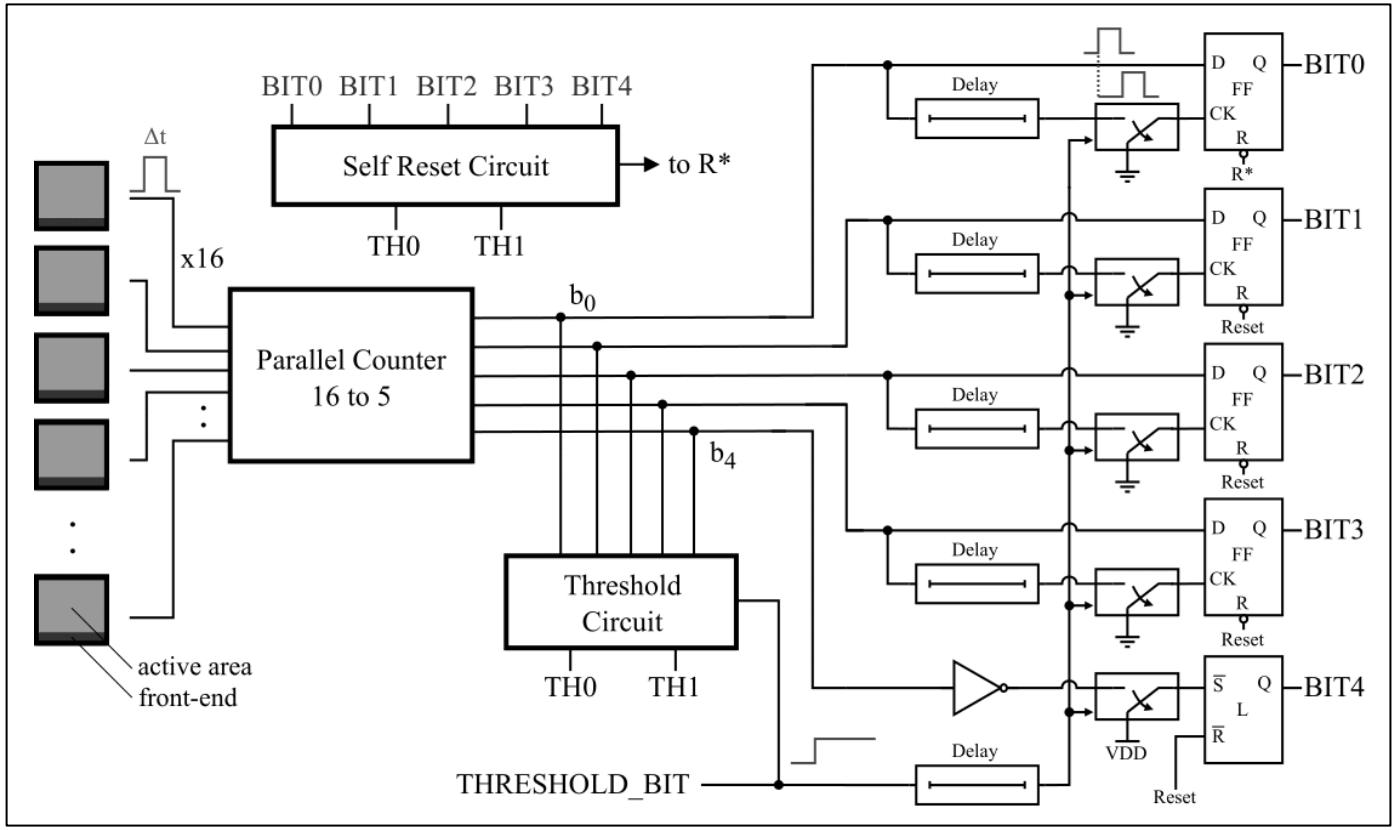
- The avalanche is quenched by means of an active network consisting of different monostable circuits.
- The hold-off time provided to the SPAD can be chosen between four values (30 ns, 70ns, 110 ns, 150 ns), through dedicated input bits.
- A memory circuit similar to the one employed in array 1 is used here.



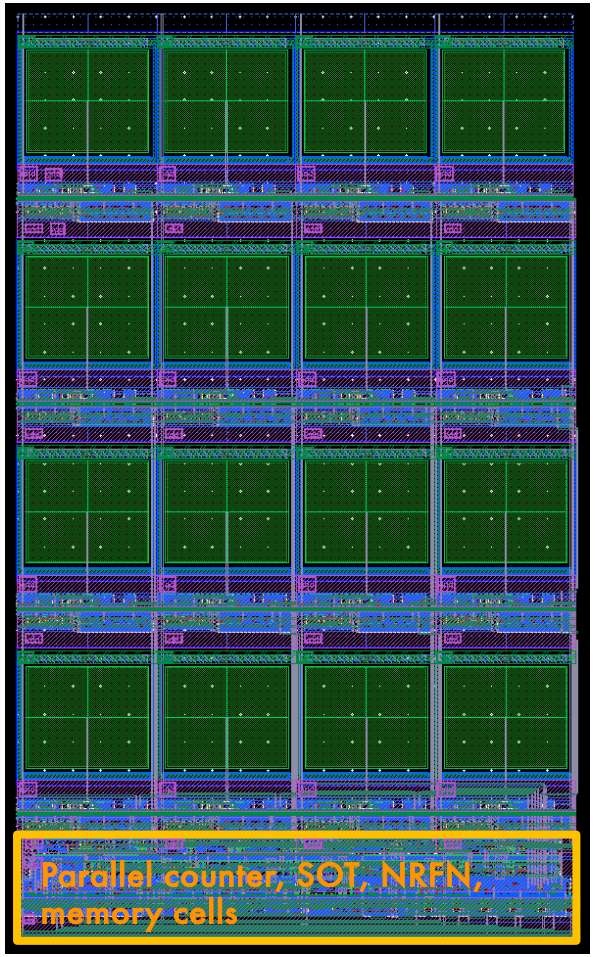


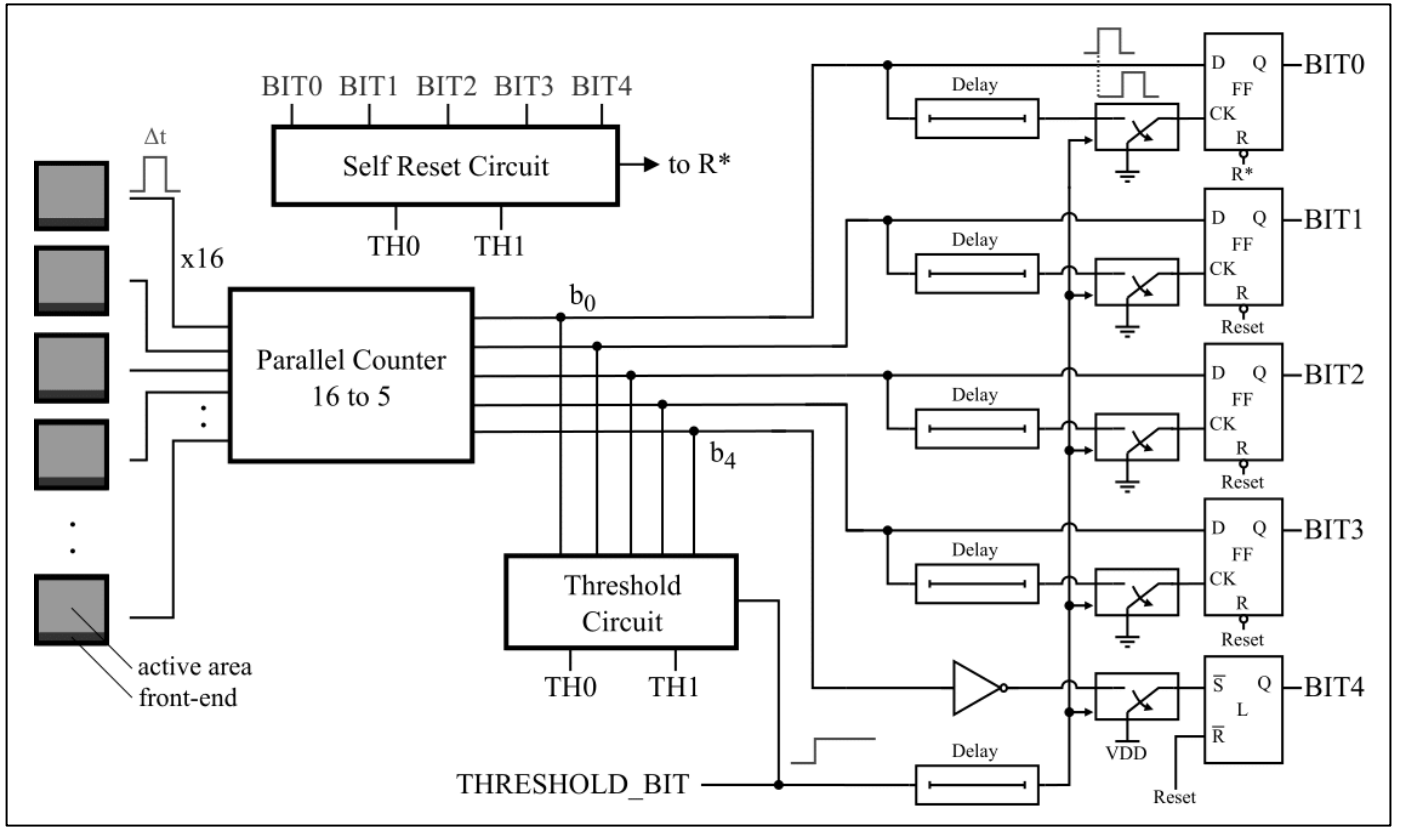
Mini-SiPM with parallel counter

- The SiPM contains **16 SPADs**, arranged in a 4x4 array, and a processing circuit.
- The 16-bit input **parallel counter** provides in **real time** the number of simultaneously triggered SPADs.
- The count result is fed to the memory elements through an **auto-triggering mechanism**, which filters out spurious glitches coming from the counter.
- A **SOT** logic has been implemented.
- A **noise rejection feedback network (NRFN)** has been designed to filter out individual dark pulses.



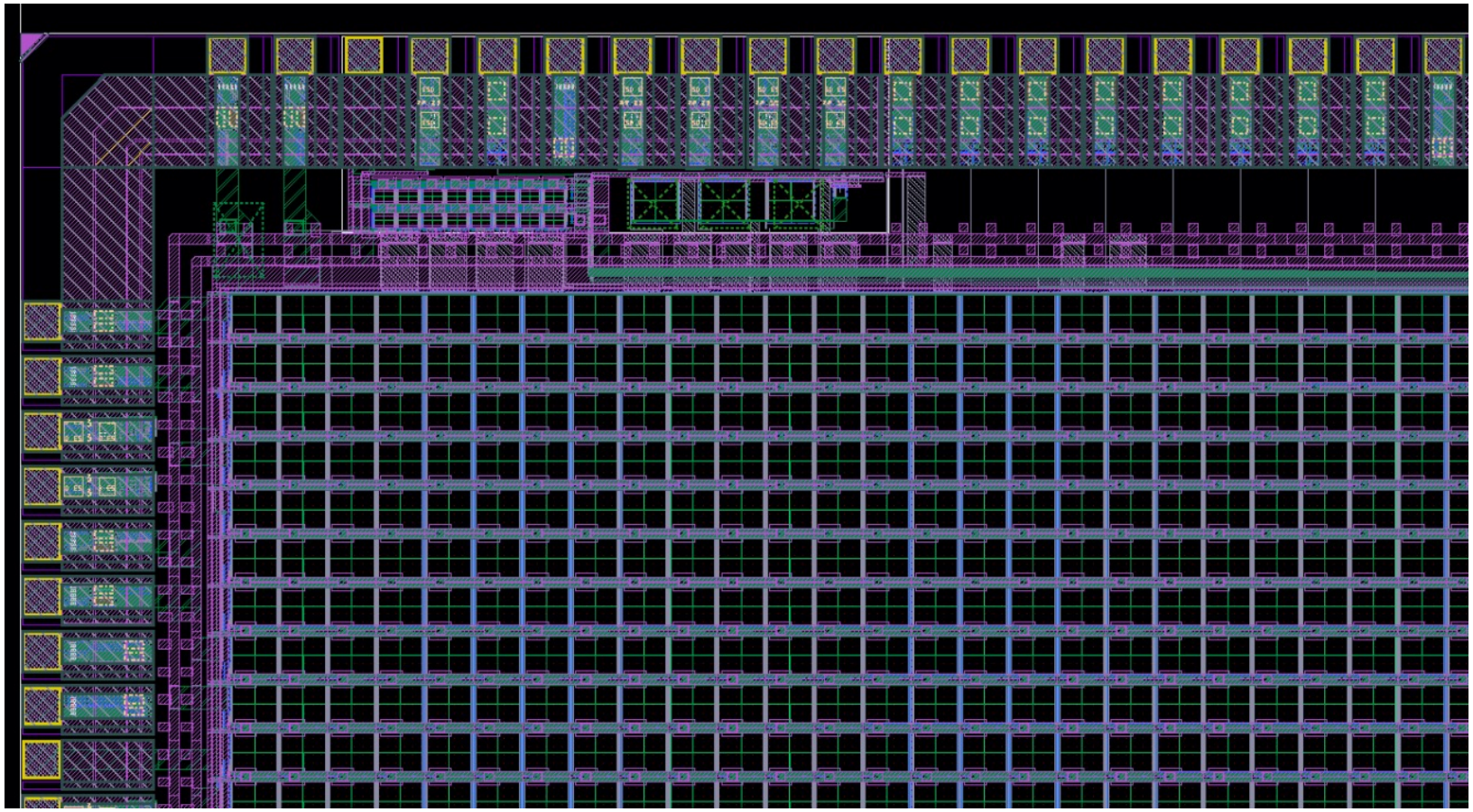
Mini-SiPM with parallel counter



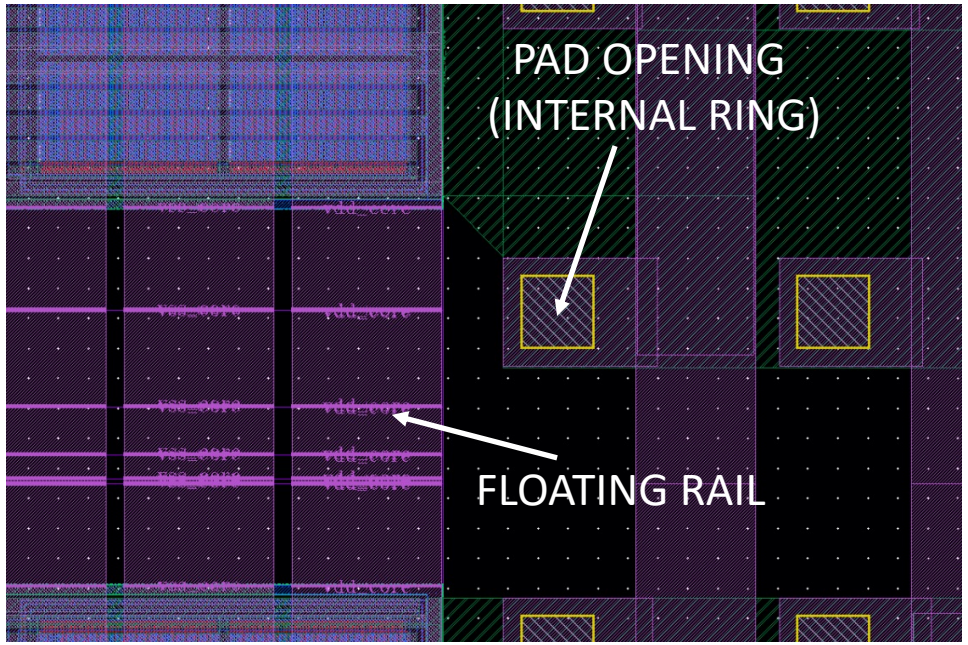


ASAP110LF chip – Design issue

- Pads used to provide VDD to the chip core do not contact the innermost rail of the pad ring → innermost rail is floating
- I/O pads consist of two sections: the driver/receiver and the configuration section, which is supposed to be biased trhough the innermost pad ring rail → I/O pads do not work

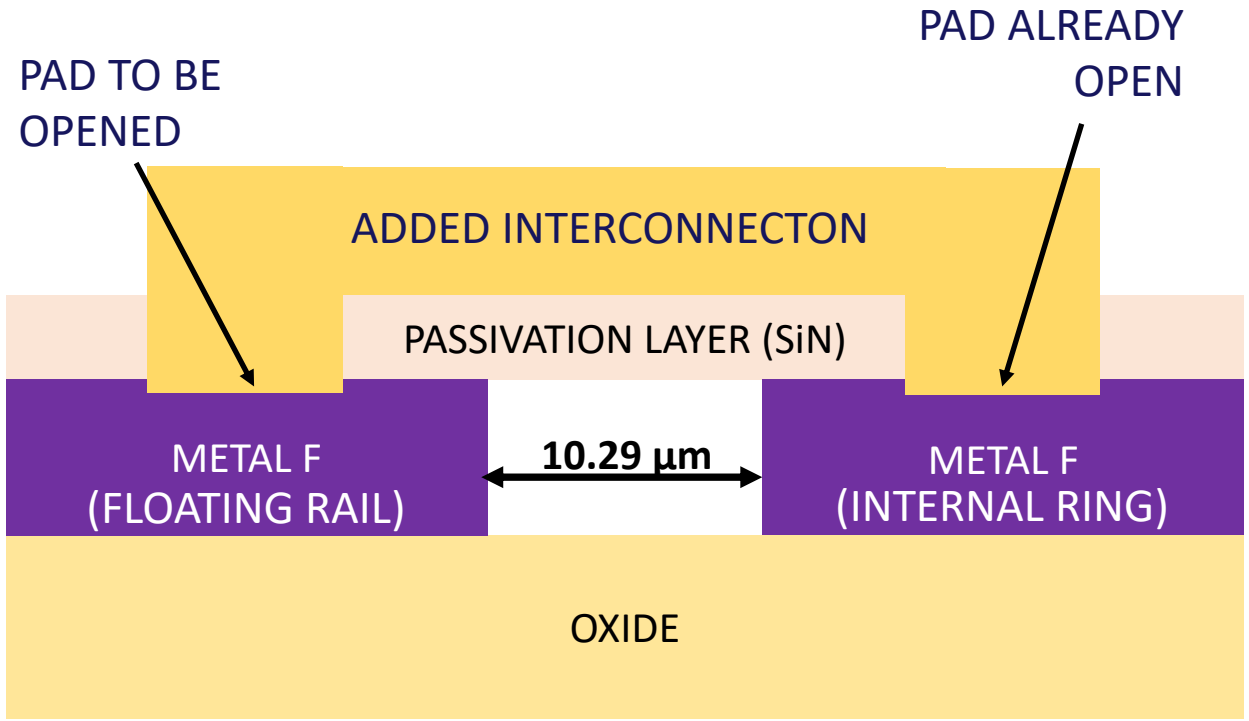


Solution: Focused Ion Beam (FIB)

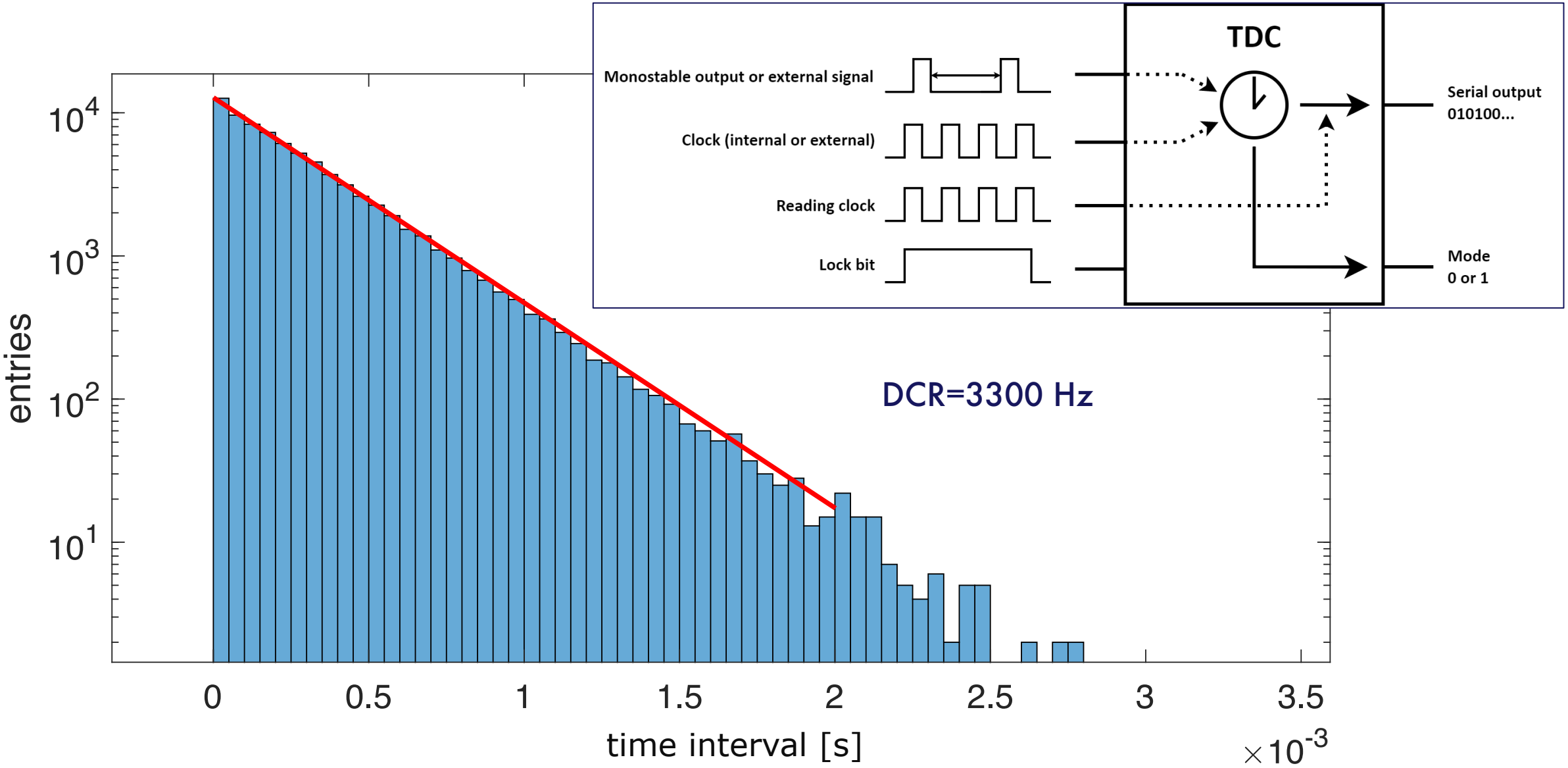


- Procedure already applied to three chips (two with two interconnections in two different points of the ring, one with a single interconnection) – it works!
- Cost: 350 Euro/interconnection + VAT

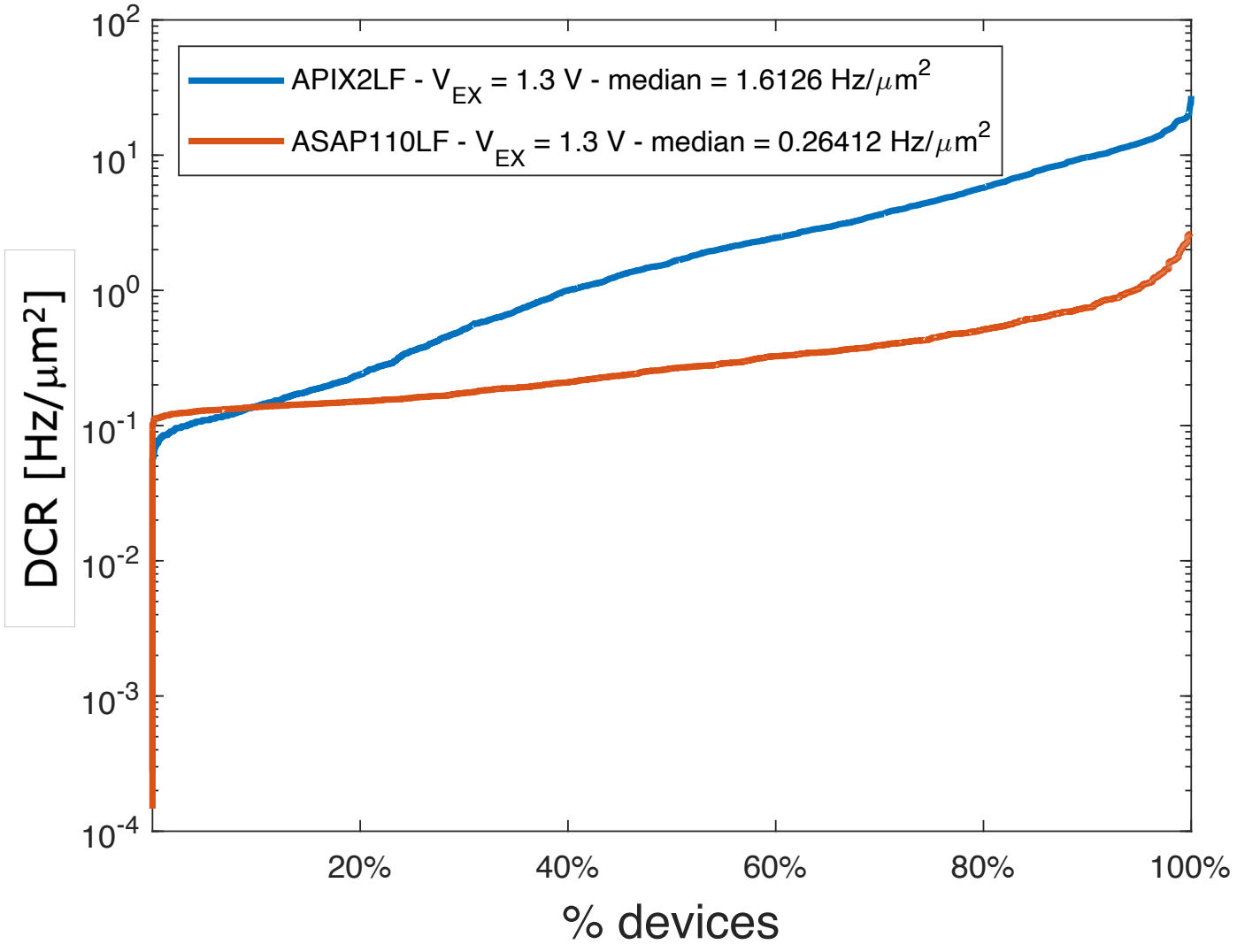
- Connect floating rail to internal ring biased to VDD → pad opening already available on one side, passivation layer to be opened on the other



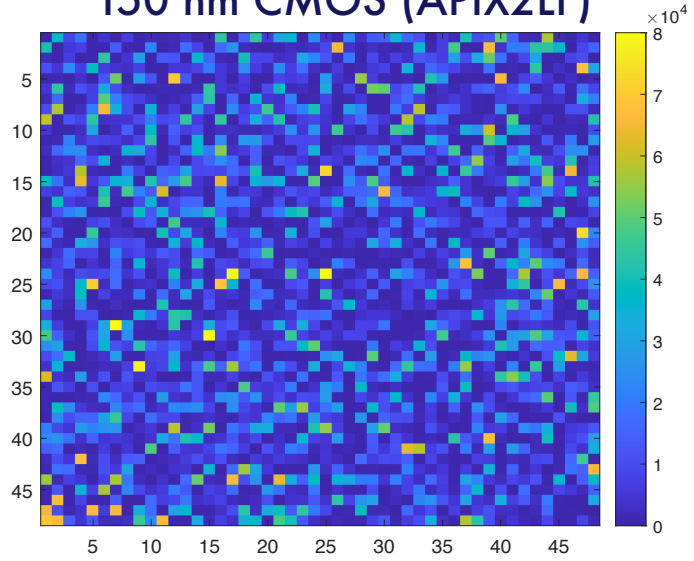
ASAP110LF chip – Time resolved DCR characterization



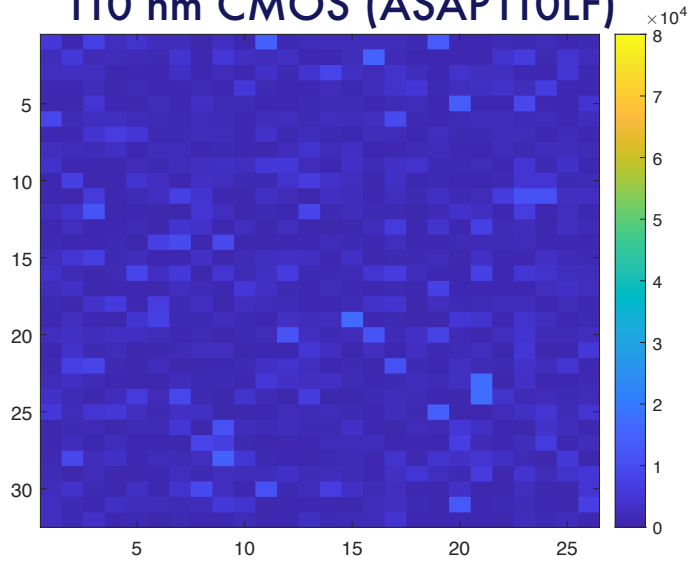
DCR in 150nm and 110 nm CMOS SPADs



150 nm CMOS (APIX2LF)

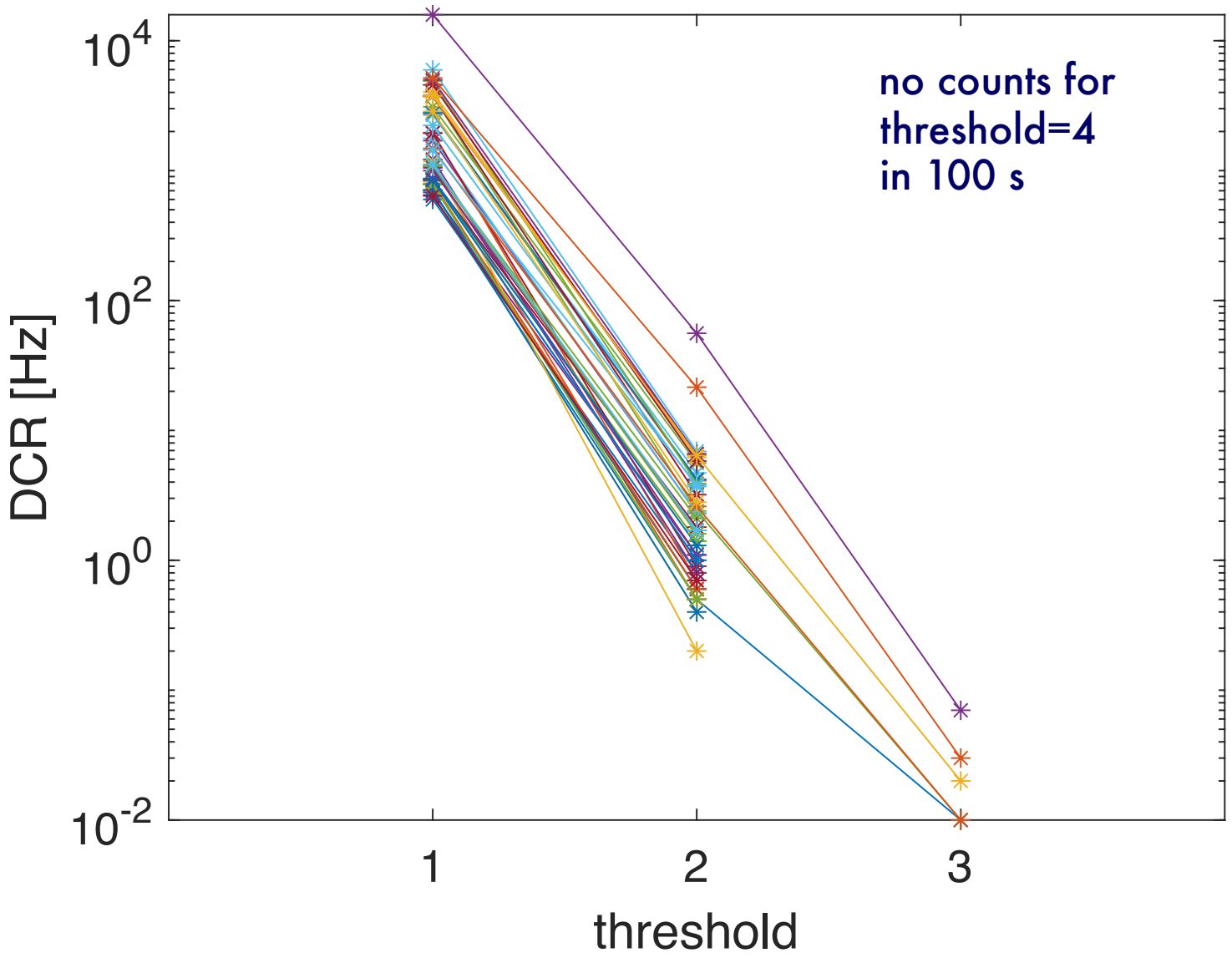


110 nm CMOS (ASAP110LF)



L. Ratti, "SPADs and SiPMs in CMOS technology"

DCR vs threshold in mini-SiPMs



Plans for future activity

- Interest in the activities of the ECFA DRD4 initiative
- Test structure characterization
  - IV curves and breakdown voltage in elementary SPAD cells, also as a function of the temperature
  - dark count rate (DCR) as a function of the bias voltage and of the temperature, including correlated noise sources, i.e., after-pulsing and inter-cell electrical and optical cross-talk
  - photo-detection efficiency
  - displacement damage and total ionizing dose effects
  - need for FIB (focused ion beam) procedure on 7 samples to recover from a design bug (about 3 kEuro, including VAT)

Plans for future activity (continued)

- Design and characterization of small scale prototypes of monolithic SiPMs including a few thousand of SPADs (targeting dual-readout calorimetry)
  - elementary cell pitch of 15-20 um
  - fully digital and mixed digital and analog approach considered to be explored – best compromise between fill factor and functional density
  - on-sensor electronics to be equipped with event detection, thresholding and time stamping capabilities, together with the ability to follow the time evolution of the light pulses
  - characterization in the lab with optical sources
- Design and characterization of a digital SiPM demonstrator
  - tentatively including 8 SiPMs, each with around 1 mm^2 area
  - processing electronics to be integrated mostly in the inter-SiPM region to minimize the impact on the fill factor
  - characterization in a beam test