Letter of Intent: DRD7
R&D Collaboration for Electronic Systems

Dr Thomas Berghauer, Chair
DRDC

31 August 2023

Dear Thomas,

The undersigned institutes intend to submit to the DRDC a proposal for a new CERN DRD collaboration to develop future electronic systems and technologies for particle physics.

As documented in the ECFA R&D Roadmap, high-performance electronic systems are a key aspect of all future detector projects. The complexity and cost of the necessary developments are high and continue to increase. Delivery of new detectors will require a greater level of coordination and better ways of cooperative working within the field, and the new collaboration will provide the platform to support this approach.

The collaboration's work will include development and demonstration of new hardware, firmware, and software concepts relevant to the requirements of medium- and long-term detector projects. The collaboration will also facilitate access to expertise, tools, and industry vendors in support of the entire DRD programme, and will act as a focal point for development of future common standards and approaches. It will support both specific technical goals in the area of electronics, and the general strategic recommendations of the Roadmap.

The collaboration will bind together the efforts of experts across a range of European and international institutes, ranging from large laboratories to individual researchers with particular expertise. Major electronic systems are now too complex for any single institute to implement alone, often requiring expertise in disparate technologies. Through adoption of open development practices and support for the sharing of IP, we will increase the efficiency and capability of all participants. The large laboratories will continue to facilitate access to advanced tools and technologies on behalf of the collaboration as a whole. The work of all DRD collaborations will be supported by adoption of common standards for IP integration and interfaces, and through well-supported workflows for system and component simulation, design, and verification. The development of new detector systems will therefore be a joint enterprise between this and other DRD collaborations, involving sharing of both people and resources.

The collaboration will initially include R&D projects in six development areas (organized as Working Groups), complementing its wider transversal role in coordination and support for which a model is being worked out:

- Data density and power efficiency (WG 7.1)

- Intelligence on the detector (WG 7.2)
- 4D and 5D techniques (WG 7.3)
- Extreme environments (WG 7.4)
- Backend systems and components-off-the-shelf (WG 7.5)
- Complex imaging ASICs and technologies (WG 7.6)

In each of these areas, we will propose a number of well-defined projects with clear development goals. Currently, 16 new projects are in preparation under the guidance of expert convenors (brief descriptions are appended to this letter). These projects will provide specific technical outputs, and act as pathfinders towards a new vision for future electronic systems based on multilateral cooperation in electronics developments. Resources to implement these projects are being, or will be, sought from national funding agencies and large laboratories. On a five-year time scale, the collaboration's vision includes, as examples:

- Establishment of well-supported IP repositories allowing sharing and reuse of IP blocks, hardware designs, and software / firmware components
- Development of software-reconfigurable front-end IP blocks and ASICs at new technology nodes, speeding up and de-risking detector system design
- Development of a new generation of components and IP blocks for powering, timing and linking the future detector front-ends
- Adoption of common standards for control, synchronisation, and readout of detector systems, reducing development time and risk
- Implementation of well-supported and cost-effective access to tools and facilities for simulation, testing and verification of monolithic imaging sensors and systems.

The collaboration currently comprises approximately **XXX** interested individuals from **YYY** institutes in **ZZZ** countries, and we are developing an agreed work plan for an initial three-year R&D phase. We aim to submit a detailed proposal for the first tranche of projects before the end of 2023. Approximately 50 institutes from 18 countries intend to contribute to these collaborative projects with an aggregated yearly effort of over 100 FTEs. The collaboration will remain open to new participants and projects, and is intended to continue and evolve in the long term.

On behalf of the collaboration,

DRD7 Steering Committee
J. Baudot, M. French, D. Newbold, A. Rivetti, F. Simon, F. Vasey

Annexes:

1. List of contributing institutes
2. List of interested institutes
3. Description of projects per working group
4. List of projects per country and institute

Annex 1: List of contributing institutes

Annex 2: List of interested institutes

Annex 3: Description of projects per working group

WG 7.1 Data density and power efficiency	Project 7.1.a	7.1.b	7.1.c
Description	Silicon Photonics Transceiver Development	Powering Next Generation Detector Systems	Wireless Allowing Data and Power Transmission (WADAPT)
Innovative-strategic vision	First opportunity to design and operate full custom optical data transmission systems in HEP detectors, co-packaged with FE electronics.	Improve power efficiency of detector systems at reduced material budget while meeting ultra-high TID tolerance. Improve efficiency of serially powered systems using switching mode shunt elements.	Wireless data and power transmission technology to connect neighboring detector layers with the aim of reducing mass and power consumption. Promising alternative to cables and optical links
Performance target	100 Gb/s per fibre optical readout (upstream) with 2.5 Gb/s control optical link (downstream). High level of radiation tolerance (1×10^{16} particles/cm2 and 10 MGy), Cryogenic temperature operation for some lower-speed variants.	-GaN DC-DC Converter: conversion factor 10, 10A, 1MHz, efficiency 95%, -Resonant Converter: conversion factor 5, 500mA, 30MHz, efficiency 75 %, -3-level Buck Converter: conversion factor 5-2, 500mA, 30MHz, efficiency 75 % -Capless-LDO: 1.1-1.2Vin, 0.9Vout, 200mA -GaN DC-DC Current Source: 48/24Vin, 10A, 200W, 2 MHz -SLDO: 1.4-2Vin, 0.9-1.2Vout, 1A Iload, 1A Ishunt	Radial wireless readout. Serialized data channels operating at 1 to 10 Gbps and aggregated across detector layers.
Multi-disciplinary, cross WG content	Combines data-density, timing distribution, back-end, as well as 2.5/3D integration. Will be first used by detectors requiring tight integration in extreme environments.	Joint effort in power electronics, ASIC and PCB design, thermal management, EMC, reliability. Necessary for all particle detector systems.	Leading to generalized use of wireless data links. Possible combination with rad tol designs for extreme environments, 4D and monolithic techniques
Contributors	**CA**: Sherbrooke **CERN** **DE**: DESY, Dortmund, KIT, Wuppertal **IT**: INFN Pisa, Sant'Anna, Trento **UK**: Birmingham, Imperial College **US**: TBC	**AT**: TU Graz **CERN** **DE**: FH Dortmund, RWTH Aachen **ES**: ITAINNOVA **IT**: UNI Udine **US**: TBC	**FR**: CEA-Leti, LPSC **IL**: Tel-Aviv **KR**: GWNU Gangneung **SE**: Uppsala
Existing resources (rough estimates, TBC)	23.2 FTE/yr 330k/yr	6.8 FTE/yr 135k/yr	2 FTE/yr 500k/yr (TBC)
To be requested resources (rough estimates, TBC)	7 FTE/yr 120k/yr	3.7 FTE/yr 37.5k/yr	70k/yr

WG 7.2 Intelligence on the detector	Project 7.2.a (TBC)	7.2.b	7.2.c	
Description	eFPGA – Programmable Logic Array IP	Radiation Tolerant RISC-V processor	Virtual electronic system prototyping	
Innovative-strategic vision	The design of radiation-hard and SEU-tolerant programmable logic gate array IP block (embedded FPGA) will introduce programmability and reconfigurability by means of software updates.	Given the growing complexity of HEP ASICs, develop a radiation-tolerant RISC-V microcontroller to reduce design and verification time while adopting an abstract design methodology and enabling programmability.	The high cost of prototyping at advanced technology nodes, as well as the complexity of future detectors, necessitate the use of design space exploration through high-level architecture studies to establish precise and optimal requirements.	
Performance target	A parameterizable FPGA fabric will be developed and prototyped: ~1000 Configurable Logic Blocks, 2000 FF, 10 SRAMS, TMR protection, ECC protection for configuration RAM and SRAM.		Transaction accurate model comprising an event generator connected with real-world physics events, and providing metrics such as readout efficiency, latency, and average queue occupancy. Reusable, easy-to-program and open access framework	
Multi-disciplinary, cross WG content	Of great interest to any detector front-end. In-depth knowledge of radiation effects on digital circuits and mitigation technique is requested.	Of great interest to any detector front-end. Joint effort on architectures and ASIC design, radiation effects and mitigation techniques, software and firmware.	Of great interest to any detector front-end. Joint effort on system design, digital circuit design and computer architecture.	
Contributors	**DE**: Dortmund **UK**: Imperial College	**BE**: KU Leuven **CERN** **DE**: Dortmund, **UK**: RAL	**CERN** **UK**: RAL **US**: TBC	
Existing resources (rough estimates, TBC)	1.5 FTE/year Funding for two mini-ASIC runs	4.7 FTE/year	2.2 FTE/year	
To be requested resources (rough estimates, TBC)	-			

WG 7.3 4D and 5D techniques	Project 7.3.a	7.3.b Timing measurements and distribution	
Description	High performance TDC and ADC blocks at ultra-low power	**7.3.b-1** Data-driven impact studies and calibration strategies for time measurements	**7.3.b-2** Timing distribution techniques and systems
Innovative-strategic vision	Detector developments with ever-increasing speed, channel density, and precise measurement of time and signal amplitude in each channel will succeed only if time or amplitude domain digitization is done at ultra-low power per channel.	First opportunity to have a common strategy between the different HL-LHC experiments for data-driven timing studies.	High precision (ps-level) deterministic clock distribution
Performance target	Short-term developments can use 130/65 nm CMOS, while smaller feature size processes like CMOS 28nm will be used for long-term applications. The performance of the ADC/TDC block, mainly speed and power, will strongly depend on the technology used, but one of the main goals for each block is ultra-low power, confirmed by a very good Figure of Merit, compared to state-of-the -art developments.	Study and propose generic data-driven calibration strategies for time measurements in detectors requiring high precision timing. These include simulations, impact studies and data-based calibration strategies of phase variations in all or part of the HL-LHC detector timing distribution tree (for example jumps due to resets in the electronics system and or temperature dependent phase drift), as well as the calibration of the front-end TDCs timewalk and non-linearities.	Develop and compare implementations on different COTS (FPGA) and custom (WR) platforms. Investigation of generic solutions to mitigate the observed limitations.
Multi-disciplinary, cross WG content	Time or/and amplitude measurement at ultra-low power is a common concern in high-density high-speed detectors for future HEP experiments.	A unified and shared approach is a prerequisite for emerging and future timing detectors	Distribution is critical and universal to all detectors requiring timing
Contributors	**FR:** IN2P3 (Omega), CEA (Saclay) **KR**: DGIST, Daegu **PL:** AGH Krakow **US:** SLAC, others TBC	**CERN**, **FR:** IN2P3-LPC, **US:** Boston, others TBC	**CERN**, **ES:** CIEMAT, Itainnova, CSIC (ICFA & IMB-CNM) **FR:** IN2P3 (CPPM, IJCLab) **UK:** Bristol **US**: TBC
Existing resources (rough estimates, TBC)	2-8 FTE/y	5 FTE/y 130k /year	
To be requested resources (rough estimates, TBC)	Needs to be sustained beyond 2024	Needs to be sustained beyond 2024	

WG 7.4 Extreme environments	Project 7.4.a	7.4.b	7.4.c	
Description	Modeling and development of cryogenic CMOS PDKs	Radiation resistance of advanced CMOS nodes	Cooling and cooling plates	
Innovative-strategic vision	Will create the critical mass needed to work on device characterisation, development of reliable models and PDK deployment on advanced CMOS processes for cryogenic temperatures	The continuous evolution of commercial CMOS technologies makes it necessary to constantly monitor the existing and emerging technology nodes	Micro-channel cooling plates are extremely efficient to remove the heat from the front-end electronics and/or sensors since the coolant is very close to the heat source. On the other hand, this technology has two main challenges: cost and integration	
Performance target	Development of models, PDKs and cryo-qualified CMOS IP blocks suitable for integration on complex mixed-signal ASICs	Rolling monitoring, surveying and benchmarking of CMOS technologies	Reduce cost of micro-channels embedded in silicon substrates by enclosing them with alternative techniques (buried channels or thermocompression). Explore the potential of ceramics as a micro-channel medium, easing the integration with fluidic connectors and possibly bringing additional electronic features to the cooling plate.	
Multi-disciplinary, cross WG content	Development of cryo-qualified CMOS IP blocks will be needed for: DRD2 (Liquid Detectors) and DRD5 (Quantum and Emerging Technologies). Results of this research project could generate potential for technology transfer.	The radiation response of MOS transistors needs to be studied from different perspectives (effects of device size, temperature, bias, dose rate, noise measurements, etc...)	Critical to dense front-ends, at the interface between electronics, mechanics and integration.	
Contributors	**AT:** Graz **CA:** Sherbrooke **DE**: Julich **IT:** INFN Torino **JP:** KEK **UK**: Oxford, Holloway **US**: TBC	**AT:** Graz **CERN** **IT:** INFN (Bergamo, Pavia),uni Padova	**DE:** DESY **ES:** CNM, IFIC-Valencia **FR:** CPPM, LAPP, LPNHE **UK:** Manchester	
Existing resources (rough estimates, TBC)	3.5 FTE/yr	15 FTE/year 340k/year	7 FTE/year (?)	
To be requested resources (rough estimates, TBC)	3.0 FTE/yr			

WG 7.5 Backend systems and COTS	Project 7.5.a COTS architectures, tools and IP		7.5.b	7.5.c (TBC)
Description	**7.5.a-1** Benchmarking heterogeneous COTS architectures for Physics	**7.5.a-2** a general-purpose repository of TDAQ tools and algorithms	No backend, full 100GbE solutions from FE to DAQ	Generic backend board
Innovative-strategic vision	Identify experiment-agnostic, common TDAQ activities, define a set of benchmarks which allows easy comparison of cost / energy efficiency of various compute architectures for the purposes of back-end / trigger processing	Make generic algorithms and tools available for easy adoption to concrete cases and give reference implementations for various architectures (FPGA, GPU, CPU, IPU and others). In combination with 7.5.a this will allow for strategic decisions to be made about future DAQ hardware, but in isolation this will serve as a repository for tried and tested 'best practice' implementations of common TDAQ components.	Implementing processors and SoCs in the Front-End may enable readout architectures based on high throughput 100Gb Ethernet linking directly the detector front-end with a switch at the backend.	Demonstrate that back-end electronics can be built using advanced COTS technologies at an affordable cost. Should provide all features needed for particle physics acquisition systems, like system clock receiver, flexible clock tree and very high precision clocks for time distribution.
Performance target and timeline	Define Figures of Merit (power, efficiency) (year 1), provide reference implementations and examples and documentation (years 2-3)	Develop a repository for firmware, software and documentation of best-practice implementations (years 1-2). In the first instance these will be inherited from the benchmark algorithms identified in 7.5.a-1 (end of year 1), and will be expanded in later years as performance gains are realised from reference implementations (year 2 onwards)	· 2023: Standard FEC-based 100GbE identification and link implementation. COTS switch evaluation versus this protocol. · 2024: FE ASIC emulator in an FPGA using RISC-V/SoC open source solutions. Proof of concept implementation. Smart-switch specifications and prototyping. · 2025: System tests. Specifications & recommendation for potential FE ASICs.	- Prototype card (Q4/23 Q1/24) - VL+ based downlinks (Q4/23 / Q1/24) -Timing distribution reception via WR (Q2/24) -Data to/from PC via PCIe (Q1/24) -Interface via 400 GbE (Q2/24) -Use as compute accelerator using HLS
Multi-disciplinary, cross WG content	Commodity TDAQ hardware is cross-experiment in nature	Will be transverse to much of the DRD program for detector specific DAQ considerations. The aim is to document algorithm implementations for multiple current, emerging and future architectures.	This activity is universal across HEP for detectors requiring high/concentrated data readout bandwidth.	A generic back-end board would be very useful for the community, in particular for smaller experiments
Contributors	**CH**: Geneva **ES**: ICTEA /U. Oviedo IP; IFIC-CSIC/U. Valencia.; CIEMAT **SL:** Joseph-Stefan Institute **UK:** Bristol, Manchester **US:** TBC		**CERN** **FR:** IN2P3-CPPM **NL:** NIKHEF **UK:** IC, STFC **US:** TBC	**CERN** **FR:** IN2P3 **NL:** NIKHEF **UK:** STFC ?
Existing resources (rough estimates, TBC)	5 FTE/yr		3 FTE/year 40k/year	5.5 FTE/year
To be requested resources (rough estimates, TBC)	To be sustained	To be sustained		

WG 7.6 Complex imaging ASICs and Technologies	Project 7.6.a	7.6.b	
Description	Common access to selected imaging technologies and IP blocks	Common access to 3D and advanced integration	
Innovative-strategic vision	The successful deployment of monolithic sensors in the community demonstrates their enormous potential. Efficient and affordable access to these technologies and IP-blocks requires concentration of resources	3D wafer stacking in foundries opens perspectives for additional functionalities, novel architectures and further integration. 2.5 and 3D integration is innovative from a system perspective and for detector integration	
Performance target	The main deliverables are: the shared PDKs, the chips resluting from the submissions and their test results. Supported technologies are: Tower Jazz 180nm, TPSCo 65nm, LFoundry 110nm.	The main mission is to facilitate the access to critical 3D integration technologies for the scientific community for prototyping and production of future detectors. For the moment it is assumed that in-foundry 3D stacking will not be prototyped before common runs in 2027 or 2028. For the in-house and third party 2.5, 3D and photonics integration the main deliverable is to make these technologies available for on-detector integration of monolithic sensors.	
Multi-disciplinary, cross WG content	CMOS sensors are considered for several types of detectors: calorimeters, trackers, etc. They require specific expertise in analog and digital IC design, device design and technology, and significant testing effort. The project is therefore transversal and multi-disciplinary.	Advanced integration technologies for CMOS sensors concern several types of detectors: calorimeters, tracking, etc. The project is therefore transversal and multi-disciplinary.	
Contributors	**CERN** **FR:** IN2P3 (IPHC, CPPM) **IT:** INFN (Torino, Padova, Milano, Bologna, Perugia, Pavia, Pisa), Trento **NL:** NIKHEF **UK:** STFC **US**: SLAC, others TBC	**CA**: Sherbrooke University **DE**: KIT, HLL Max-Plank, Dortmund, Wuppertal **US**: TBC	
Existing resources (rough estimates, TBC)	16 FTE/y 500k/y	7.3 FTE/y	
To be requested resources (rough estimates, TBC)			

Annex 4: List of projects per country and institute

		7.1.a SiPh	7.1.b Power	7.1.c wi-less		7.2.a eFPGA	7.2.b RISC V	7.2.c SysSim		7.3.a T/ADC	7.3.b timing		7.4.a Cryo-e	7.4.b Rad-e	7.4.c cooling		7.5.a TDAQ	7.5.b No BE	7.5.c Gen BE		7.6.a access	7.6.b 2.5/3D
Existing resources **TBC** FTE/year kCHF/year		23.2 330k	6.8 135k	2 70k ?		1.5	4.7	2.2		2-8	5 130k		3.5	15 340k	7		5	3 40k	5.5		16 500k	7.3
To be requested resources **TBC** FTE/year kCHF/year		7 120k	3.7 37.5k																			
Countries	# projects																					
AT:	**3**		X										X	X								
BE:	**1**						X															
CA:	**3**	X											X									X
CERN	**8**	X	X				X	X			X			X				X	X		X	
CH:	**1**																X					
DE:	**6**	X	X			X	X						X		X							X
ES:	**4**		X								X				X		X					
FR:	**6**			X						X	X				X			X	X		X	
IL:	**1**			X																		
IT:	**5**	X	X										X	X							X	
JP:	**1**												X									
KR:	**2**			X						X												
NL:	**2**																	X	X		X	
PL:	**1**									X												
SE:	**1**			X																		
SL:	**1**																X					
UK:	**9**	X				X	X	X			X		X		X		X	X	X		X	
US: TBC	**10**	X	X					X		X	X		X				X	X			X	X

Institutes	#proj-ects	7.1.a SiPh	7.1.b Power	7.1.c wi-less		7.2.a eFPGA	7.2.b RISC V	7.2.c SysSim		7.3.a T/ADC	7.3.b timing		7.4.a Cryo-e	7.4.b Rad-e	7.4.c cooling		7.5.a TDAQ	7.5.b No BE	7.5.c Gen BE		7.6.a access	7.6.b 2.5/3D
AT:																						
TU Graz	3		X										X	X								
BE:																						
KU Leuven	1						X															
CA:																						
Sherbrooke	3	X											X									X
CERN	8	X	X				X	X			X			X				X	X		X	
CH:																						
Geneva	1																X					
DE:	**6**																					
DESY,	2	X													X							
FH Dortmund,	4	X	X			X	X															X
HLL-Max-Plank,	1																					X
Julich,	1												X									
KIT,	2	X																				X
RWTH Aachen,	1		X																			
Wuppertal	2	X																				X
ES:	**3**																					
CIEMAT,	2										X						X					
CSIC-ICFA Cantabria,	1										X											
ICTEA Oviedo,	1																X					
IFIC Valencia,	2														X		X					
CSIC-IMP&CNM Barcelona,	3										X				X		X					
ITAINNOVA	2		X								X											
FR:	**6**																					
CEA-Leti,	1			X																		
CEA-Saclay	1									X												
IN2P3-CPPM Marseille,	4										X				X			X	X		X	
IN2P3-IJCLab Paris,	1										X											
IN2P3-IP2I Lyon,																						
IN2P3-IPHC Strasbourg,	1																				X	
IN2P3-LAPP Annecy,	1														X							
IN2P3-LPNHE Paris,	1														X							
IN2P3-LPSC Grenoble,	2			X							X											
IN2P3-OMEGA	1									X												
IL:																						
Tel-Aviv	1			X																		
IT:	**5**																					
INFN Bergamo&Pavia,	1													X							X	
Bologna	1																				X	
Milano	1																				X	
Padova,	1													X							X	
Perugia	1																				X	
Pisa,	1	X																			X	
Sant'Anna,	1	X																				
Torino,	1												X								X	
Trento,	1	X																			X	
Udine	1		X																			

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Institutes	#proj-ects	7.1.a SiPh	7.1.b Power	7.1.c wi-less		7.2.a eFPGA	7.2.b RISC V	7.2.c SysSim		7.3.a T/ADC	7.3.b timing		7.4.a Cryo-e	7.4.b Rad-e	7.4.c cooling		7.5.a TDAQ	7.5.b No BE	7.5.c Gen BE		7.6.a access	7.6.b 2.5/3D
JP: KEK	 1												X									
KR: DGIST, GWNU	**2** 1 1			 X						X												
NL: NIKHEF	 2																	X	X		X	
PL: AGH Krakow	 1									X												
SE: Uppsala	 1			X																		
SL: JSI	 1																X					
UK: Birmingham, Bristol, Holloway, Imperial College, Manchester, Oxford, STFC-RAL	**9** 1 2 1 2 2 1 4	X X				X	X	X			X		X X		X		X X	X X	X		X	
US Boston, SLAC Others TBC	**10** 1 2 10	 X	 X					 X		 X X	X X		 X				 X	 X			X X	X