The commissioning of the Upstream Tracker for the LHCb upgrade

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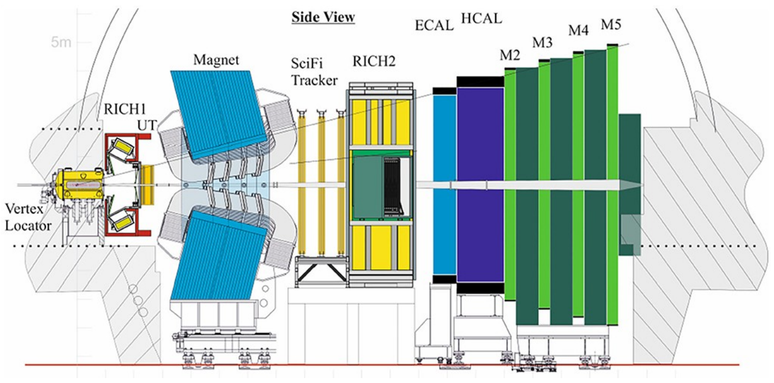
Abstract

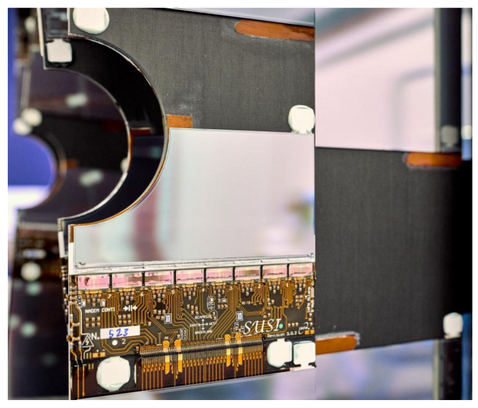
The LHCb detector has undergone a major upgrade that will enable the experiment to acquire data with an all-software trigger, made possible by front-end readout in real-time and the capabilities of performing the data selection algorithm while the data are acquired. To achieve this goal, almost all the detector subsystems have been replaced by new designs mandated by the processing speed requirements. At the heart of the real-time analysis is a fast and efficient track reconstruction, without spurious tracks composed of segments associated with hits from different charged particles. A detector crucial to the charged particle trajectory reconstruction is the Upstream Tracker (UT), a 4-plane silicon microstrip detector in front of the dipole magnet. The UT also provides a momentum measurement, as it is in magnet's fringe field. The UT comprises about 1000 sensors of four different designs, about 4000 dedicated front-end ASICs (SALT chips), performing analog processing, digitization, common-mode subtraction, and zero-suppression. Communications with the DAQ system are coordinated by a set of data control boards that also provide the optical interface. Four firmware algorithms are needed to process the UT data in the TELL40 readout boards because of the different data rates to be dealt with. We focus our report on the challenging task of ensuring that the excellent performance of the various detector components is maintained in the experiment environment and at the high rates expected. The UT was installed in LHCb in early 2023. The first year of commissioning was challenging for data synchronization issues related to specific properties of the GBTx chip. We report the lessons learned during the early commissioning phase and the upcoming run when the detector will be integrated in LHCb.

The LHCb Upstream Tracker

The Upstream Tracker (UT) is a silicon strip detector placed upstream of the LHCb bending magnet and is composed of four planes of silicon microstrips. It is critical to enable a fast reconstruction of the collision.

Four different silicon sensor designs are used to handle the varying occupancy over the detector acceptance. A dedicated front-end ASIC, the SALT chip, provides pulse shaping with fast baseline restoration, digitization via 6-bit ADCs, and digital signal processing providing pedestal and common-mode noise subtraction as well as zero-suppression.



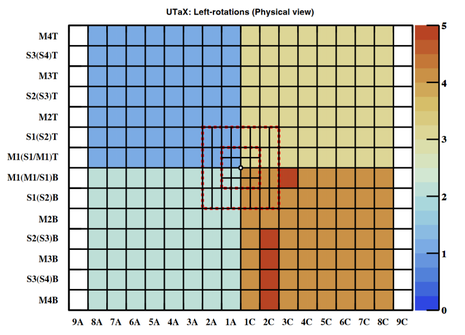


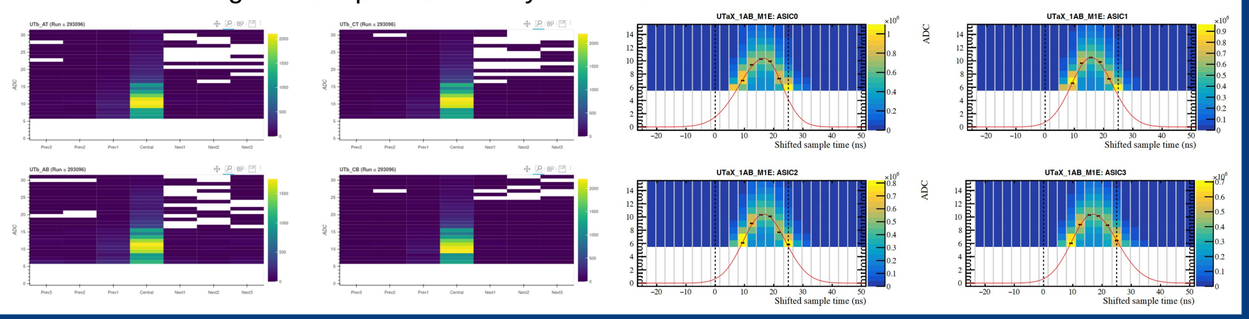
Time alignment

Time alignment was done using the TAE events produced by the LHC during its 2024 luminosity ramp-up.

Coarse time alignment makes sure that all ASICs identify a bunch crossing with its corresponding identification number within the LHC orbit. This was done per DCB card as a first approximation.

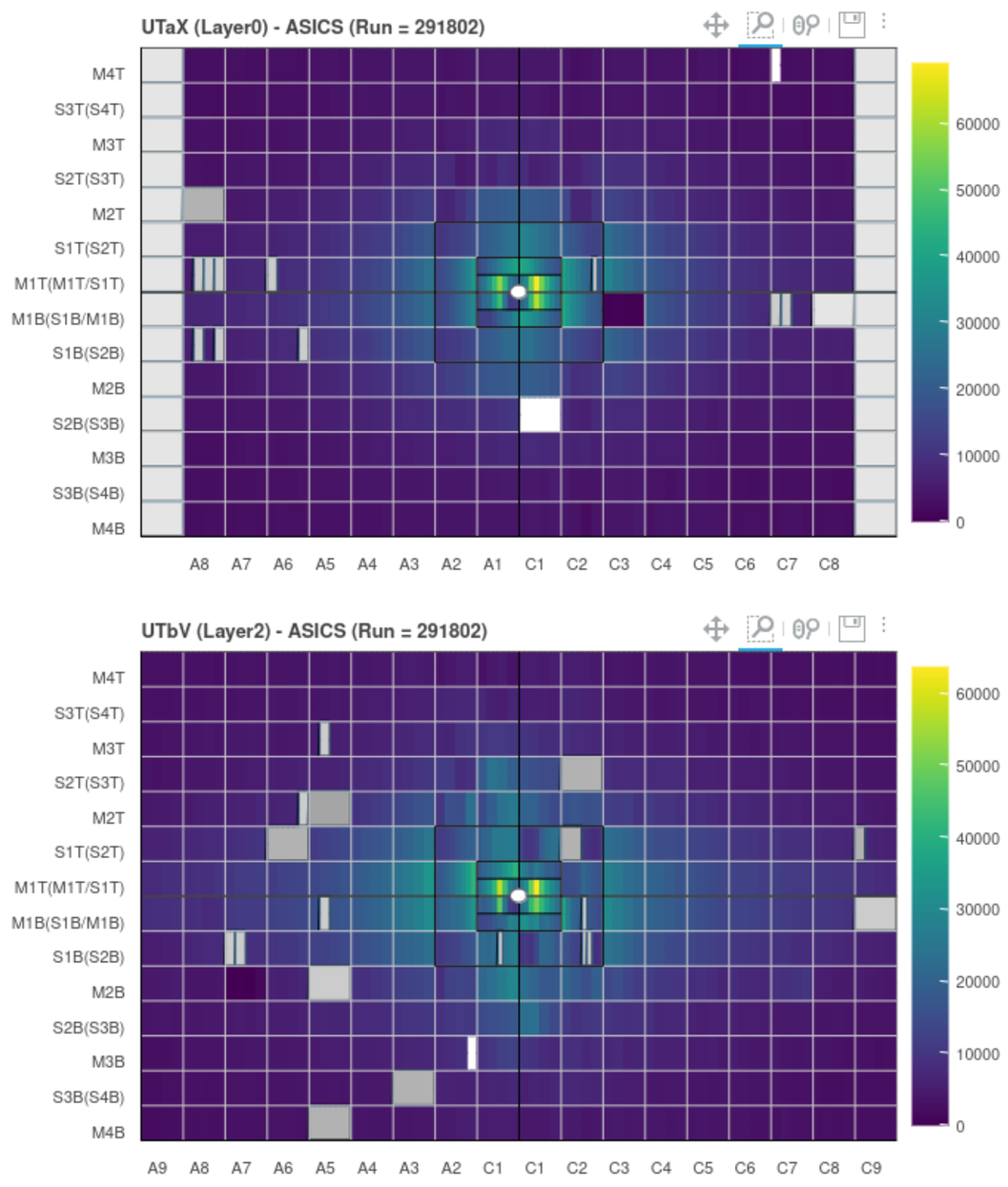
Fine time alignment was done using normal data taking, but scanning the ADC sampling phase. A signal shape measured in test beam [1] was fitted to the signal position measured in the detector. This gave us a per ASIC delay correction.





Most of the detector is working already!

The image shows a monitoring plot, each bin represents an average occupation of 128 channels (1 ASIC). This data was recorded with proton-proton collisions at nominal data rates.
The plot is computed in real time during data taking, so it is a good indicator of the detector health. Occupancy is expected to be higher in the centre-most and the central horizontal plane.
This figure shows that most of the detector is working, with a few disabled channels of different kinds and a few calibrations to be improved.



The UT features 4015 ASICs of 128 channels each, with a total of 513,920 strips in 4 layers.

Commissioning is still an ongoing task.

96.7% of the strips are already working.

4 ASICs unstable:

- White
- Case by case fixes
- Most of them should be solved soon.

2 Hybrids HW issues:

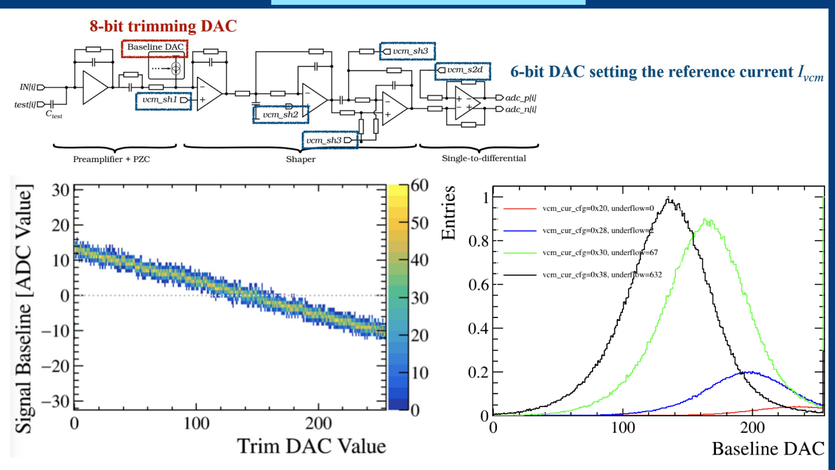
- Light gray
- Will require opening the detector.
- To be fixed in next stop

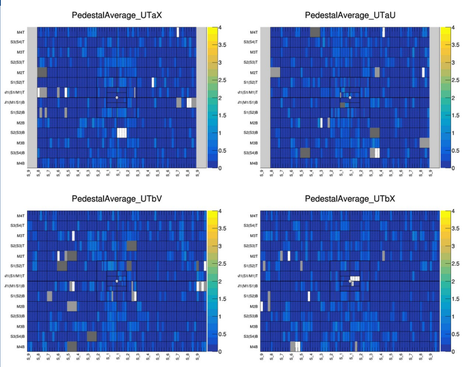
30 individual ASICs disabled, still under investigation.

A few installation issues:

- Dark gray
- Would require major intervention
- Currently not planning to fix them as risk is not worth the potential gain.

TrimDAC Scan





Each strip can be adjusted for baseline value by using the TrimDAC. [2]

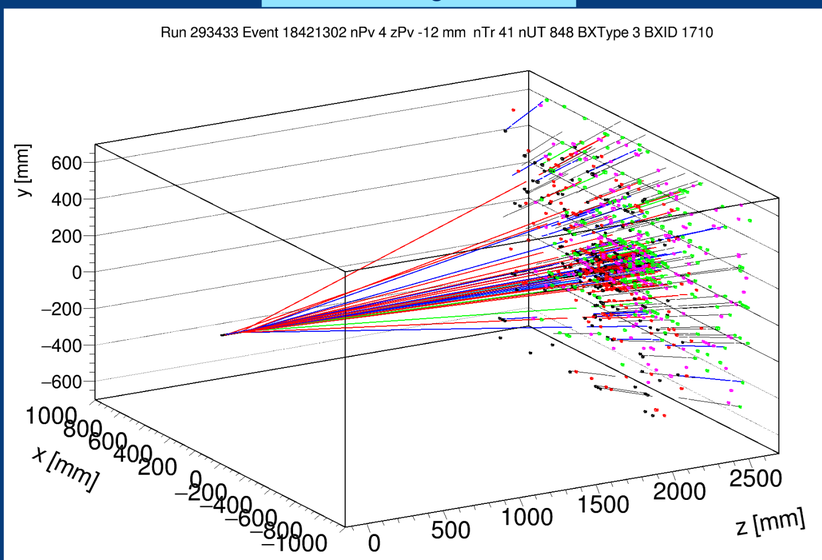
TrimDAC does not cover all cases: some ASICs require a different common mode voltage.

TrimDAC scans at different common mode voltages allow almost all ASICs to be compensated.

Only 139 channels out of 513920 had problems.

99,973% of channels working

Data in global



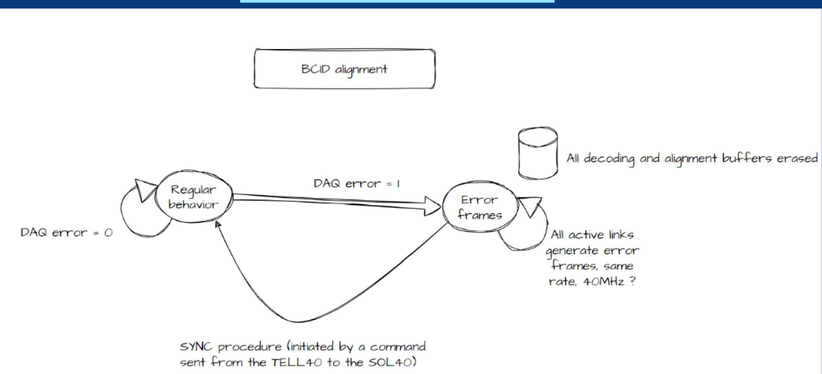
The UT is already taking data at nominal rates with the rest of LHCb.

The geometrical alignment is still a work in progress: as alignment becomes better tracking efficiency will increase. Still, this preliminary plot features one event showcasing how tracks can be projected from VELO as straight lines and get coincidences with the UT hits.

In this case, for 41 long tracks fofund in this event, 37 could be matched with UT hits:

- 10 tracks with 3 hits (black)
- 24 tracks with 4 hits (red)
- 3 tracks with 5 hits (green)

Automatic Recovery



The hardware and readout chain suffers from eventual de-synchronizations in a time scale of minutes.

Some are due to Single Event Upsets in the ASICs, some are due to problems in the readout electronics and some are not yet fully understood.

In any case, the data acquisition system and the software control are smart enough to recover most of these situations by themselves, without human intervention and minimizing the efficiency loss.

References:

[1] M. Artuso, *et al.*, *First beam test of UT sensors with the SALT 3.0 readout ASIC,* CERN-LHCb-PUB-2019-009, 2019.
https://cds.cern.ch/record/2683902?ln=en

[2] M. Firlej et al., *SALT3 chip documentation*,
https://twiki.cern.ch/twiki/pub/LHCb/StripAsic/salt_v5_spec.pdf

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