16th Pisa Meeting on Advanced Detectors

ALLEGRO FCC-ee detector concept & R&D on noble-liquid calorimetry

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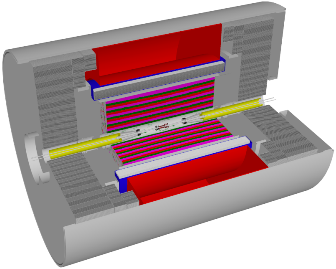
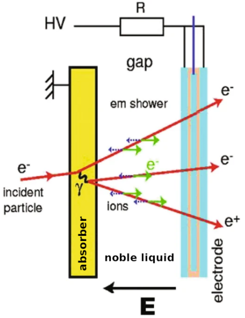
ALLEGRO detector concept

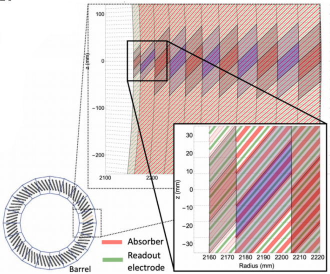
- Proposed general-purpose detector for FCC-ee
- Recently coined as ALLEGRO
  - A Lepton-Lepton collider Experiment with Granular Read-Out
- High-granularity noble-liquid ECAL a central and most studied feature
  - LAr or LKr as active medium, Pb or W absorbers
  - Multi-layer PCB as readout electrode
- Vtx detector, drift chamber and ECAL inside 2 T solenoid magnet, sharing cryostat
- HCAL and muon system outside solenoid
- Optimized for full FCC-ee physics program
  - Focus on PFlow & particle ID performance



Noble-liquid calorimetry

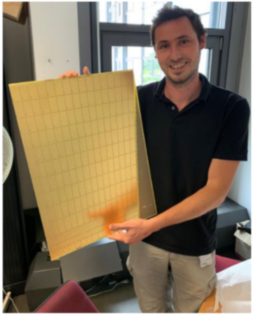
- Sampling calorimetry relying on ionization of active material (liquefied noble gas)
- Based on alternating layers of absorbers, noble liquid and readout electrodes
  - Voltage applied over noble-liquid gap
  - Incident particle ionizes noble liquid
  - e^- (and ions) drift to electrodes and induce current signal
- Successful in many HEP experiments
  - MarkII, DØ, H1, NA48/62, ATLAS
- Advantages: excellent energy resolution, linearity, stability and uniformity, good timing properties
- Challenges: complex mechanical structure inside cryostat, signal feed-through, granularity

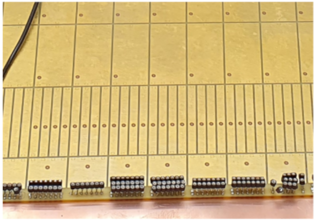


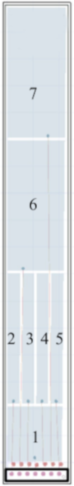


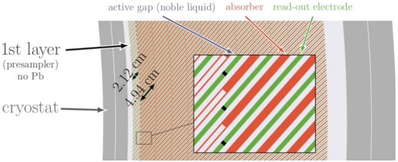
High-granularity noble-liquid calorimeter

- Printed circuit board (PCB) technology allows "arbitrarily" high granularity
  - Signal traces inside the electrode
  - Target: at least 10x ATLAS granularity
- CERN prototype PCB 58 cm $\times$ 44 cm $\rightarrow$
  - 50° inclination, gives 40 cm (22 χ_0) thick ECAL
  - Split to 16 θ-towers & 12 depth layers; 240 cells
  - Narrow strips in front for π^0 detection
  - 7-layer PCB, complex internal structure
  - Readout from inner and outer edge
- New PCB with outer edge readout & other updates to be produced shortly



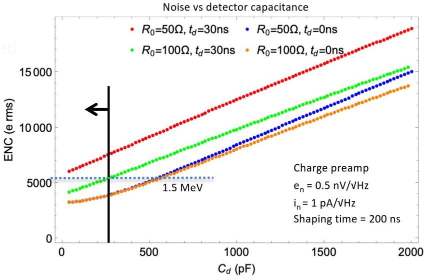


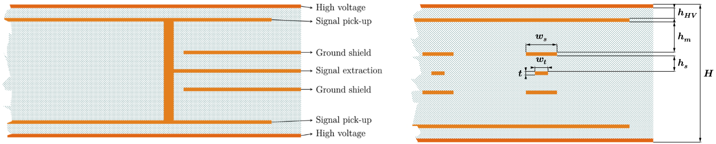


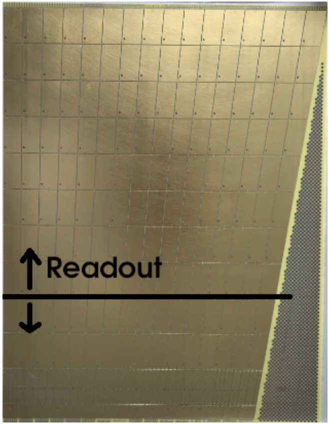


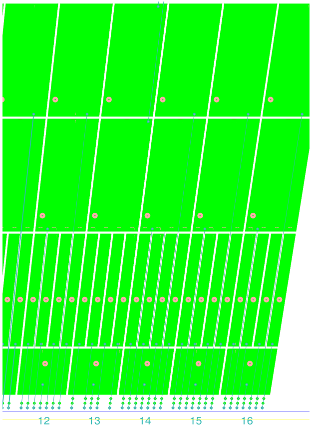
Readout electrode structure & shielding

- Signal traversing under other cells induces *cross-talk* (x-talk) that worsens resolution
- Can be mitigated by sandwiching signal traces between grounded shields
- **Trade-off between x-talk and electronics noise**
  - Shields reduce x-talk but increase capacitance to ground and hence noise
- In PCB v0 baseline is 2x width shields above and below each signal trace
  - Other configurations implemented for studies






Readout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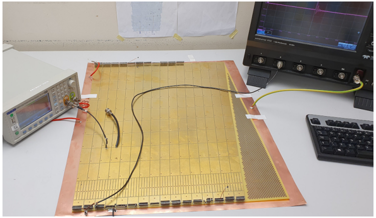
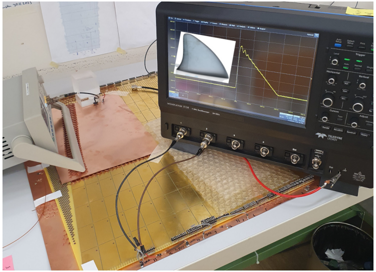
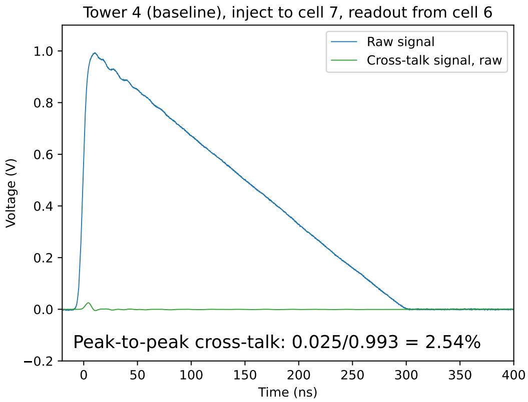
PCB measurement setup

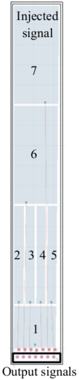
- Electrical properties measured with a table-top setup
- Copper sheet as grouding and "absorbers" above and below the electrode
- Function generator used for injecting shark-fin signal
  - 300 ns wide 1 V peak at 5 ms intervals
  - Mimics the real signal of drifting charges
- Main and x-talk signal read with oscilloscope and analyzed offline
- Extra care needed for good quality measurements
  - Short cables, thorough grounding, impedance matching





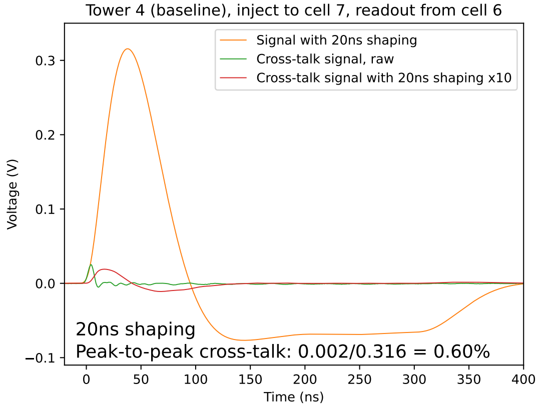
PCB measurements

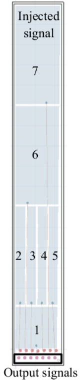




- Compare main signal magnitude to x-talk signal
- X-talk measured as "peak-to-peak" ratio
- X-talk ratio of <1% is needed and achieved with *shaping*

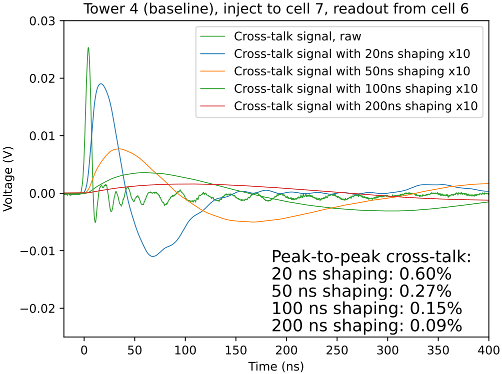
PCB measurements





- Signals shaped with ATLAS-style CR-RC^2 shaper
  - Here modeled by an analytical function
  - In reality implemented with electronics
- After shaping x-talk signal too small to see $\rightarrow \times 10$

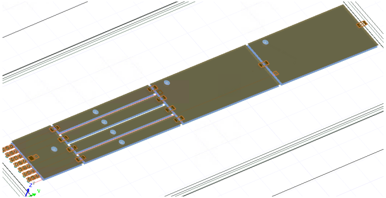
Cross-talk and shaping time

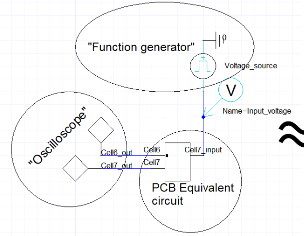


- Longer shaping time gives lower x-talk
  - At LHC long shaping times not good due to pileup, but fine in e^+e^-
- X-talk down to 0.1% and less with long shaping time
  - Also noise goes down with longer shaping time
- Low x-talk seen also in other shielding configurations

Readout electrode simulation studies

- Electrode properties also studied with simulations
  - Using Ansys Electronics Desktop
- A cut-out of the PCB taken and prepared to equivalent configuration as in the lab
  - Same conductor & dielectric materials, grounding, absorbers, input & output ports
- Model analyzed and converted to equivalent circuit, results analyzed





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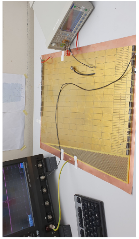
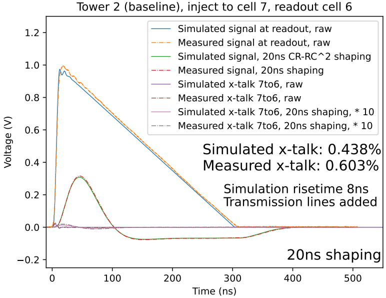
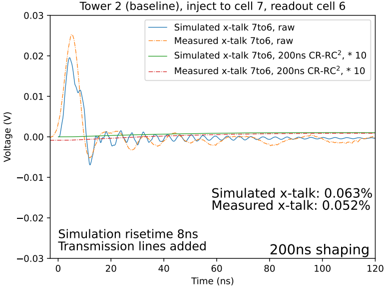


PCB simulation studies

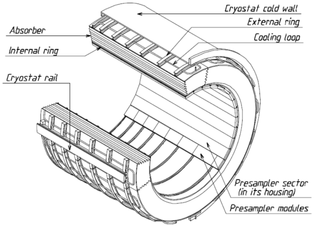
- Main signal and x-talk signal shapes in good agreement with measurements
  - Accounting for the finite turn-on of the analog signal
- X-talk in the same ballpark with 20 ns shaping
  - Exact replication of laboratory setup hard to achieve
  - With 200 ns shaping time x-talk values agree well
- Agreement sufficient for starting to try new ideas with simulations
  - Different shielding scenarios (e.g. lateral shields)
  - 6-layer PCB with one-sided or alternating shields



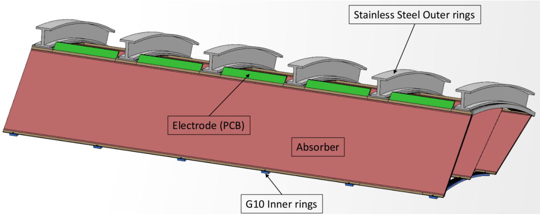


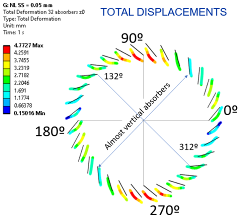
Barrel ECAL - mechanical design

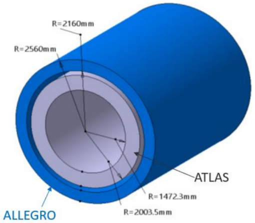
- ATLAS LAr ECAL used as reference
  - Larger radius, new electrode geometry
- Finite element analysis used for structural element design (strength, size)
- Clever solutions needed for making the structure possible to build!



ATLAS liquid argon calorimeter general layout



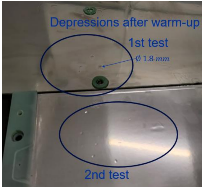


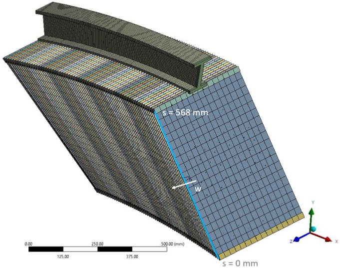


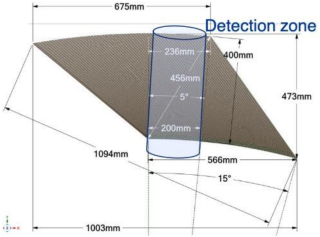
EM calorimeter size comparison

Absorbers & test-beam prototype

- First absorber prototypes produced with 1.8 mm of lead with 50 μm steel layers
- Immersed to liquid nitrogen, small depressions seen after cold test
  - Origin being investigated, thicker 100 μm steel layer being studied
- Design of test beam prototype frozen by 9/2025
  - 64 electrodes and absorbers
  - Big enough for containing a typical shower
  - To be placed in a cryostat for beam tests





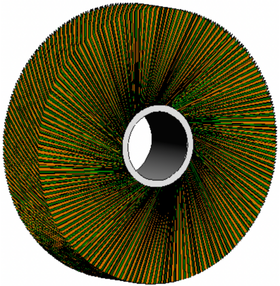


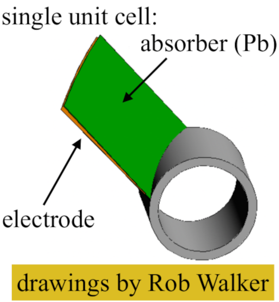
Endcap EM calorimeter

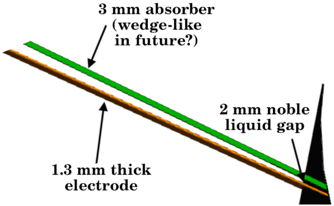
- Noble-liquid based sampling calorimeter
- ECAL endcap designed to feature:
  - Thin absorbers (high granularity)
  - Readout from outside faces only (no dead material), uniformity in ϕ

$\Rightarrow$ **Turbine-like geometry as one option**

- $\sim$240 absorbers and electrodes each
- Geometry ported to FCC-SW for FCC-ee simulations

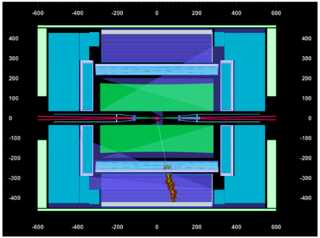


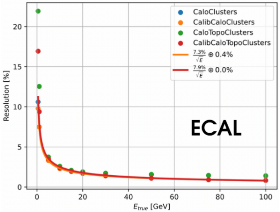


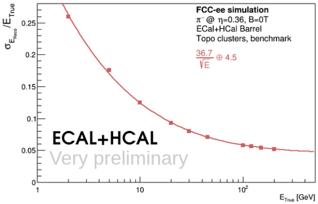


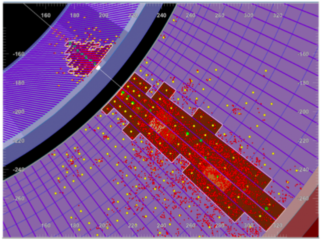
Detector simulation & clustering

- Optimal granularity & materials being studied with simulations
  - Find optimal granularity for π^0/γ separation
  - LAr or LKr as liquid, Pb or W as absorbers
- Full-Sim of ALLEGRO being built to FCC-SW
  - ECAL+HCAL topo-clustering implemented
  - Next: add tracking and Particle Flow
- EM resolution with a sampling term of 7-8% in simulation



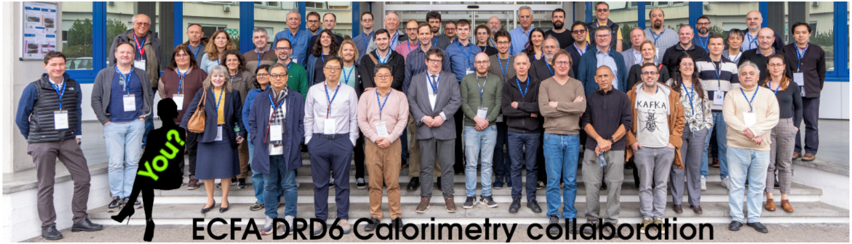




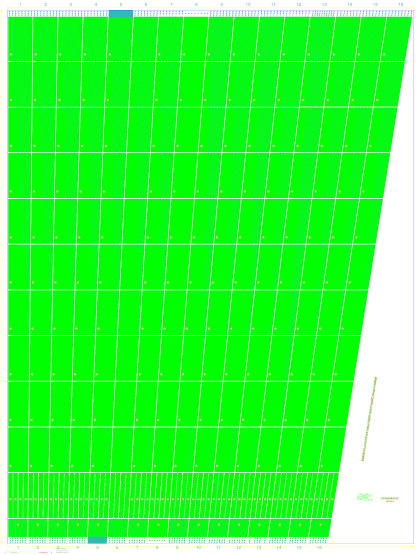


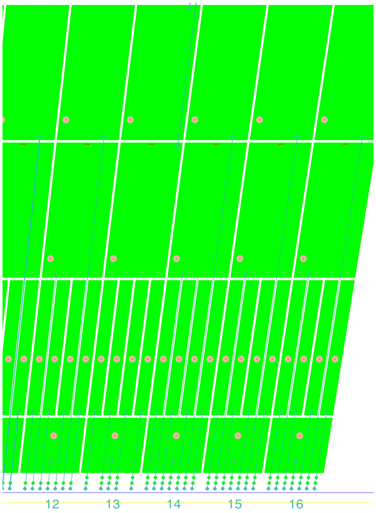
Conclusions & outlook

- ALLEGRO is a general-purpose FCC-ee detector concept
- Multi-layer PCB's as readout electrodes allow high granularity
- New prototype PCB being designed at CERN
- Test-beam prototype to be built by 2027-28
  - To be studied with test beams inside a cryostat
- ECFA DRD6 Calorimetry collaboration founded in April
  - Noble-liquid calorimetry in work package 2
- Team is growing fast, already 20 institutions joined!
  - **Ideal time to join ALLEGRO!**



Back-up

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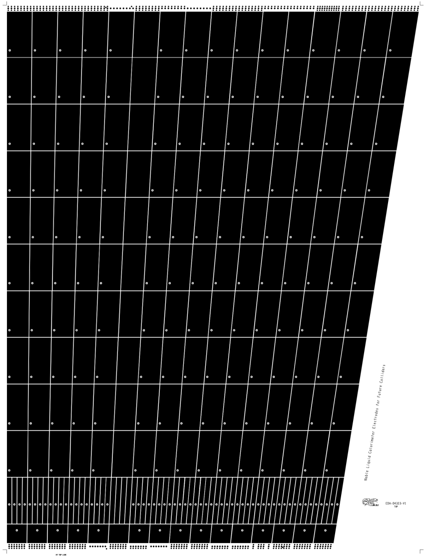
Noble Liquid Calorimeter Electrodes for Future Colliders
EDA-04323-V1
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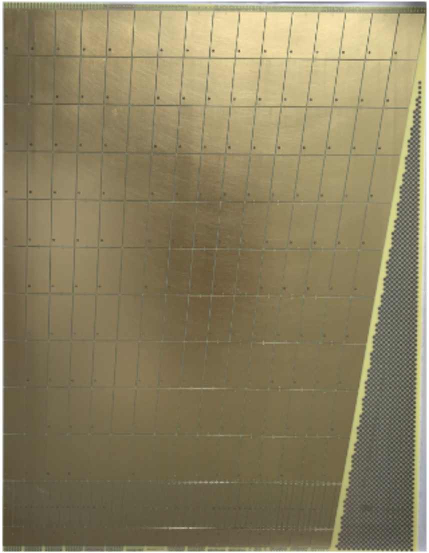
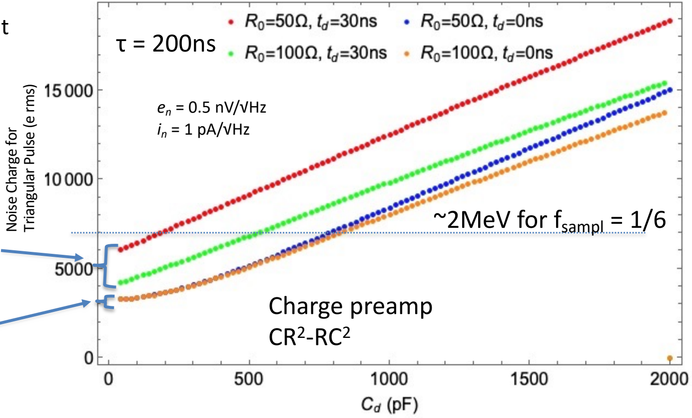


Noise as a Function of C_d and Impedance R_0

Series noise ENC scales with C_d, but **parallel noise** (independent of C_d) becomes **dominant for small C_d**.

Total noise including 5m transmission line (t_d = 30 ns)

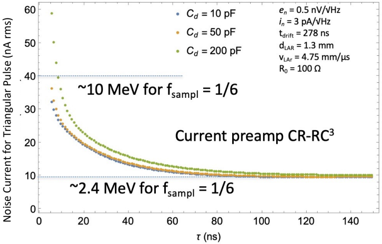
Total noise without transmission line (t_d = 0 ns)

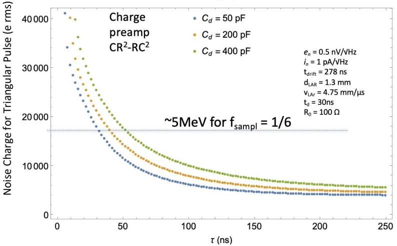


Adding a transmission line (here 5m, t_d = 30 ns) leads to **deterioration of noise**
Higher impedance (50 Ω → 100 Ω) **reduces effect** of transmission line.

Optimizing the Noise Level

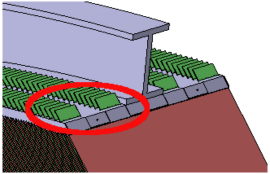
- Assume transmission line of 5 m (t_d = 30 ns)
- **R_0 = 100 Ω** is supposed to be the highest possible impedance for the coax cables leading the signal out (e.g. Axon)
  - difficult to obtain for transmission line inside the PCB
- **Current preamp (CR-RC³), see plot:**
  - e_n = 0.5 nV/√Hz and i_n = 3 pA/√Hz
  - Achieving **2.4 MeV noise** for τ > 80 ns and **R_0 = 100 Ω**
  - Achieving **3.0 MeV noise** for τ > 100 ns and **R_0 = 50 Ω**
- **Charge preamp (CR²-RC²)** generally show lower parallel noise i_n:
  - e.g. e_n = 0.5 nV/√Hz and i_n = 1 pA/√Hz
  - Achieving **1.3 MeV noise** for τ = 200 ns, C_d = 100 pF and **R_0 = 100 Ω**
  - Achieving **1.4 MeV noise** for τ = 200 ns , C_d = 200 pF and **R_0 = 100 Ω**
  - Achieving **1.8 MeV noise** for τ = 200 ns , C_d = 100 pF and **R_0 = 50 Ω**
  - Achieving **1.9 MeV noise** for τ = 100 ns , C_d = 100 pF and **R_0 = 100 Ω**
- **Only small dependence on C_d**

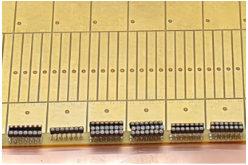


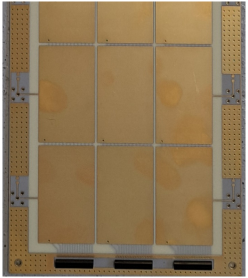


Plans for next PCB prototype

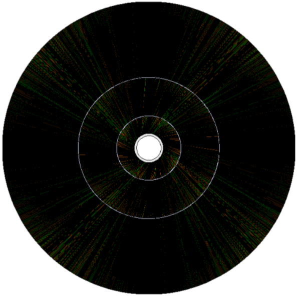
- Simulation studies underway for optimizing granularity
- Readout from outer edge only for minimizing dead material
  - X-talk of strip layer a challenge due to smaller signal
  - Singnal traces need to be "funneled" thru support structure
  - readout pins become tiny
- Would only one shield per signal strip be sufficient?
  - 6-layer PCB easier to manufacture and thinner $\rightarrow$ increased sampling ratio
- Need to re-design readout connections
  - Industry standard connector?
  - Soon results from Paris prototype $\Rightarrow$







- Another consideration is the variation of the gap with radius
  - means that response is very different at the inner and outer radii (41 cm and 275 cm)
- To mitigate this, the detector can be subdivided into a set of nested cylinders:



Tradeoff between minimizing variation in gap width vs. minimizing transitions/dead areas

In this example, each cylinder has $r_o/r_i \approx 1.9$