



ALCOR: a mixed-signal ASIC for the dRICH detector of the ePIC experiment at the EIC

Fabio Cossio (INFN Torino) on behalf of the ePIC dRICH Collaboration

31 May 2024

Frontier Detectors for Frontier Physics 16th Pisa Meeting on **Advanced Detectors** La Biodola • Isola d'Elba • Italy 26 May - 1 June, 2024

The Electron-Ion Collider at BNL

Major US project in nuclear physics, one of the most important scientific facilities for the future of nuclear and subnuclear physics

EIC will be the world's first collider with polarized electron, proton and light nuclear beams (≥ 70%)

EIC will allow to explore the secrets of QCD:

- understand origin of mass & spin of the nucleons
- provide extraordinary 3D images of the nuclear structure

Status: **approved** project progressing towards its realization at BNL, first beam operations are expected to start in the early 2030s

One experiment foreseen for now: electron-Proton/Ion Collider (ePIC)



RHIC infrastructure



The dual-radiator RICH (dRICH) for forward PID



Compact and cost-effective solution for broad momentum coverage (3-50 GeV/c) at forward rapidity $(1.5 < \eta < 3.5)$ spherical mirrors

- **Radiators**: aerogel (n ~ 1.02) and C_2F_6 (n ~ 1.0008)
- **Mirrors**: large outward-reflecting, 6 open sectors
- Photosensors: 3x3 mm² pixels, 0.55 m² per sector, in 1 T magnetic field and radioactive environment (10¹⁰-10¹¹ n_{eq}/cm² total exposure 12 y operation)

SiPM based readout

- Single Photon sensitivity ~ 10 phs per Cherenkov event
- ✓ Good timing performance < 100 ps
- ✓ Cheap and insensitive to magnetic fields
- **X** High DCR and high radiation sensitivity \rightarrow requires cooling, annealing, timing



ALCOR (A Low Power Chip for Optical Sensor Readout)

- **32-pixel** matrix (8x4) mixed-signal ASIC (4.95 mm × 3.78 mm)
- SiPM readout: single-photon time tagging
 + Time-over-Threshold or Slew-Rate
 measurements
- On-chip signal amplification, conditioning and digitization: 32-bit event word
- Fully digital output: 4 LVDS 320 MHz DDR Tx links
- Power consumption ~10-12 mW/channel
- 0.11 µm CMOS technology

Top pads							
Pix0	Pix0	Pix0	Pix0	Pix0	Pix0	Pix0	Pix0
Col0	Col1	Col2	Col3	Col4	Col5	Col6	Col7
Pix1	Pix1	Pix1	Pix1	Pix1	Pix1	Pix1	Pix1
Col0	Col1	Col2	Col3	Col4	Col5	Col6	Col7
Pix2	Pix2	Pix2	Pix2	Pix2	Pix2	Pix2	Pix2
Col0	Col1	Col2	Col3	Col4	Col5	Col6	Col7
Pix3	Pix3	Pix3	Pix3	Pix3	Pix3	Pix3	Pix3
Col0	Col1	Col2	Col3	Col4	Col5	Col6	Col7
FE biasing							
End of column							
Bottom pads							



- RCG input stage current conveyor, 2 independent TIA branches with 4 gain settings
- 2 leading edge discriminators with independent (and per pixel) threshold settings (6-bit DAC)
- 4 TDCs based on analogue interpolation with 25-50 ps time-bin (at 320 MHz clock frequency)
- Pixel control logic handles TDC operation, pixel configuration and data transmission

F. Cossio (fcossio@to.infn.it)

Pixel Front-End

Input stage

- Dual-polarity RCG current conveyor
- Programmable bias currents: CG (30-100 µA) and BOOST (1-4 mA)
- Z_{in} ~ 10-20 Ω



Output stage

- TIA gain: 2.7 kΩ
- 4 gain settings: 1/3, 4/3, 7/3 and 10/3
- DC coupled: baseline compensation based on gain and CG bias current settings + fine offset adjustment (3-bit)



F. Cossio (fcossio@to.infn.it)

Time to Digital Conversion

- Coarse time: 15-bit clock counter
- Fine time measurement performed by TDC based on analogue interpolation:
 - *fast ramp*: C_{fast} charged for time interval between the event trigger and the clock
 - $\circ~$ **slow ramp**: C_{fast} charged with smaller current, counts clock cycles until C_{slow} and C_{fast} voltages are equal
- I.F. 64 or $128 \rightarrow LSB = 25-50 \text{ ps} @320 \text{ MHz}$
- Measured time interval: 0.5 1.5 clk period
- TDC conversion time: [200, 600] ns
- 4 TDCs per pixel for event derandomization





F. Cossio (fcossio@to.infn.it)

ALCOR readout system for the dRICH prototype

ALCOR-FE-DUAL

x5.79

- Two **32-channel** ALCOR ASICs wire-bonded on the PCB
- 4 ALCOR-FE-DUAL boards for each PDU (256 channels) •
- System used for 2023-2024 ePIC dRICH beam tests •





ePIC dRICH Prototype photodetector unit (PDU)



ALCOR ASIC

cm

Laser timing measurements



→ Better time resolution with 75 µm SPADs, comfortably below σ_{t} = 150 ps also at low Vbias

Time walk correction

Time walk correction to improve overall time resolution \rightarrow studies with laser setup using *ToT* and *SlewRate* measurements



10[°] 10

ALCOR ToT mode

- ToT mode cannot distinguish between afterpulses (slow-rise time, large ToT) and cross-talk (fast rise-time, large ToT)
- **SR mode** provides better separation

ALCOR slew-rate mode



2023 test beam at CERN-PS

Successful beam test with prototype dRICH and PDUs (CERN-PS, October 2023)

- HPK S13360-3050 (3x3 mm², T = -30/-40°C)
- 20 FE-DUAL (40 ALCOR v2.0, 1280 channels)
- DAQ: Xilinx Kintex 7 KC705





Conceptual design of the final layout



Exit Face



ALCOR v3

ALCOR v2: 32-channel wire bonded ASIC ALCOR v3: 64-channel ASIC (8x8 matrix) inside BGA package (256 balls)

Operation of ALCOR at multiple of **EIC clock frequency** (98.52 MHz): digital logic, TDCs and serializers/drivers re-implemented and verified at **394.08 MHz**

The ePIC detector will take data using a **streaming data acquisition system** with no traditional hardware trigger

Digital shutter: "inhibit" pixel digital logic to reduce data throughput

- ~10.2 ns bunch crossing, ~300 ps bunch length, select 2-3 ns \rightarrow 3x-5x data reduction before ALCOR digitization
- Asynchronous digital shutter implemented in ALCOR v3 pixel logic with programmable delay to compensate offsets between the channels





ALCOR v3

Small revisions on ALCOR FE design

- Increased amplifier bandwidth to improve time resolution
 - \circ SR: 10 MV/s \rightarrow 35 MV/s
 - rise time: 11 ns \rightarrow 6 ns
 - $\circ \quad \text{ ampl: 82 mV} \rightarrow 93 \text{ mV}$
 - $\circ \quad \text{rmsNoise: } 1.6 \text{ mV} \rightarrow 2.7 \text{ mV}$
 - \circ jitter: 160 ps \rightarrow 80 ps
- Hysteresis discriminator to avoid re-triggering on slow tail with very low thresholds

Tape-out scheduled during Fall 2024







- ALCOR is a 64-channel mixed-signal ASIC developed for the readout of the SiPM sensors for the ePIC dRICH at EIC
- Several laboratory and beam tests demonstrated the ALCOR-based readout capability to measure single photons with good time resolution, fulfilling the requirements for the ePIC dRICH
- New test beam at CERN-PS ongoing now to validate the full system and evaluate its performance (with 2048 readout channels and improved timing and tracking systems
- Design of ALCOR v3 ongoing: ASIC tape-out in Fall 2024
- Irradiation tests campaign (SEU and TID) at Centro of Proton-Therapy in Trento with ALCOR v2 foreseen in July 2024

Backup Slides

ALCOR pixel operating modes



4 operating modes:

- LET: leading edge measurement
- **ToT**: Time-over-Threshold measurement using the first discriminator for both edges
- **ToT2**: Time-over-Threshold measurement using both discriminators
- SR: slew-rate measurement

Each mode can be set to:

- **FE**: normal operation mode
- FE_TP: send test-pulse to analogue front-end
- TDC_TP: send test-pulse to pixel control logic to test and calibrate TDCs (bypass front-end)

Each pixel can also be disabled

ePIC dRICH photodetector unit (PDU)



ePIC dRICH DAQ scheme











Test reproducibility of repeated irradiation annealing cycles to simulate a realistic experimental situation

- irradiation: fluence/cycle of 10⁹ neq
- annealing: in oven for 150 hours at 150 °C

Full characterisation at each step:

- new
- after each irradiation
- after each annealing



In-situ annealing:

- forward bias, ~ 1 W / sensor
- T = 175 °C, thermal camera monitor
- 30 minutes



The EIC schedule

