

Tests and Characterization of a Mixed-Signal Read Out ASIC for Silicon Micro-Strip Detectors

Friday, 31 May 2024 18:00 (20 minutes)

ASTRA-64 (Adaptable Silicon sTrip Read-out ASIC) is a 64-channel mixed-signal ASIC designed for reading out micro-strip silicon detectors. Its initial application is on serving as the read-out for the Silicon Charge Detector of the HERD experiment, slated for installation aboard the Chinese space station in 2027 to facilitate tracking and supplementary charge measurement. Designed using 110 nm technology, ASTRA-64 comprises two identical mirrored blocks, each accommodating 32 channels. Each channel integrates a Charge-Sensitive Amplifier featuring two programmable gain settings suitable for both positive and negative input signal polarities. Following this is a shaper with adjustable peaking time, allowing for noise performance optimization based on the detector capacitance. The front-end gain is calibrated to enable linear charge measurement of up to 160 fC and 80 fC depending on the gain configuration. ASTRA-64 offers two distinct readout modes. In the analog readout mode, sampled voltages are sent off-chip via an analog multiplexer linked with a differential output buffer. Conversely, the digital readout mode employs a Wilkinson ADC in each channel to digitize sampled voltages, with a shared serializer transmitting digital data through an SLVS driver. Additionally, a fast shaper, in tandem with a leading-edge hysteresis discriminator, is integrated, and the outputs of the 32 channel discriminators are merged using a FAST-OR logic to produce a rapid trigger signal off-chip. Remarkably, the ASIC's power dissipation is kept below 600 μ W per channel, aligning with stringent power consumption requirements for space applications. We will present the tests, characterization, and performance of ASTRA-64.

Collaboration

Role of Submitter

I am the presenter

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