Tests and Characterization of a Mixed-Signal Read Out ASIC for Silicon Micro-Strip Detectors

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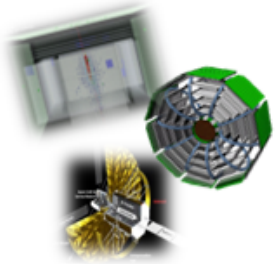
Large area Si-microstrip detectors in space

Most of space detectors for charged cosmic ray and γ-ray measurements require **solid state tracking systems based on Si-µstrip sensors.** Si-µstrip detectors are the preferred solution to instrument **large area detectors** with larger number of electronics channels coping with the **limitations on power consumption in space**



Operating Missions						
	Mission Start	Si-sensor area	Strip-length	Readout channels	Readout pitch	Spatial resolution
Fermi-LAT	2008	$\sim 74\,m^2$	38 cm	$\sim 880 \cdot 10^3$	228 µm	$\sim 66\,\mu m$
AMS-02	2011	$\sim 7\,m^2$	29–62 cm	$\sim 200 \cdot 10^3$	110 µm	$\sim 7\,\mu m$
DAMPE	2015	$\sim 7\,m^2$	38 cm	$\sim 70 \cdot 10^3$	242 µm	$\sim 40\,\mu m$

Future Missions						
	Planned operations	Si-sensor area	Strip-length	Readout channels	Readout pitch	Spatial resolution
HERD	2030	$\sim 35\,m^2$	48–67 cm	$\sim 350 \cdot 10^3$	$\sim 242\,\mu m$	$\sim 40\,\mu m$
ALADInO	2050	~ 80-$100\,m^2$	19–67 cm	$\sim 2.5 \cdot 10^6$	$\sim 100\,\mu m$	$\sim 5\,\mu m$
AMS-100	2050	~ 180-$200\,m^2$	~ 100 cm	$\sim 8 \cdot 10^6$	$\sim 100\,\mu m$	$\sim 5\,\mu m$

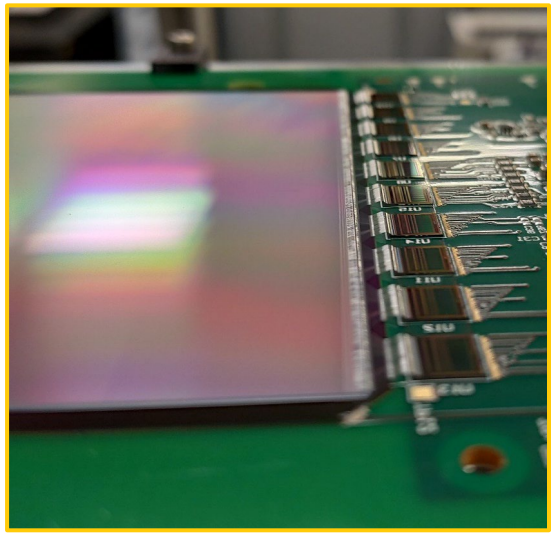
[1] HERD Collaboration. *HERD Proposal, 2018* https://indico.ihep.ac.cn/event/8164/material/1/0.pdf
[2] Battiston, R.; Bertucci, B.; *et al. High precision particle astrophysics as a new window on the universe with an Antimatter Large Acceptance Detector In Orbit (ALADInO)*. Experimental Astronomy 2021. https://doi.org/10.1007/s10686-021-09708-w
[3] Schael, S.; *et al. AMS-100: The next generation magnetic spectrometer in space – An international science platform for physics and astrophysics at Lagrange point 2*. NIM-A 2019, 944, 162561. https://doi.org/10.1016/j.nima.2019.162561

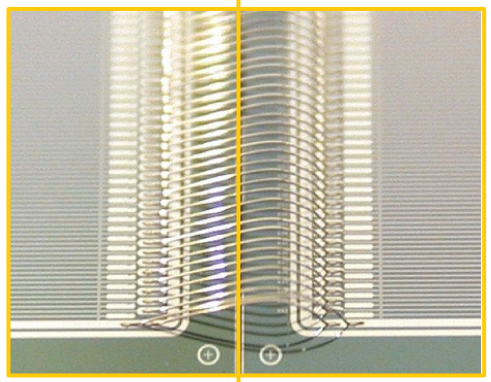
See V. Vagelli contribution: Si-microstrip LGAD detectors for cosmic-ray space-borne instruments

Silicon μStrip Detectors @ PG

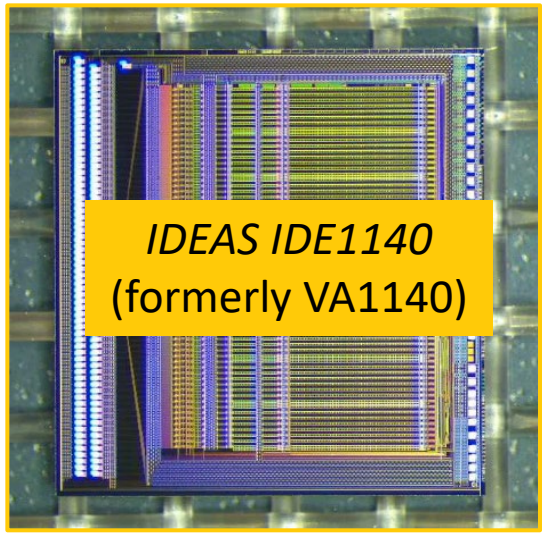
Three main components

Silicon sensors

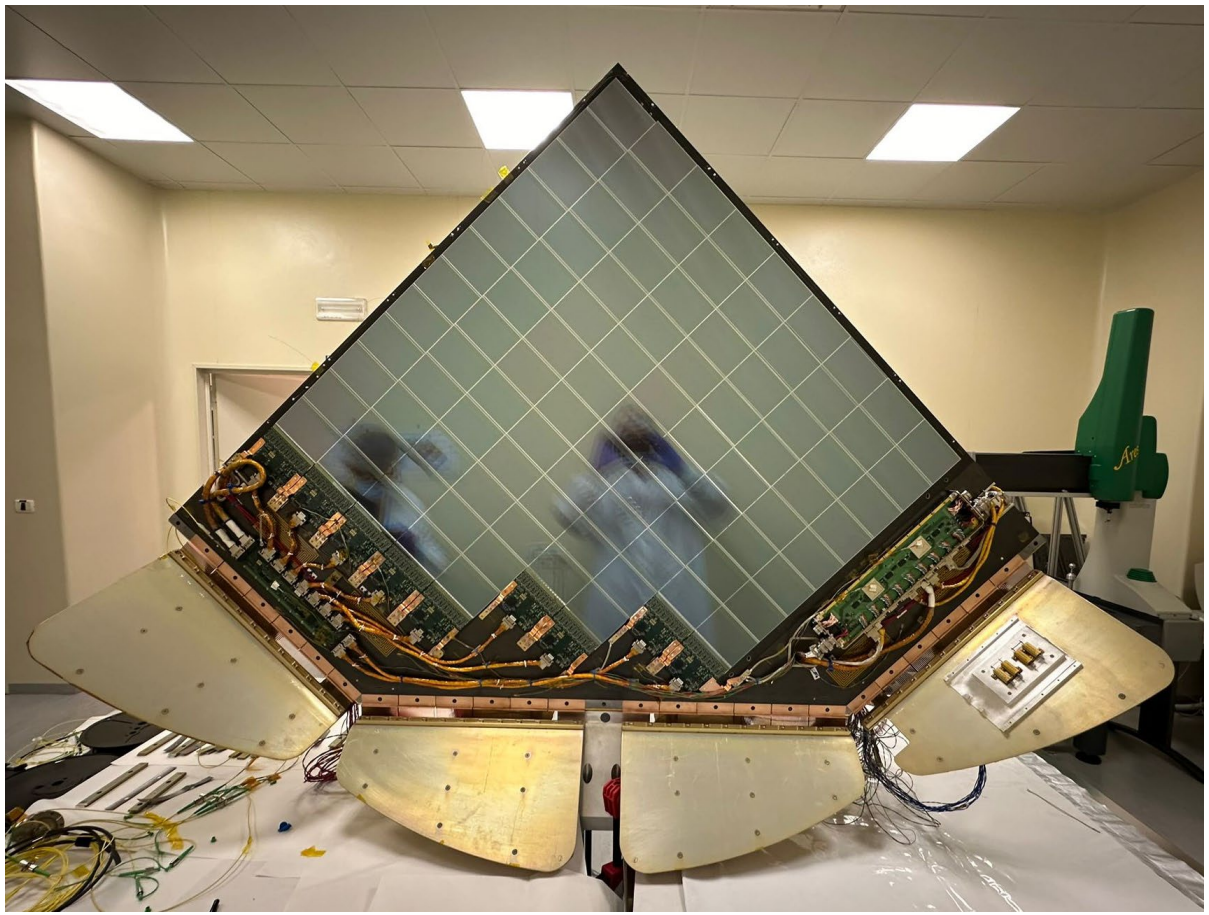


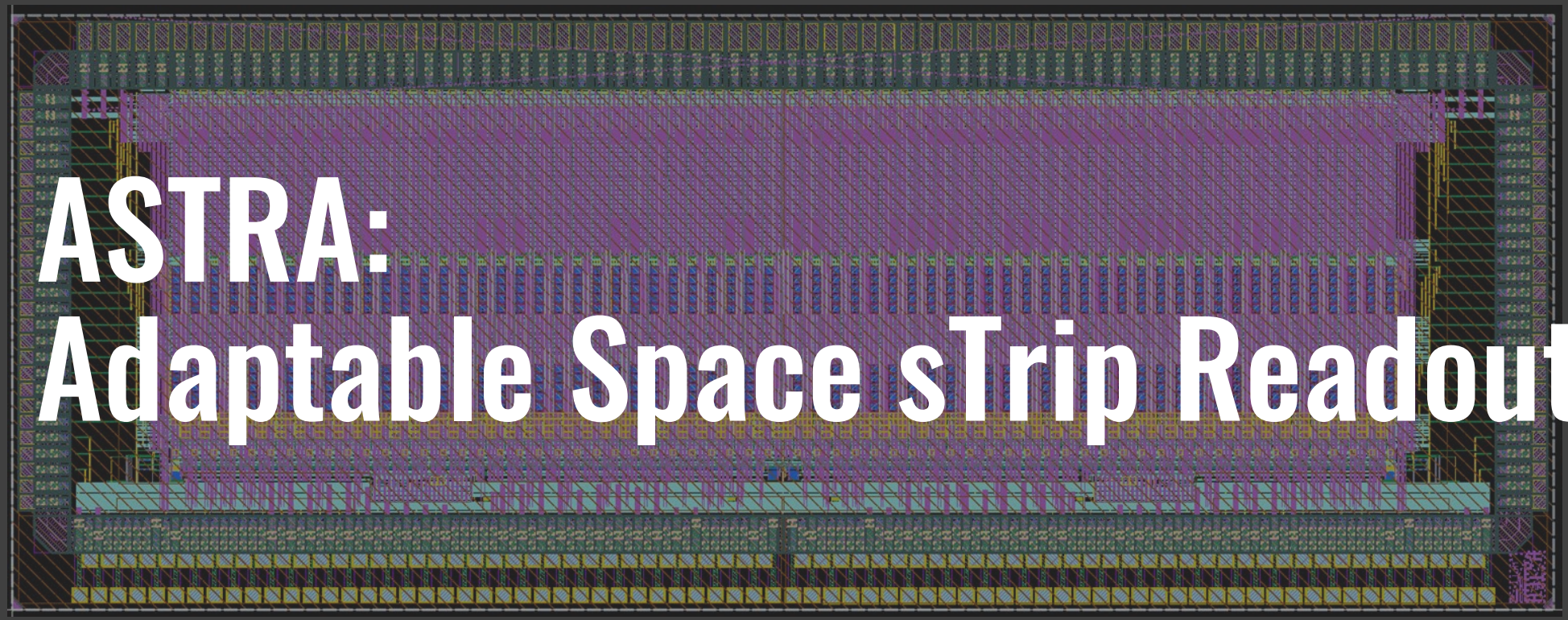


Readout ASICs



ADCs and DAQ system





ASTRA: Adaptable Space sTrip Readout ASIC

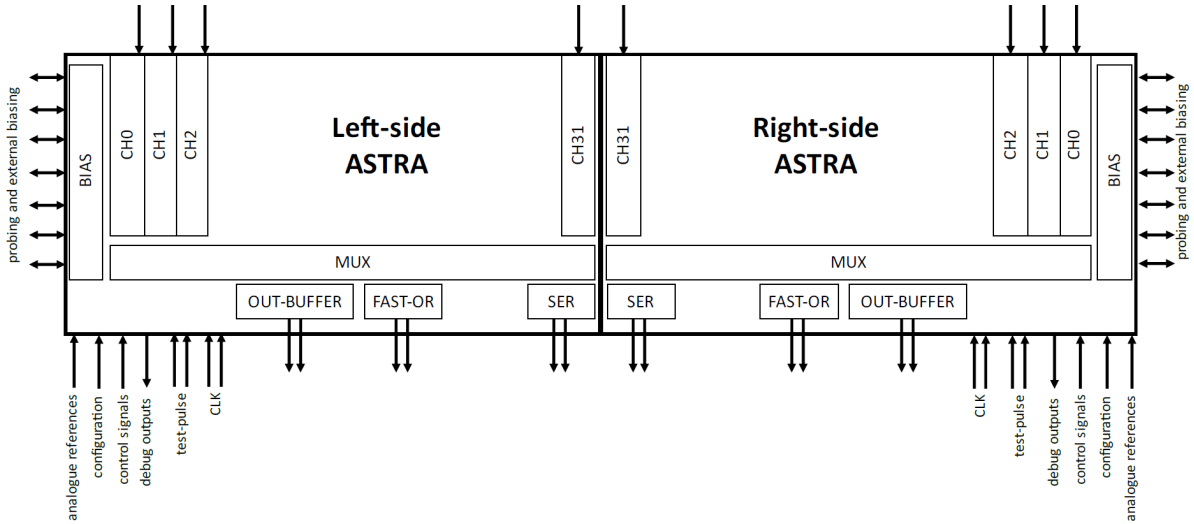
Designed by INFN Torino

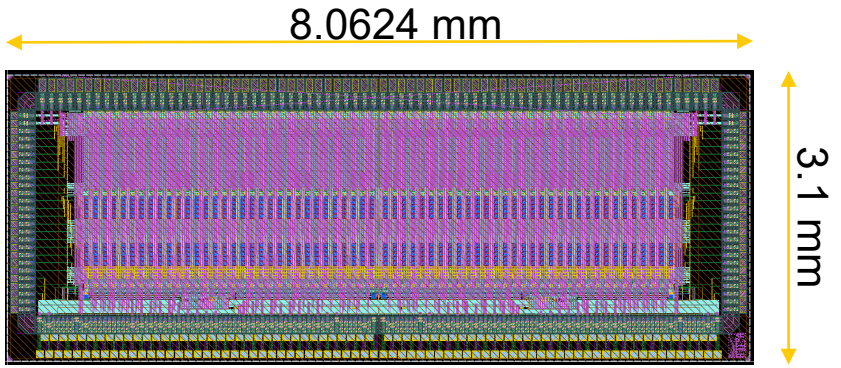
- Electronics for the read-out 110-μm-pitch silicon μStrip Detectors
- Electronics + Sensor Monolithic ASIC

ASTRA: Adaptable Space sTrip Readout ASIC

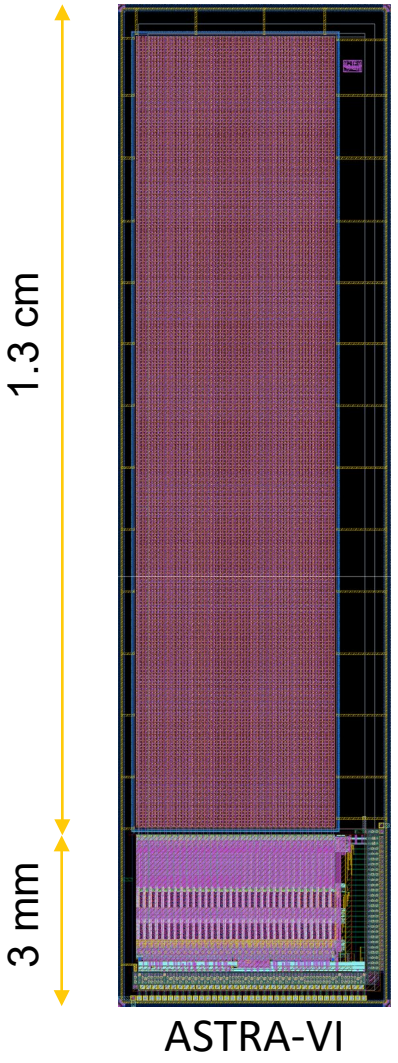
- First prototype in the framework of the INFN project ARCADIA
  - 64 channel read-out: ASTRA64
  - 32-strips fully-depleted monolithic active CMOS microstrip sensor: ASTRA-VI

- The two versions share the same electronics
  - configurable Gain
  - configurable Peaking Time
  - configurable Readout mode (analog or digital)





ASTRA64



ASTRA-VI

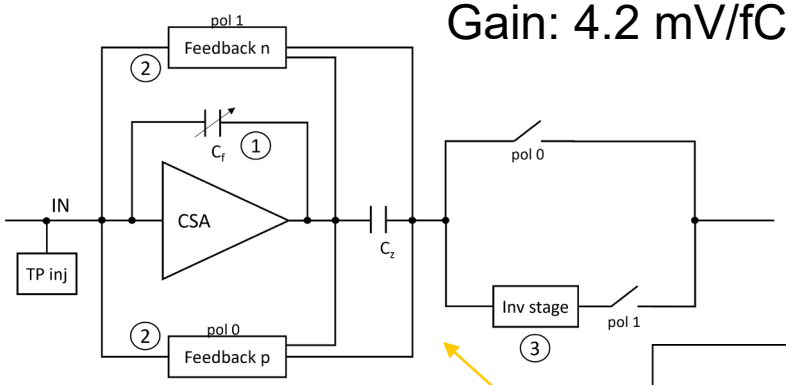
ASTRA Requirements

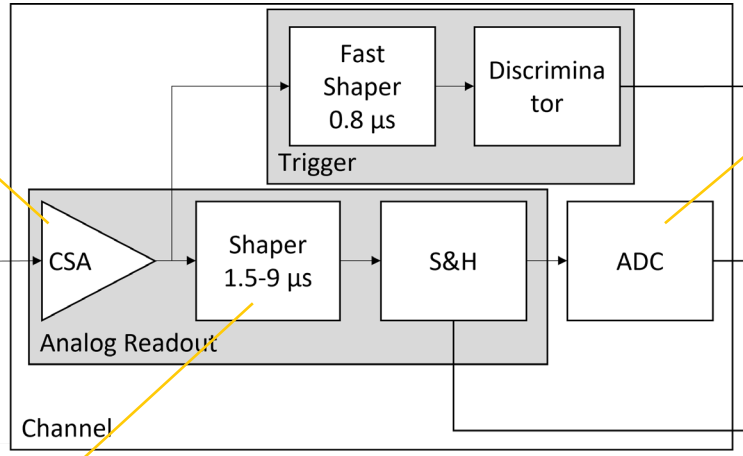
	ASTRA Requirements
Channels	64
Dynamic Range	± 160 fC
Linearity Region	± 160 fC
Shaping Time	Adjustable in 1÷10 μs
ENC	< 1000 e^- @ C_{in} 100 pF
Output	Multiplexed pulse height Digitized pulse height Channels FastOR
Power supply	Positive (only) supply
Channel power consumption	< 1 mW per channel
Production Process	110 nm CMOS
Size	6x6 mm^2

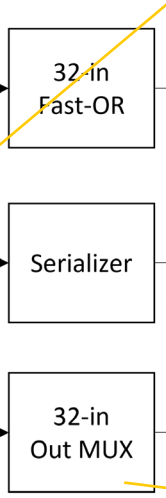
- Requirements tailored to HERD Silicon Charge Detector (SCD)
- Produced at LFoundry
  - Only HVT transistors (1.2 V) available

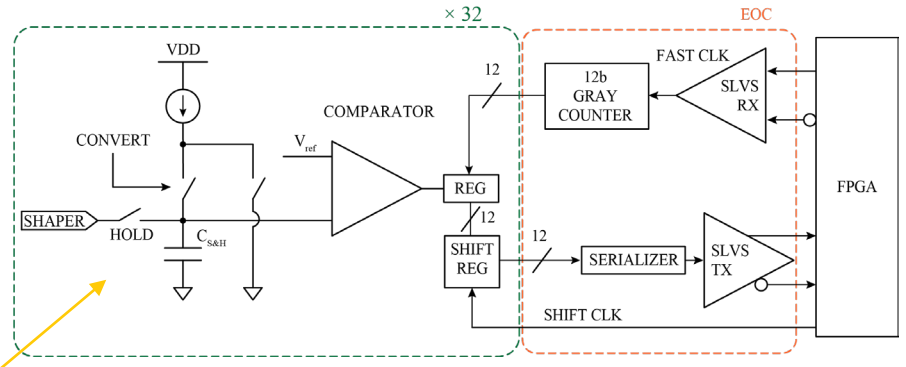
ASTRA Architecture

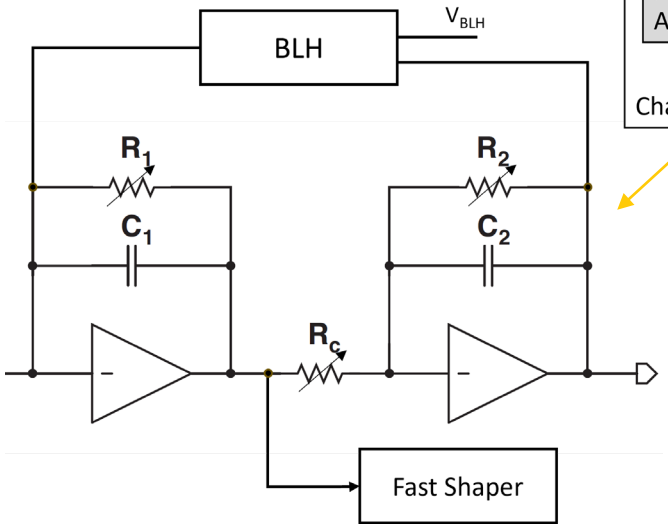
Gain: 4.2 mV/fC, 7.6 mV/fC

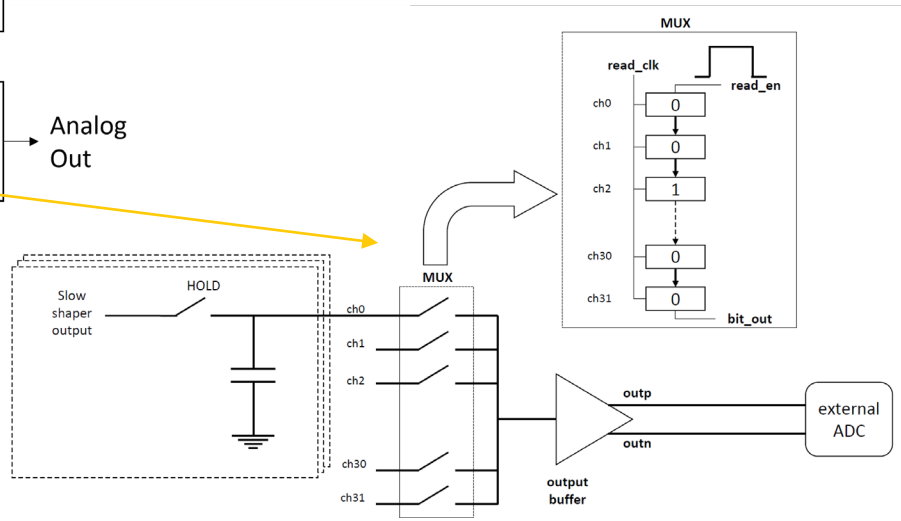




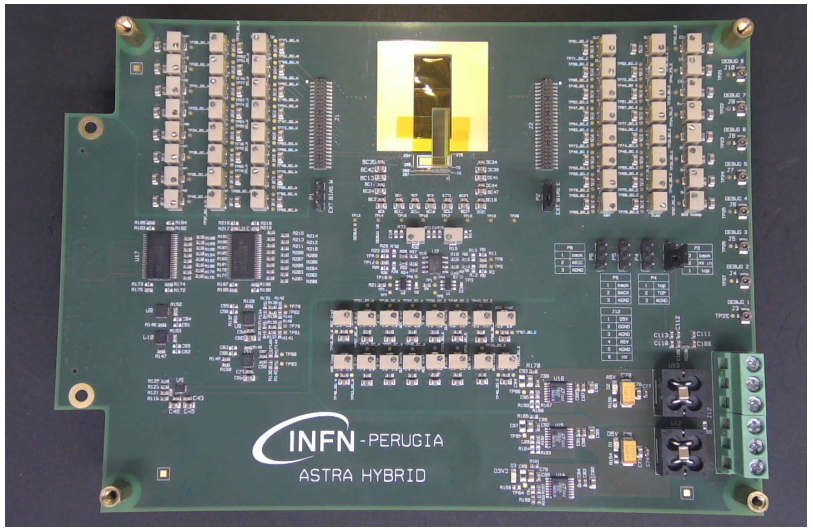




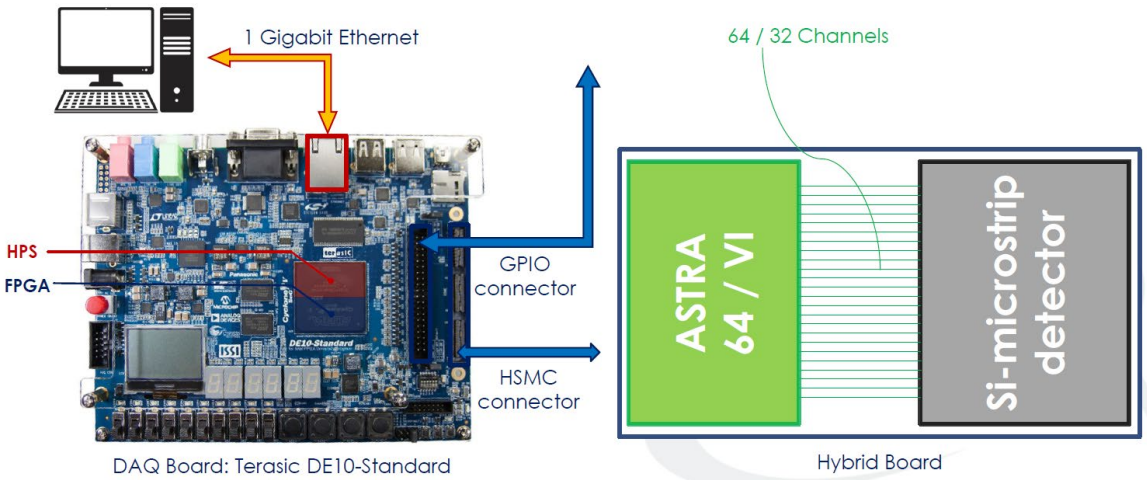




ASTRA Test Board and DAQ



- ADCs for analog output digitization
- Analog/Digital Power Supplies
- Level shifters and SLVS converters
- Can accommodate both ASTRA-VI and ASTRA-64
- Trimmer resistors for external bias
- Sensor HV bias



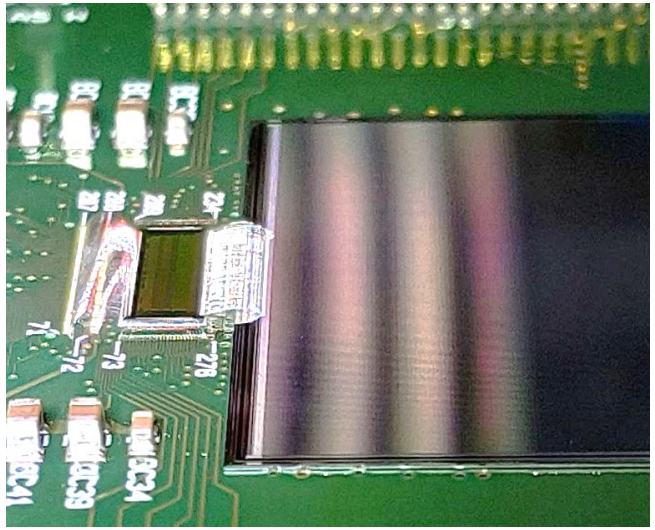
DAQ

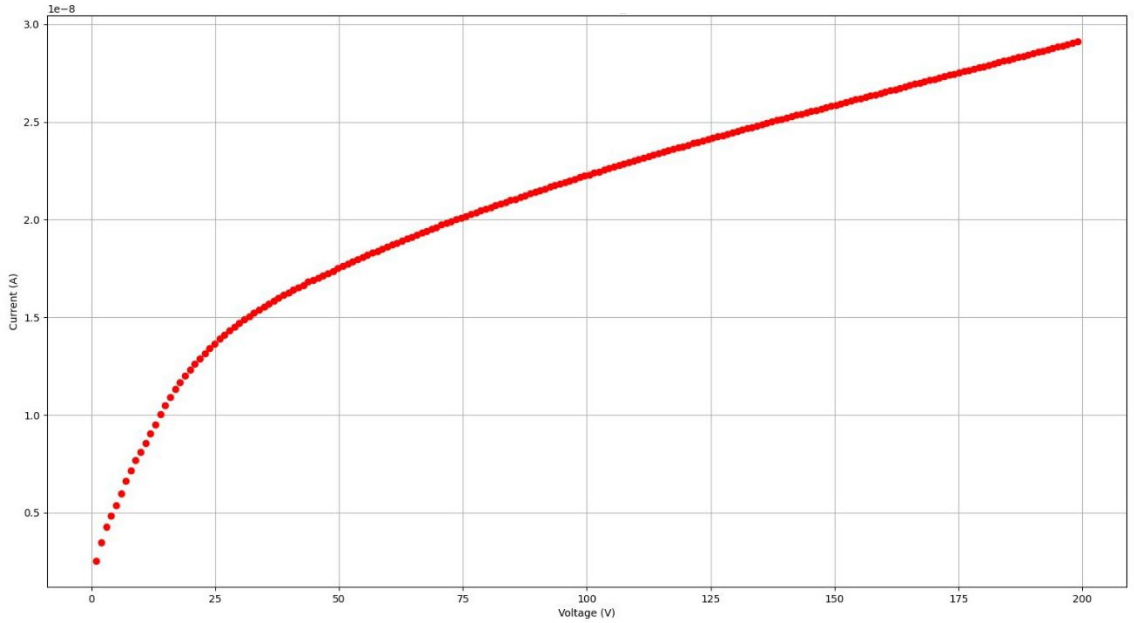
- ASTRA configuration, readout operations, and data acquisition
  - *Terasic DE10-Standard*
    - *Intel Cyclone V* FPGA

ASTRA Characterization

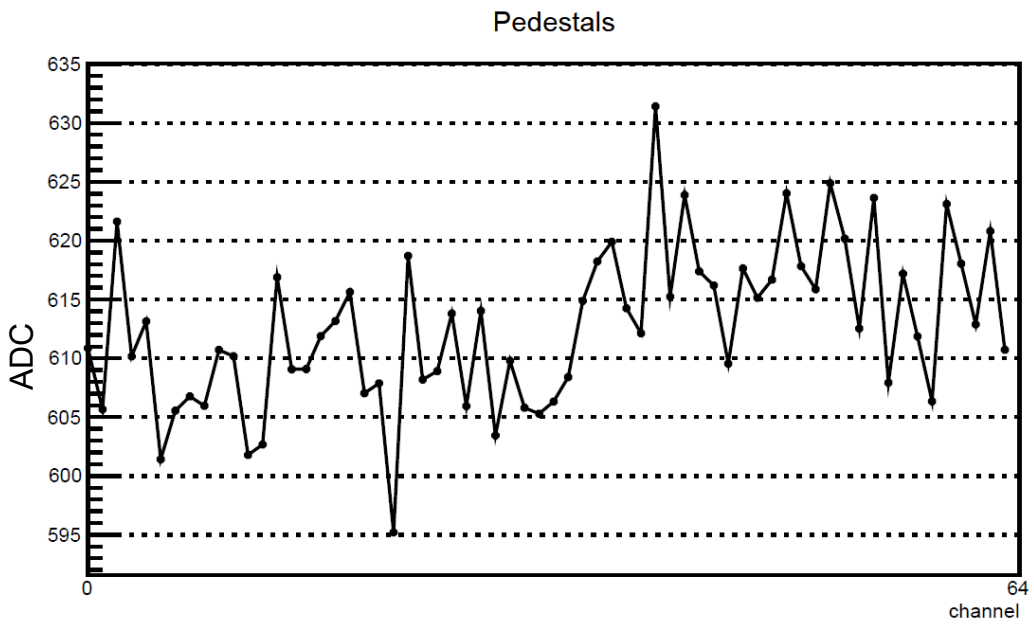
- Used the test board to characterize ASTRA-64

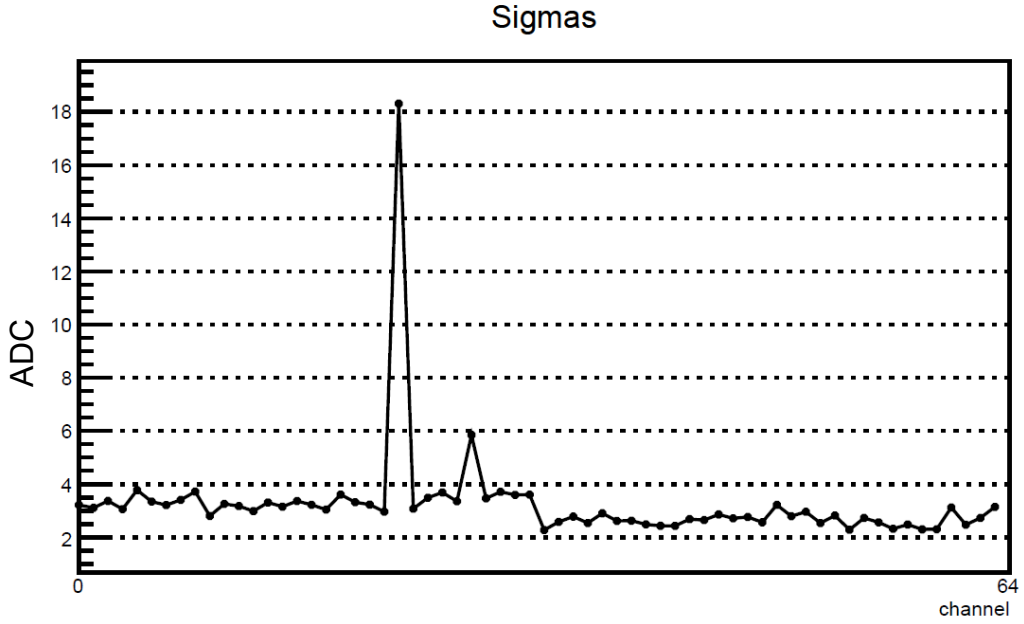
- Verification campaign to test all the functionalities
  - FOOT sensors
    - 3x3 mm^2
    - 50 μm implantation pitch
    - 150 μm readout pitch
  - Integrated test-pulse injection
  - 1058-nm laser





ASTRA Characterization: External ADC Calibration



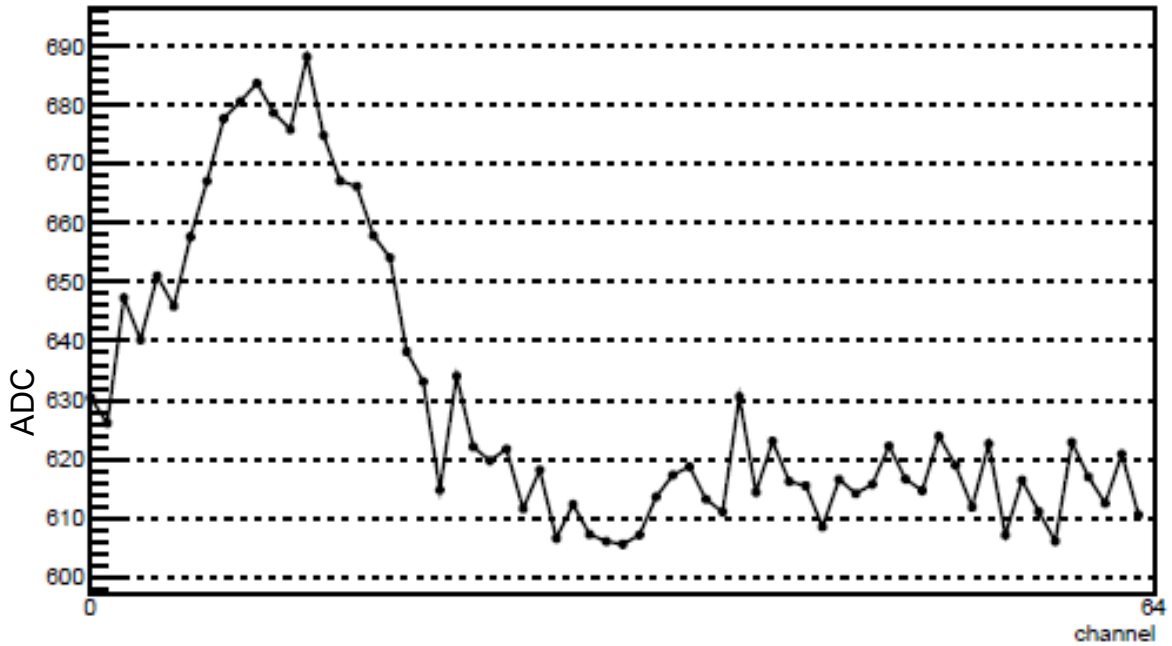


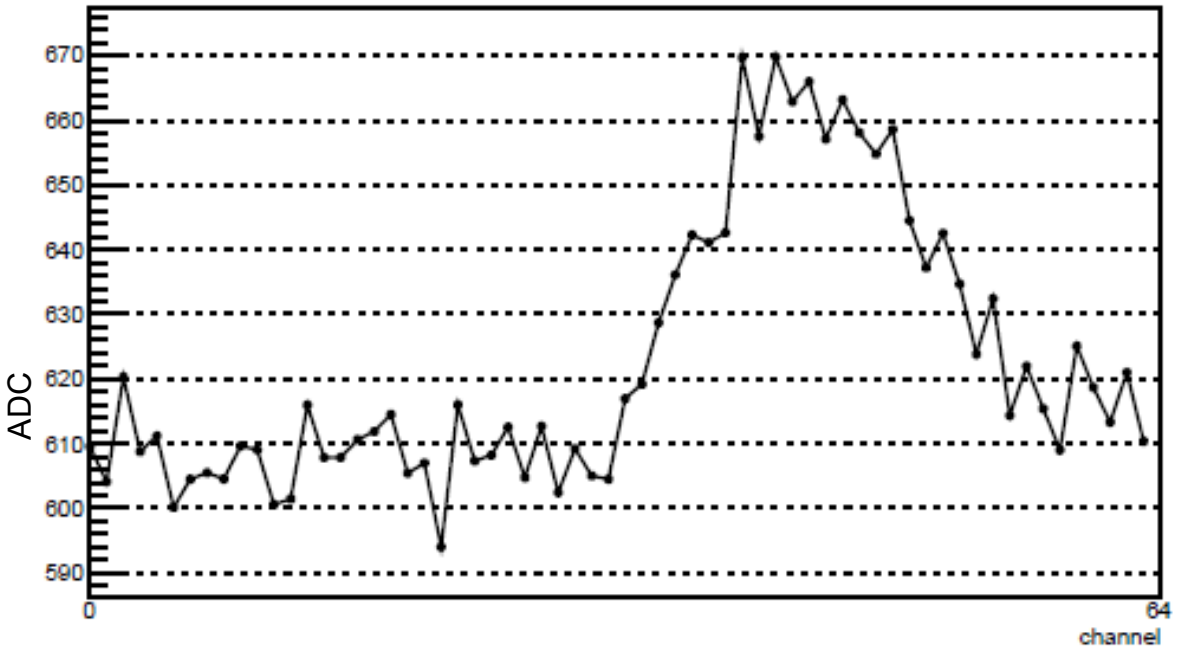
- Tested ASTRA analog output
  - Pedestal: base-line of the strips without crossing particles (average value)

- Same noise figures as in FOOT / POX / HERD hybrid boards

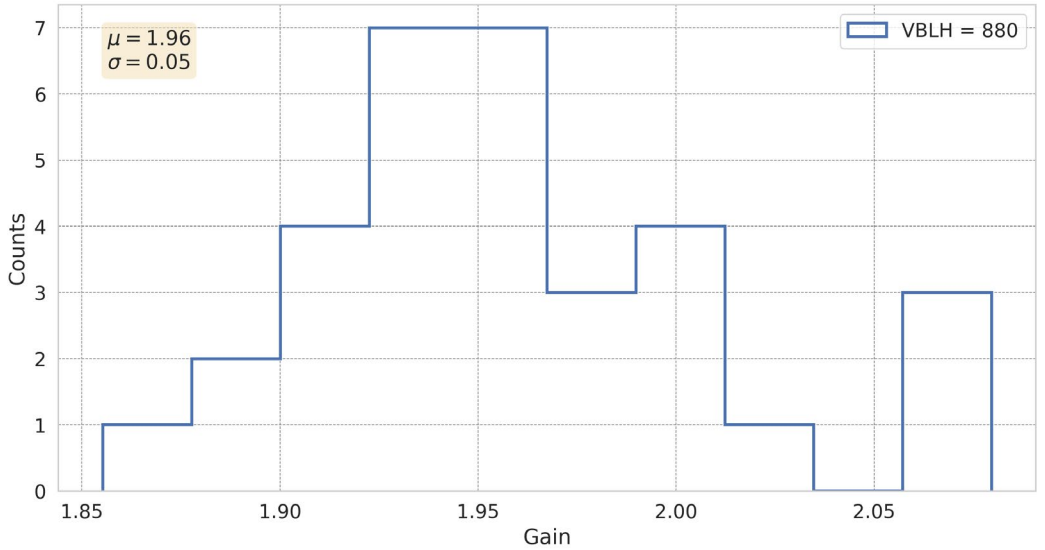
(ADC)

ASTRA Characterization: External ADC Laser





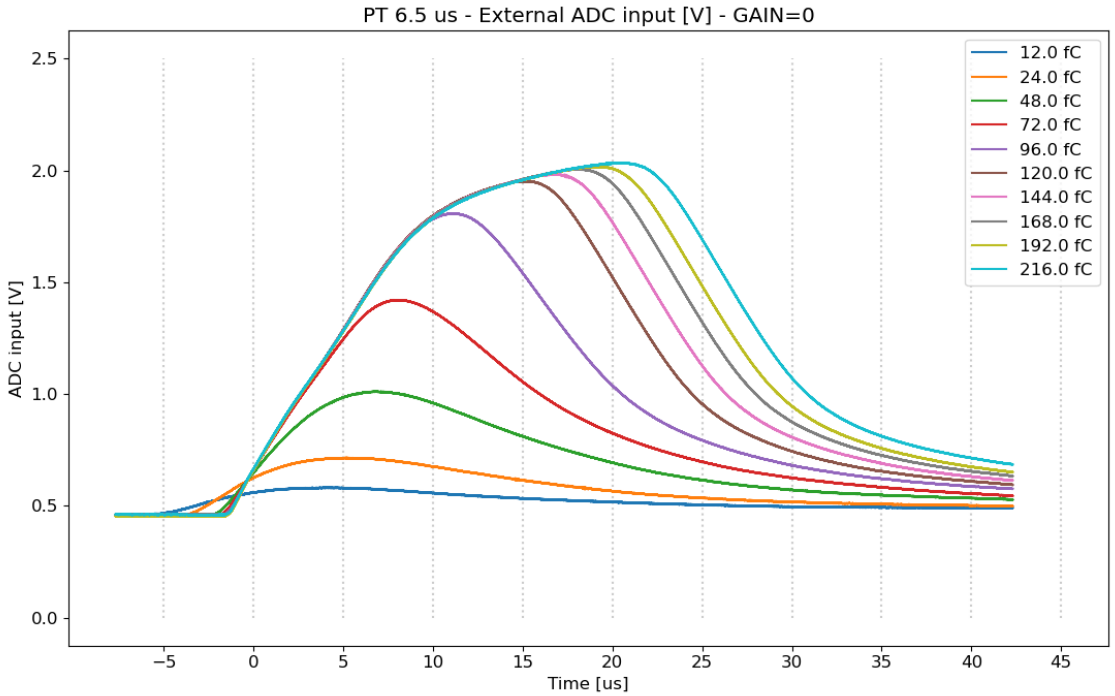
- Illuminated the sensor with 1058-nm laser
- Verified that both ASTRA-64 halves were receptive
  - Laser can only induce big signals onto the detector

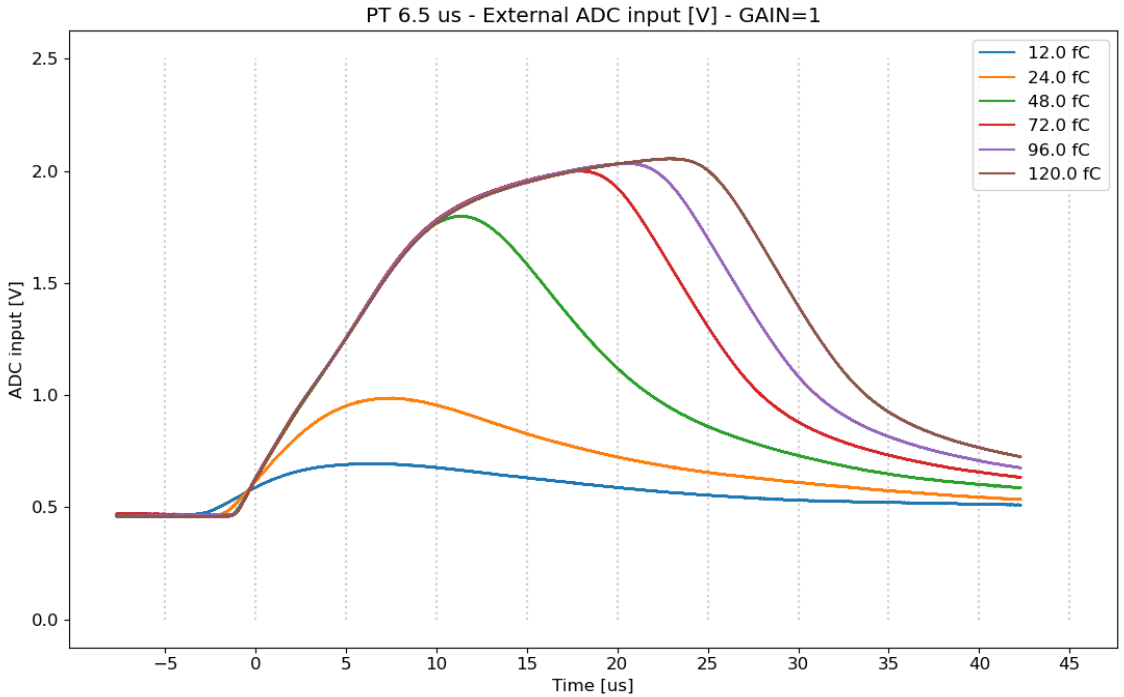


ASTRA Characterization: Front-End Response

- Freeze one channel in output and send integrated test pulses
  - Shaping time 6.5 µs
  - Conversion from V_{tp} to Q_{inj}
    - C_{inj} = 240 fF

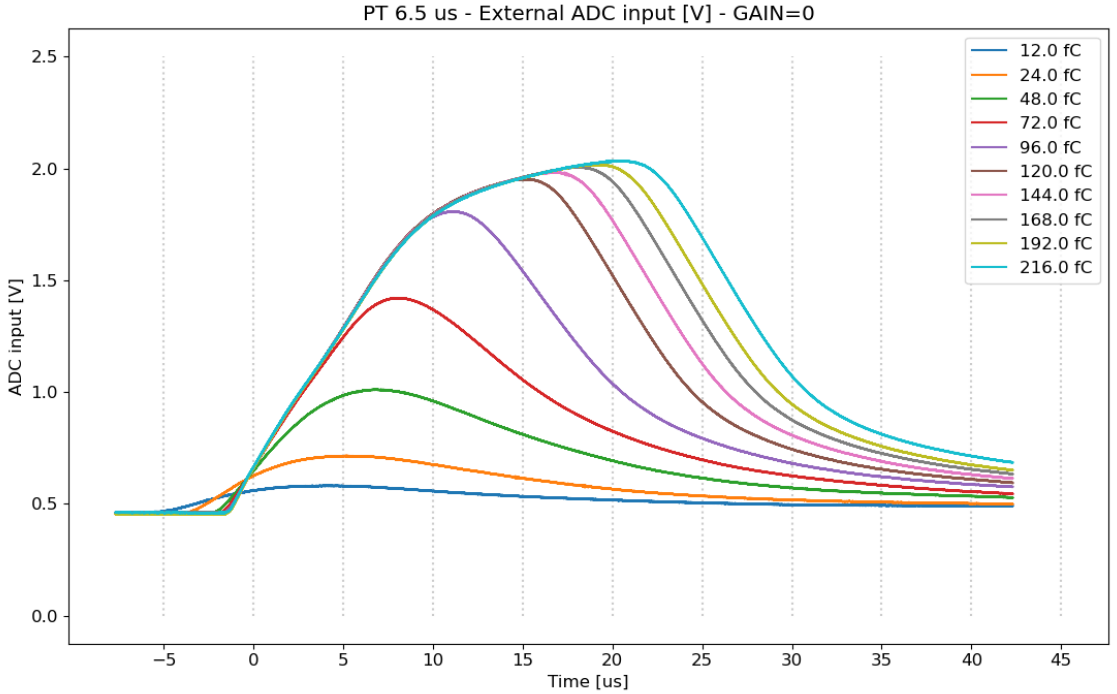
- Measure and validate
  - Pedestals
  - Max/min value
  - Noise
  - Gain
  - …

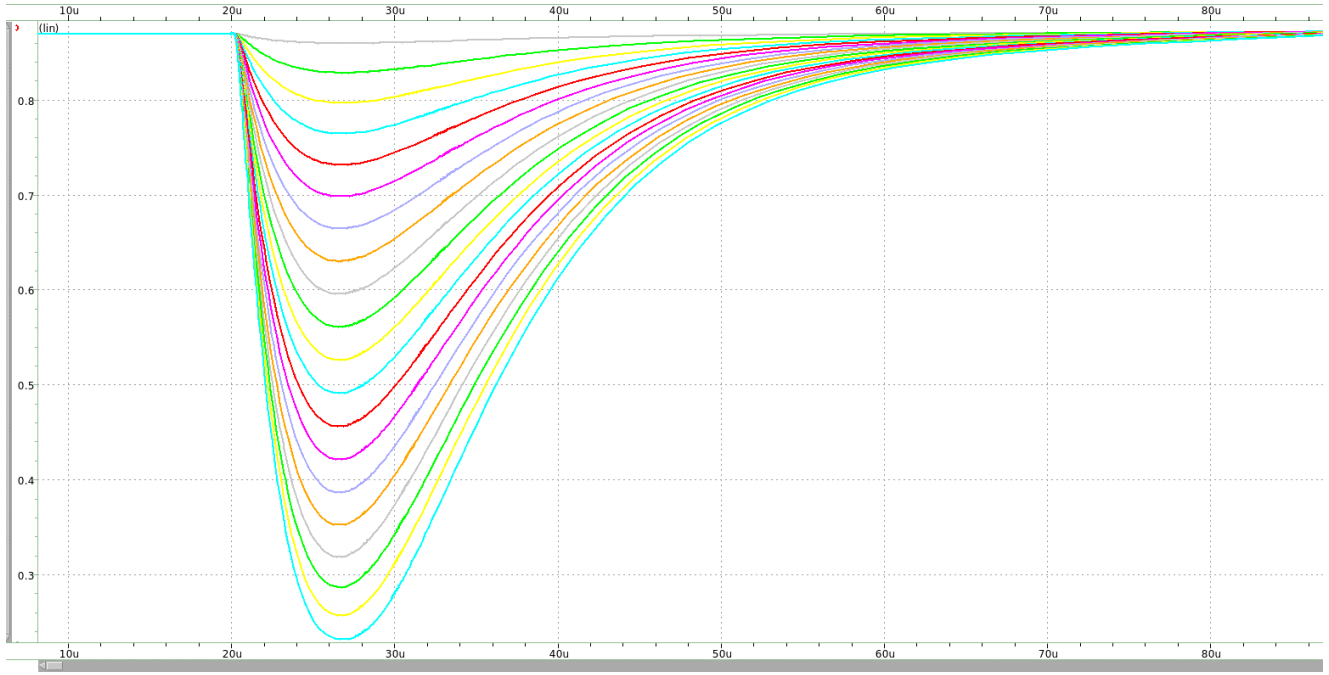




ASTRA Characterization: Test-Pulse Injection

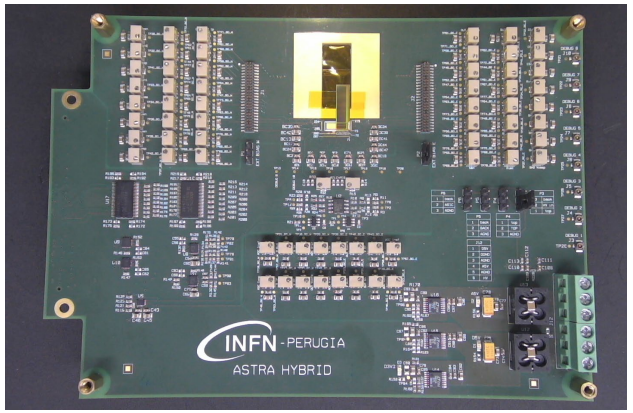
- Full chain shows two main issues regarding the external ADC input:
  - Low gain: it does not cover the ADC dynamic range (0–3.3 V)
  - Saturation occurring at some level
    - Resulting in a double slope of the gain
- To separate the response of the CSA+Shaper from the output buffer
  - Observe the debug output
  - Direct output of the shaper for some of the channels

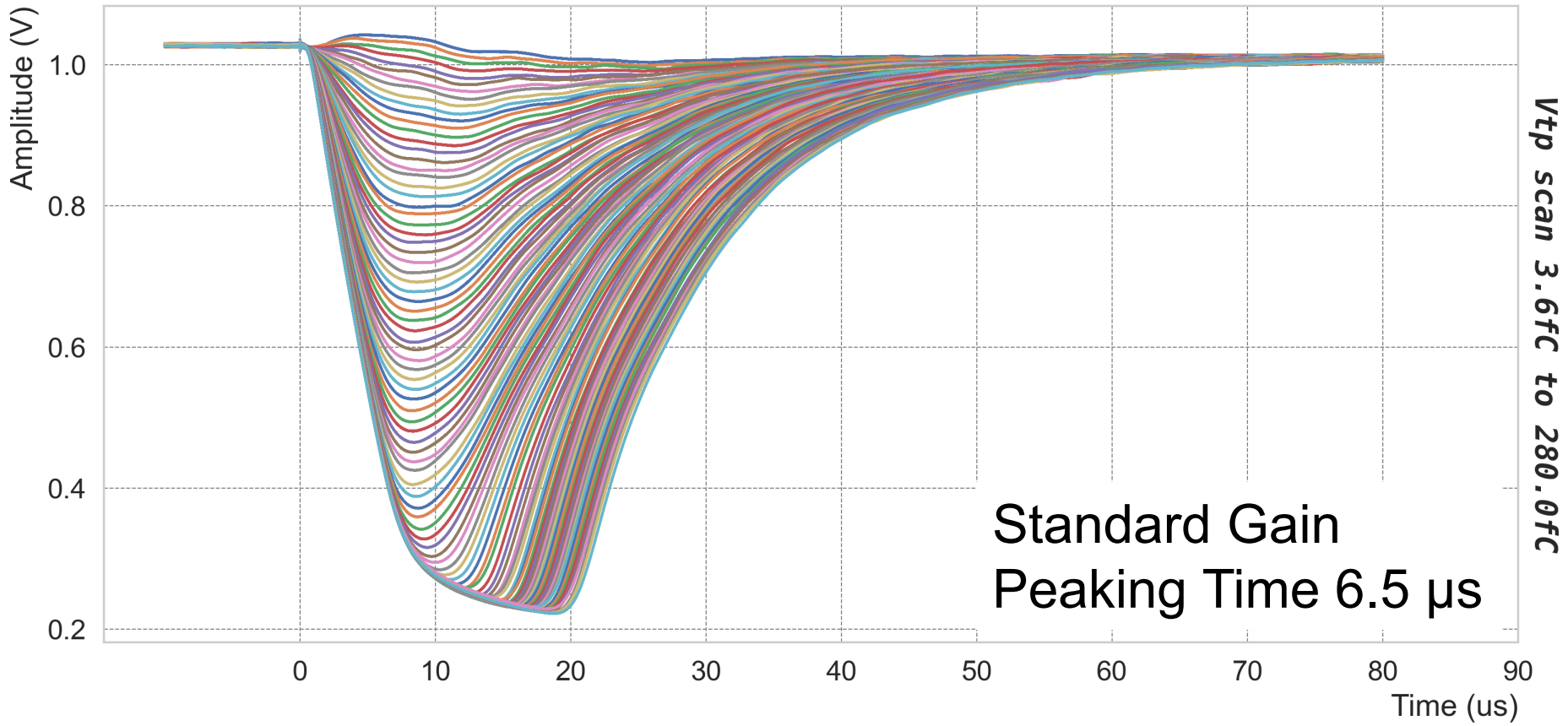




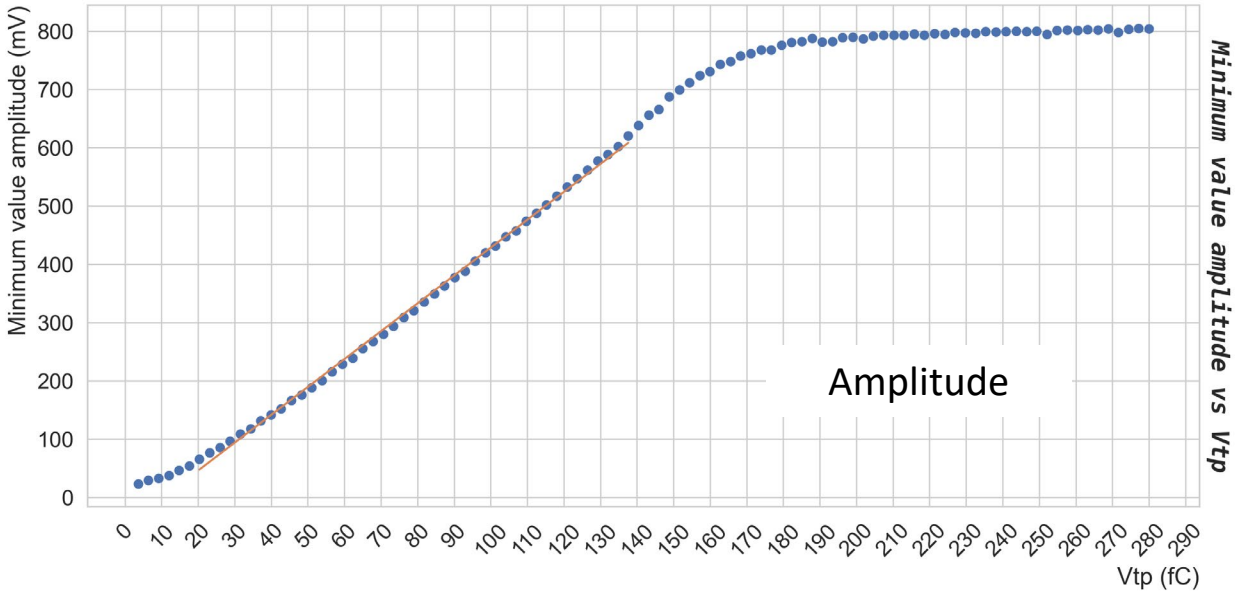
Measures: CSA + Shaper Output

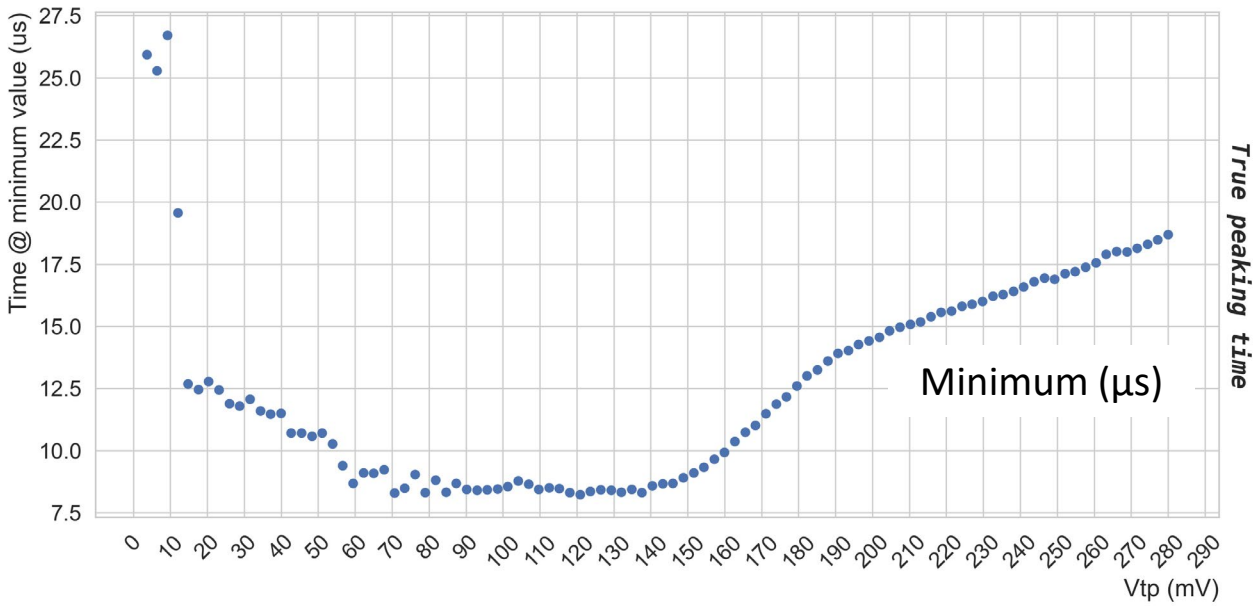
- V_{tp} scan by varying combinations of the parameters
  - Gain: Standard / High
  - Peaking Time: 3.5 µs, 6.5 µs, 9 µs
- V_{BLH} set to the maximum possible value (~1.1 V)
  - Saturation occurring at higher input charges

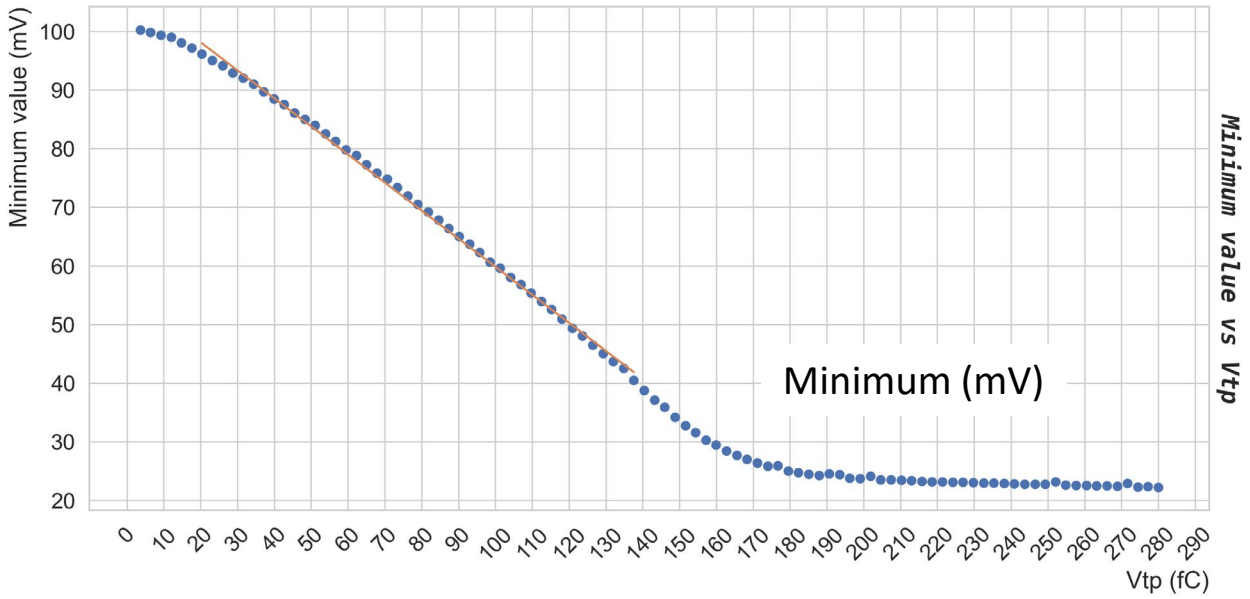




CSA + Shaper Output: Measured Parameters





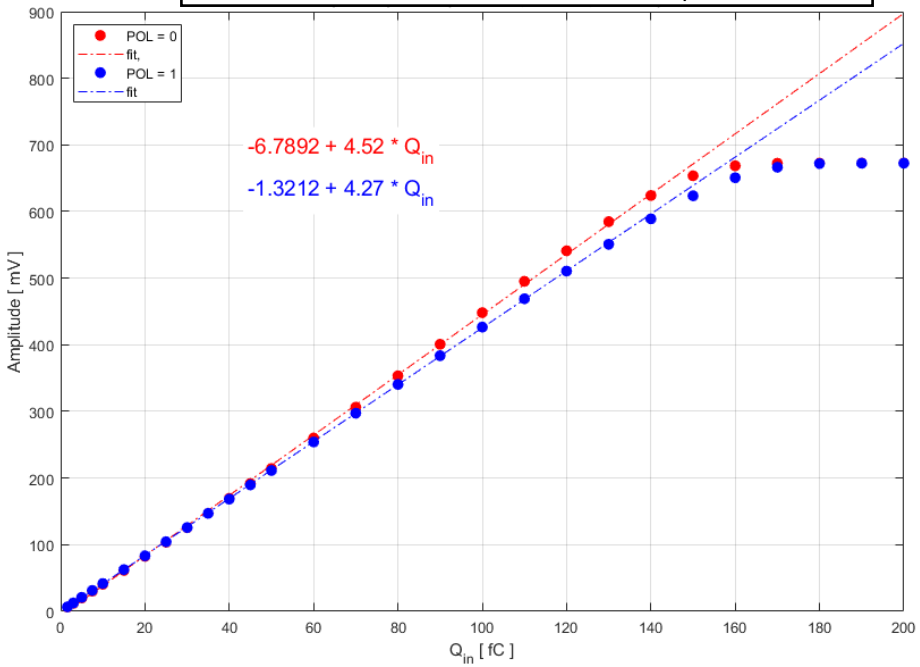


Standard Gain
Peaking time: 6.5 µs
Charge pulses: 3.6-280 fC

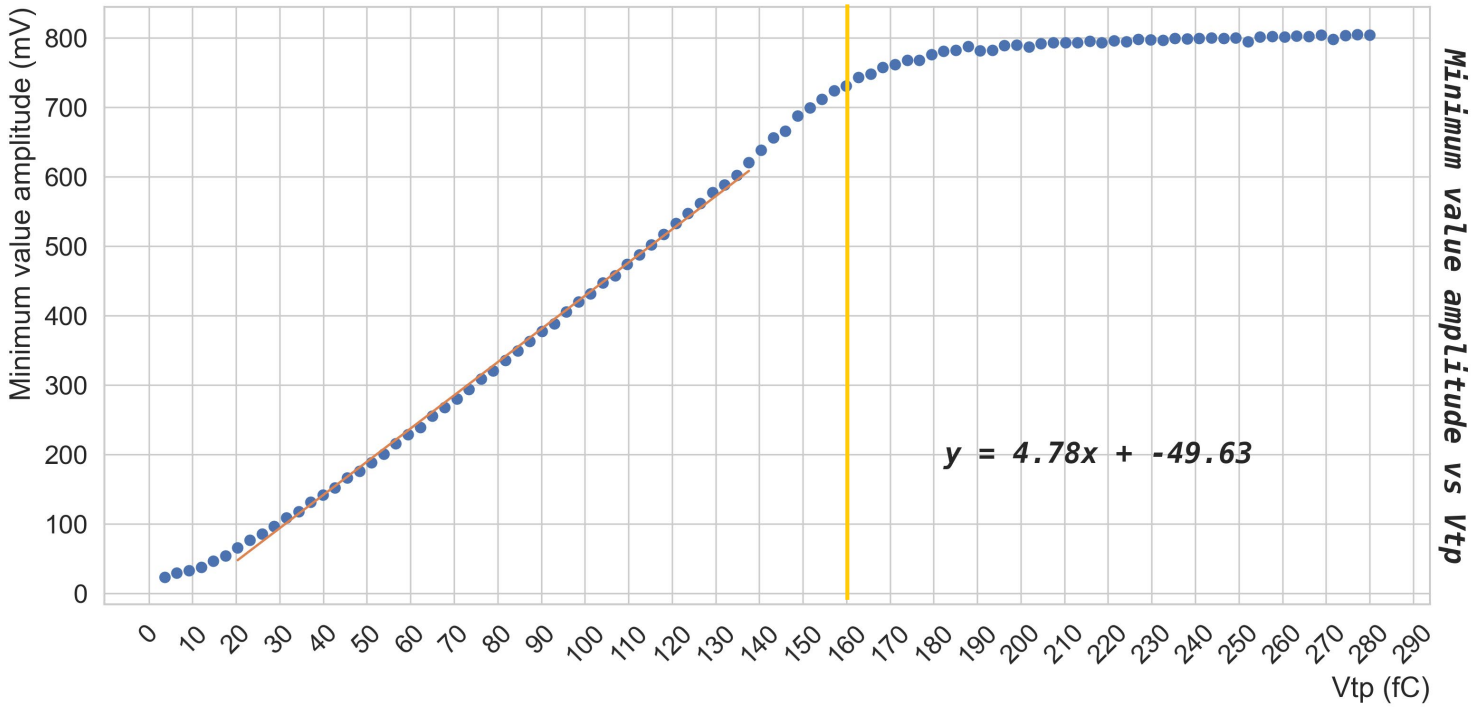
ASTRA Characterization: Front-End Linearity

- Shaping time: 6.5 µs
- Slightly higher gain compared to simulations
  - 4.78 mV/fC VS 4.3 mV/fC
  - 8.72 mV/fC VS 8.1 mV/fC

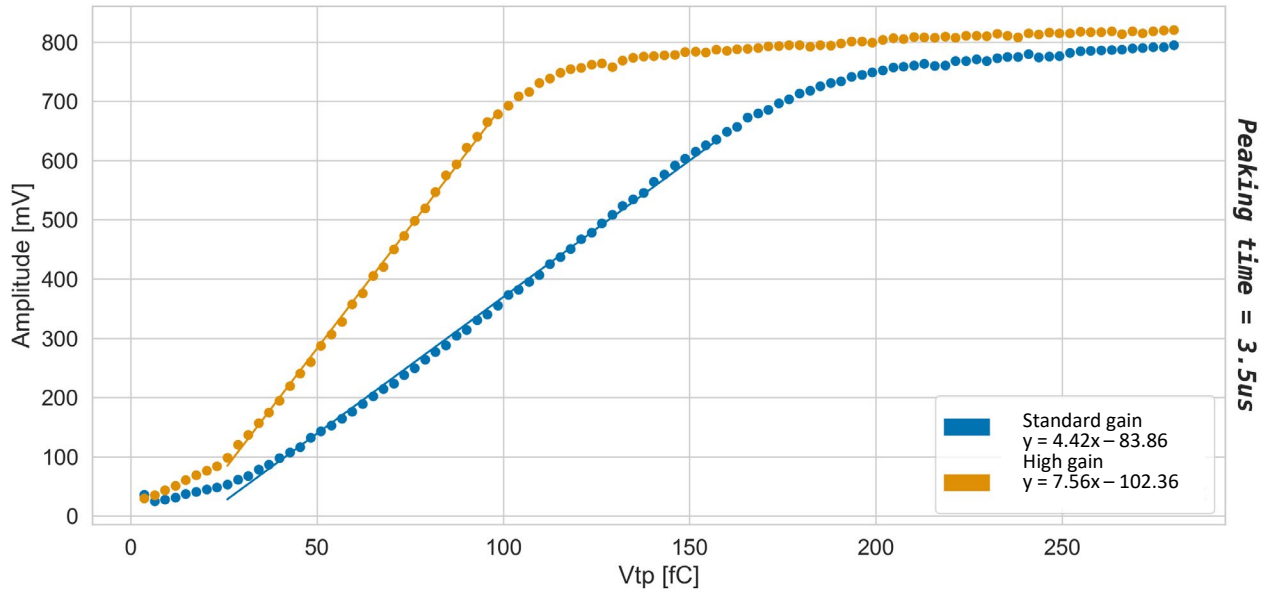
Simulation: Standard gain, T_p = 6.5 µs

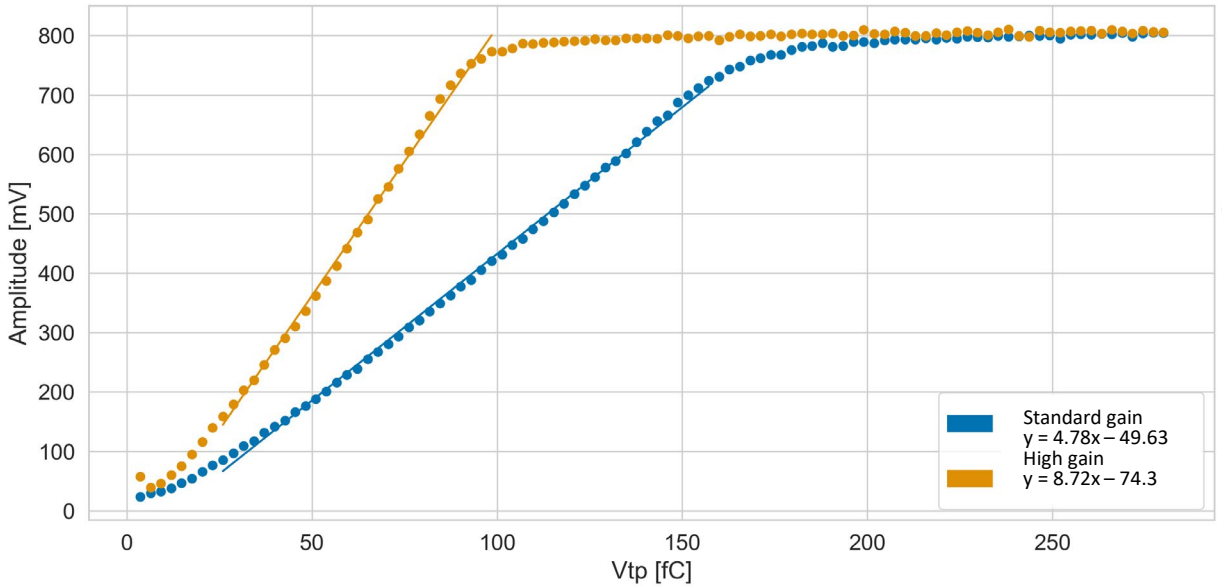


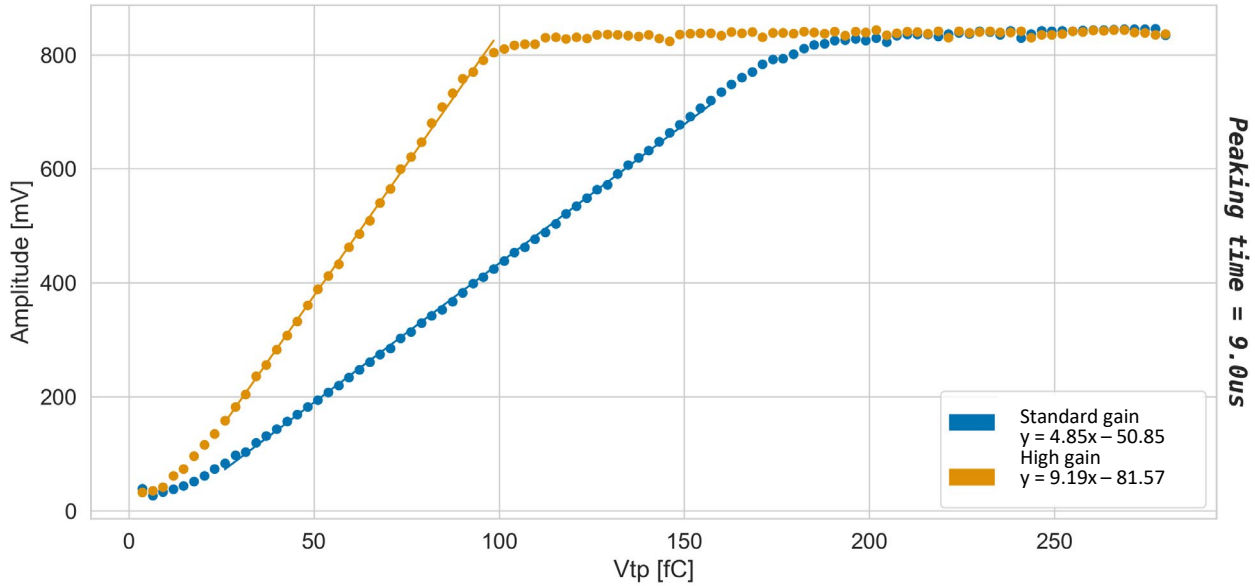
Extends linearity up to 160 fC
(but loses some for low charge)



ASTRA Characterization: Actual Gain







Gain (mV/fC)	V_{tp} 3.5 µs	V_{tp} 6.5 µs	V_{tp} 9 µs
Standard	4.42	4.78	4.85
High	7.56	8.72	9.19

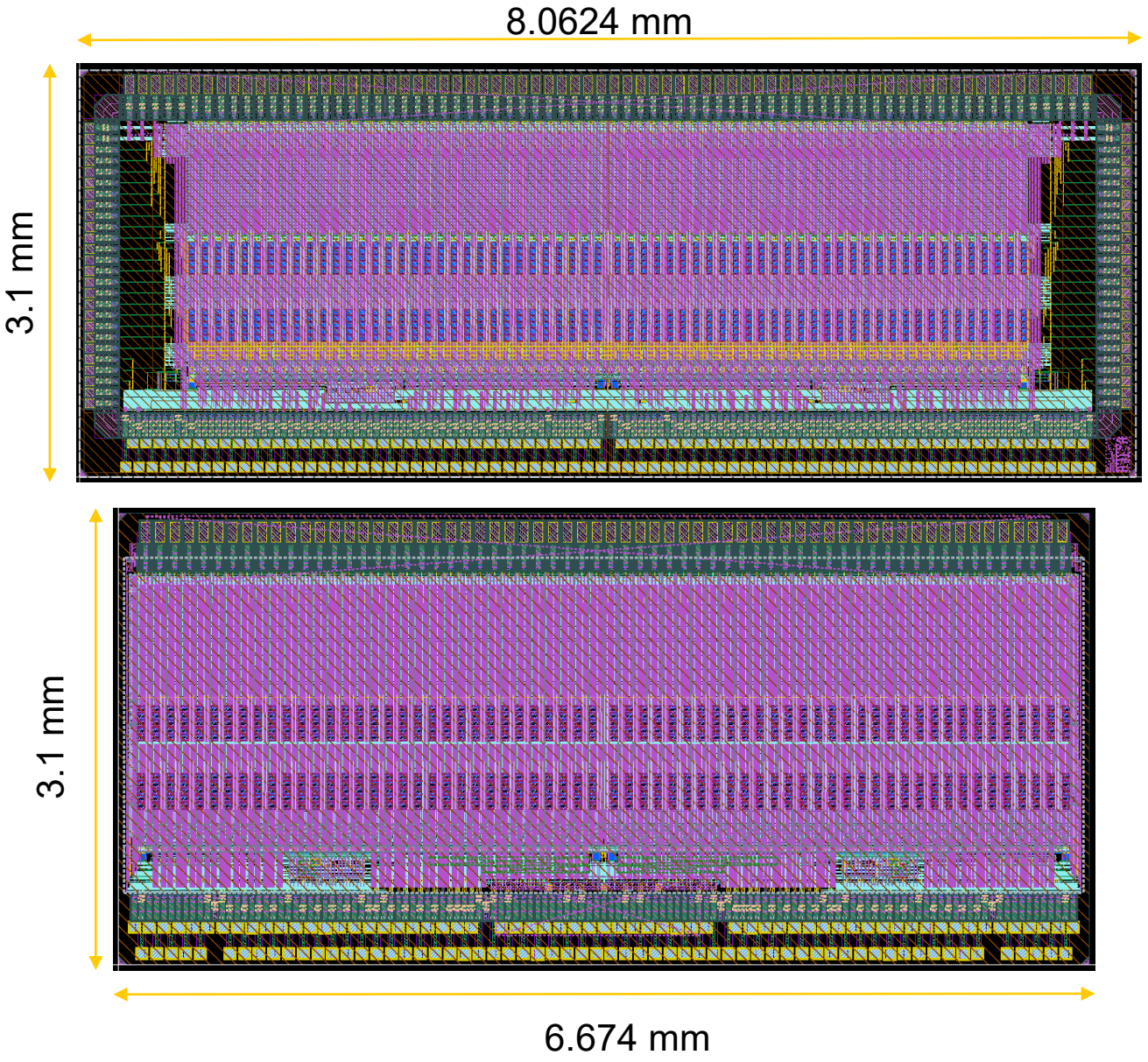
ASTRA Requirements and Specs

	Requirements	Specs (v1)
Channels	64	64
Dynamic Range	± 160 fC; ± 80 fC	160 fC; 90 fC
Linearity Region	± 160 fC; ± 80 fC	160 fC; 90 fC
Shaping Time	Adjustable in 1÷10 μs	1.5 μs, 3.5 μs, 6.5 μs, 9 μs
ENC	< 1000 e^- @ C_{in} 100 pF	< 1000 e^-
Gain	4.3; 8.1 mV/fC [peaking time 6.5 μs]	4.78; 8.72 mV/fC [peaking time 6.5 μs]
Output	Multiplexed pulse height Digitized pulse height Channels FastOR	Multiplexed pulse height, Digitized pulse height, Channels FastOR
Power supply	Positive (only) supply	1.2 V
Overall power consumption	-	Test board: 1.4 W
Channel power consumption	< 1 mW	<1 mW
Production Process	110 nm CMOS	110 nm CMOS
Size	6x6 mm^2	8.06x3.1 mm^2

Stage	Power/ch [μW]
Preamplifier	300
Inverting stage*	24
Shaper	66
Fast Shaper	32
Discriminator	18
S&H	108
ADC	36
Single-to-Diff. Amp.	8
Output Buffers (2)	37
Counter + Serializer	0.12
SLVS RX (3)	9
SLVS TX (2)***	190

630 μW/channel for analog readout
830 μW/channel for digital readout

ASTRA-64 v1 vs v2



- Removed side pads to be 2-side abuttable
- Already available from ARCADIA RUN2
- Design of PCB hosting ~4 ASTRA-64 v2 ASICs starting soon

Conclusions

- ASTRA: 64-channel ASIC readout electronics for Si μStrips
  - In-house design of versatile chip
  - Possible application in different space and ground experiments

- Each ASTRA channel performs signal amplification and charge measurement
  - Positive and negative input signal polarities readout capability
  - 2 gain settings providing input dynamic range up to 80 or 160 fC
  - 4 peaking time configurations: 1.5 μs, 3.5 μs, 6.5 μs, 9 μs
  - Dual-readout mode: analog and digital
  - FastOR trigger output

- ASTRA characterization still in progress
  - Exploit all the functionalities
  - Use it in actual beam tests