A position sensitive silicon sensor with sub-micron resolution with entirely digital operation

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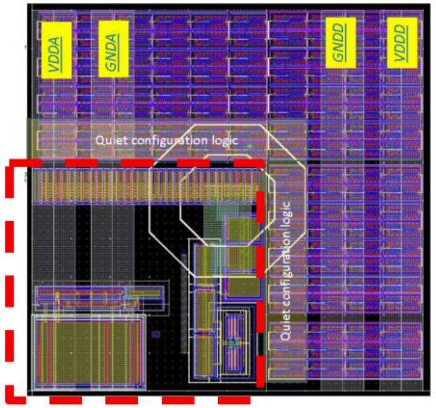
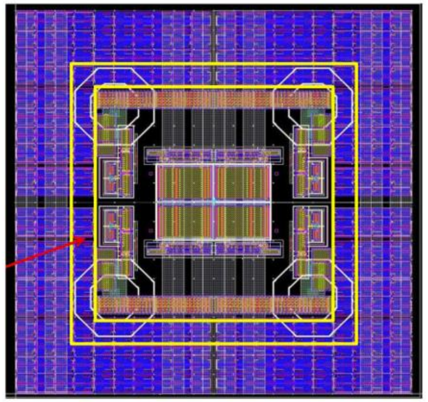
OUTLINE:

- Motivation for developing an entirely digital radiation sensor
- Operation principle and design
- First experimental results
- Outlook

State of the art devices: hybrid pixel ASICs

V. Re, 13th Pisa Meeting on Advanced Detectors



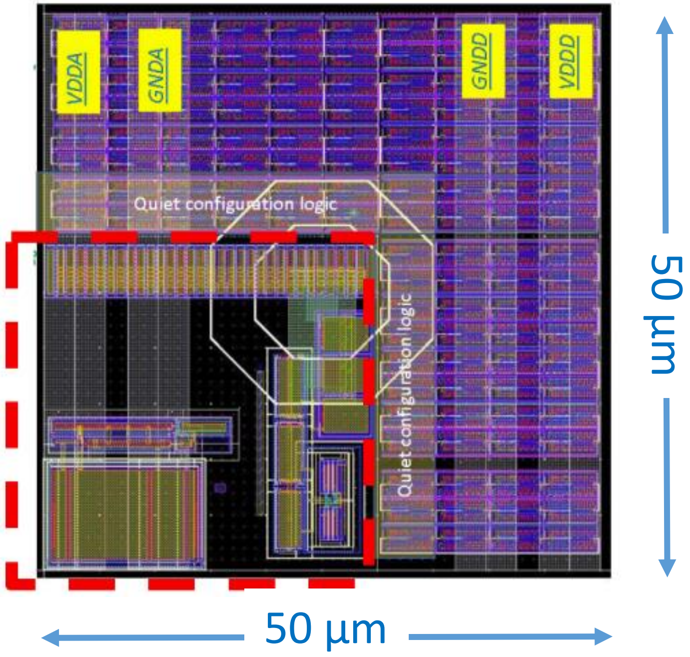


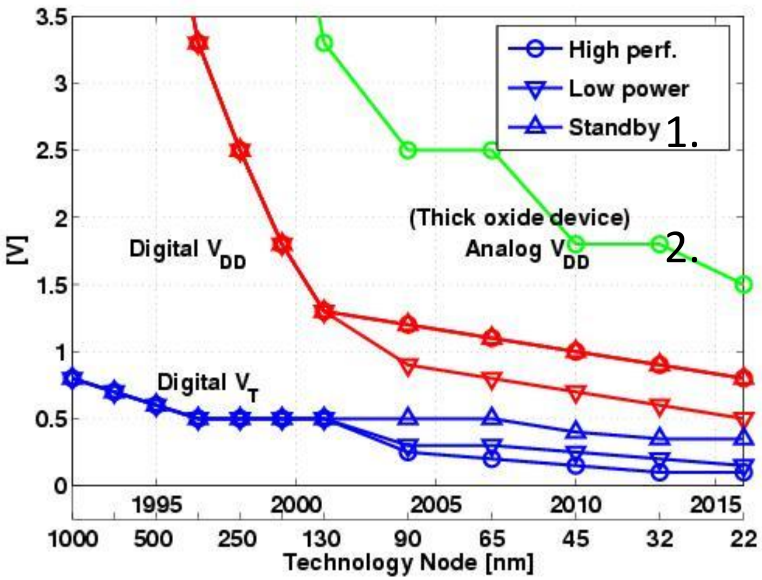
RD53 **65 nm CMOS** pixel readout chip for extreme data rates and radiation levels (V. Re et al., CERN/RD53 collaboration)

Advanced readout chip for the pixel layers of ATLAS and CMS Upgrades at CERN.

Analogue area

Expected position resolution > 15 µm.





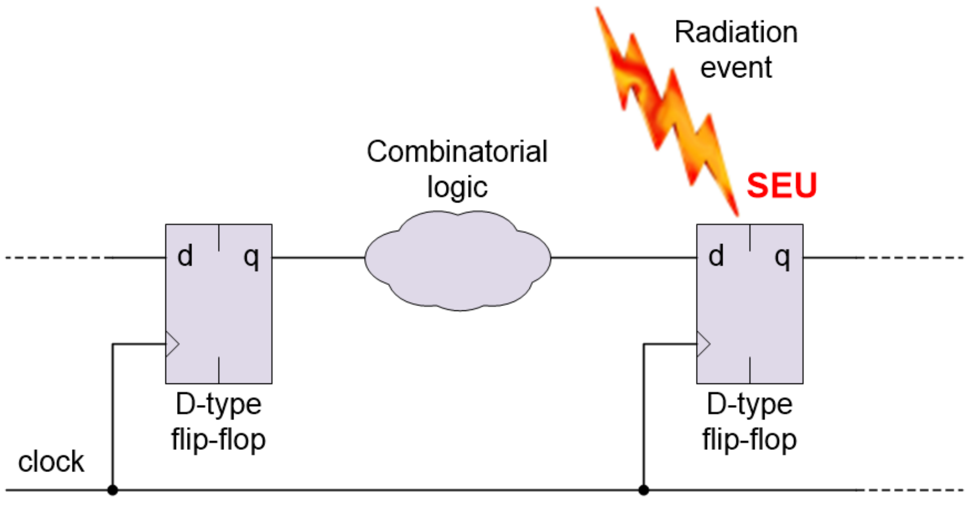
Need of higher voltage range (thick oxide transistor) (SNR)

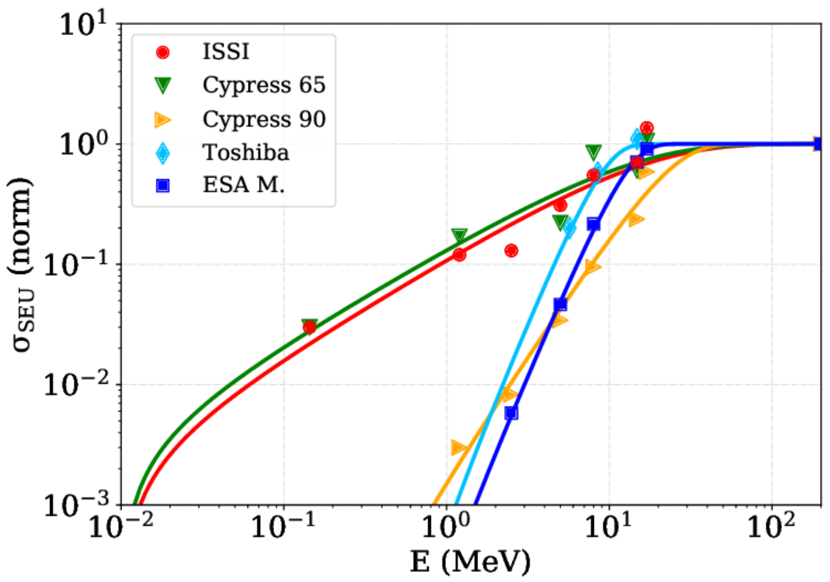
Need to reduce noise and mismatch (large transistors)

Order of magnitude more transistors per area in the digital section compared to analogue area. The latter cannot be significantly reduced!

Today's pixel size cannot be reduced much further, even with smaller feature size

PartiCam project
Single Event Upset (SEU) in memories

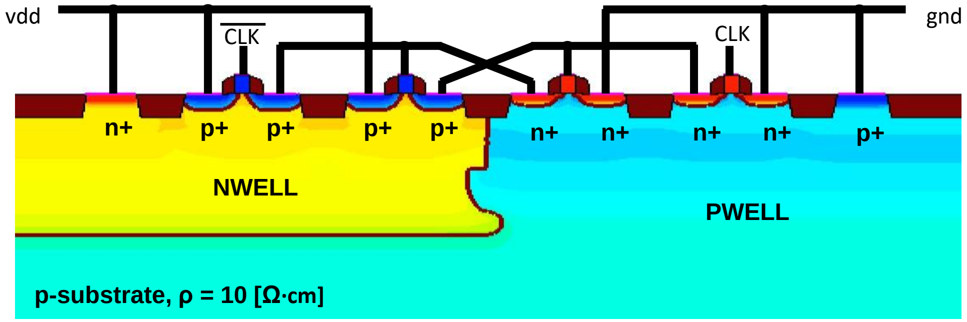


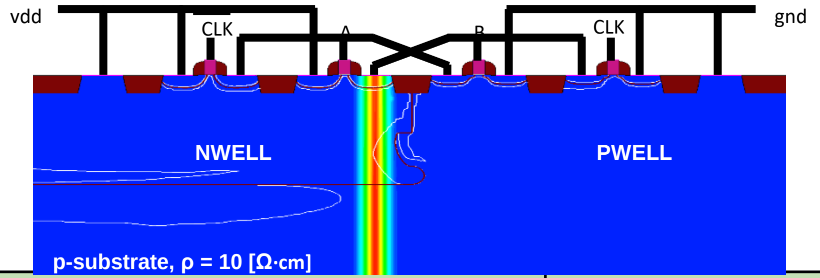


Presence of particles may induce a flip of the memory content
Exists a minimum charge (Q_T) that forces the change in memory state
Define a cross section: $N_{SEU}/N_{particles}$ per cm^2 = probability to flip
→ IDEA: define an array of memories sensitive to particles

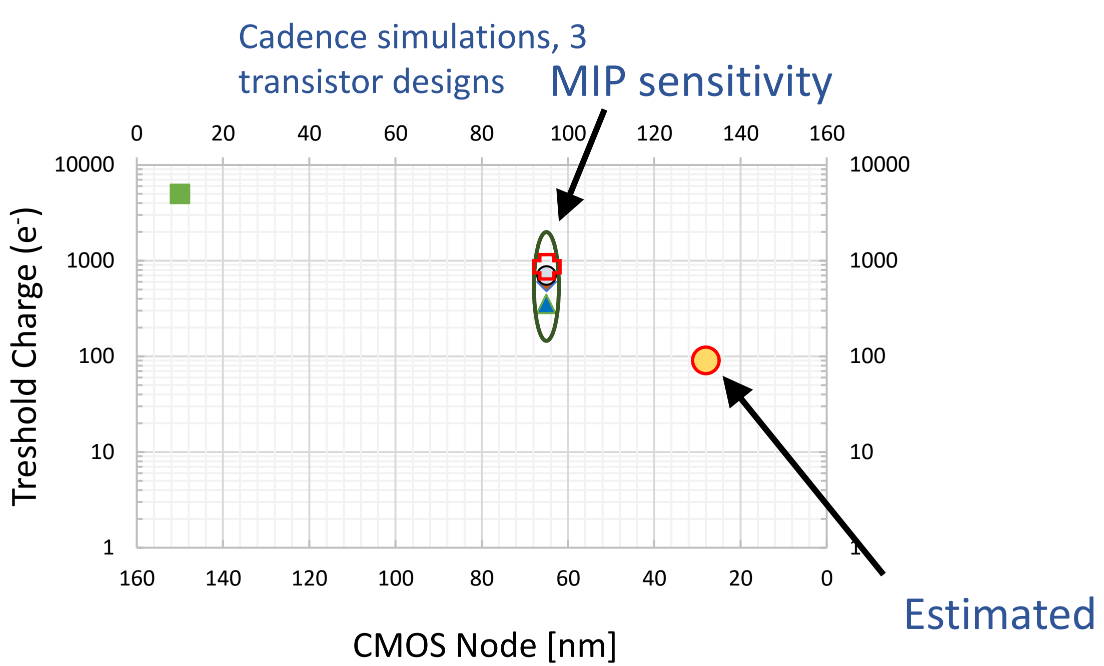
Feasibility Studies

Dependence of Threshold Charge (C_T) on reference voltage and CMOS feature size. TCAD and Cadence simulations (factory design kit). Agreement is found with the two methods.





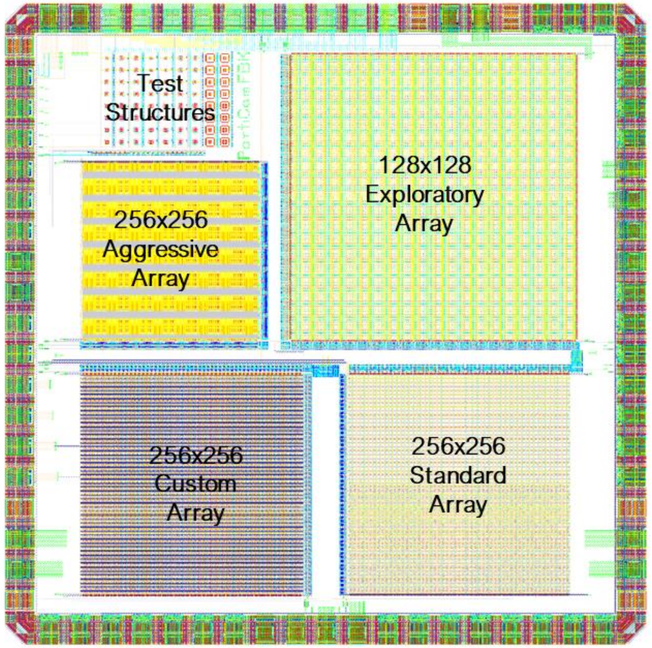
Minimum ionising particles (MIPs)	*80 – 800 e⁻*
X-rays	*500 – 5000 e⁻*
Fast alphas (1 MeV)	*3000 – 300000 e⁻*
Stopping ions	*5000 – 100000 e⁻*
Recoiling nuclei	*5000 - 20000 e⁻*

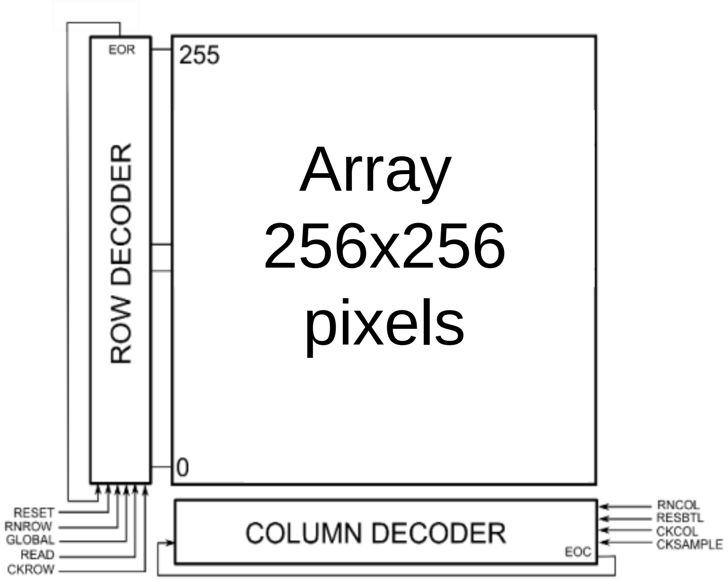


The required sensitivity to alphas, ions, recoils is reached in a 150nm process already, 65nm CMOS yields sensitivity to MIPs! Further scope for improving sensitivity:

- *optimised design of the sensitive nodes*
- *pre-charging the circuit sensitive node*
- *smaller feature size technology*

The PartiCam prototype





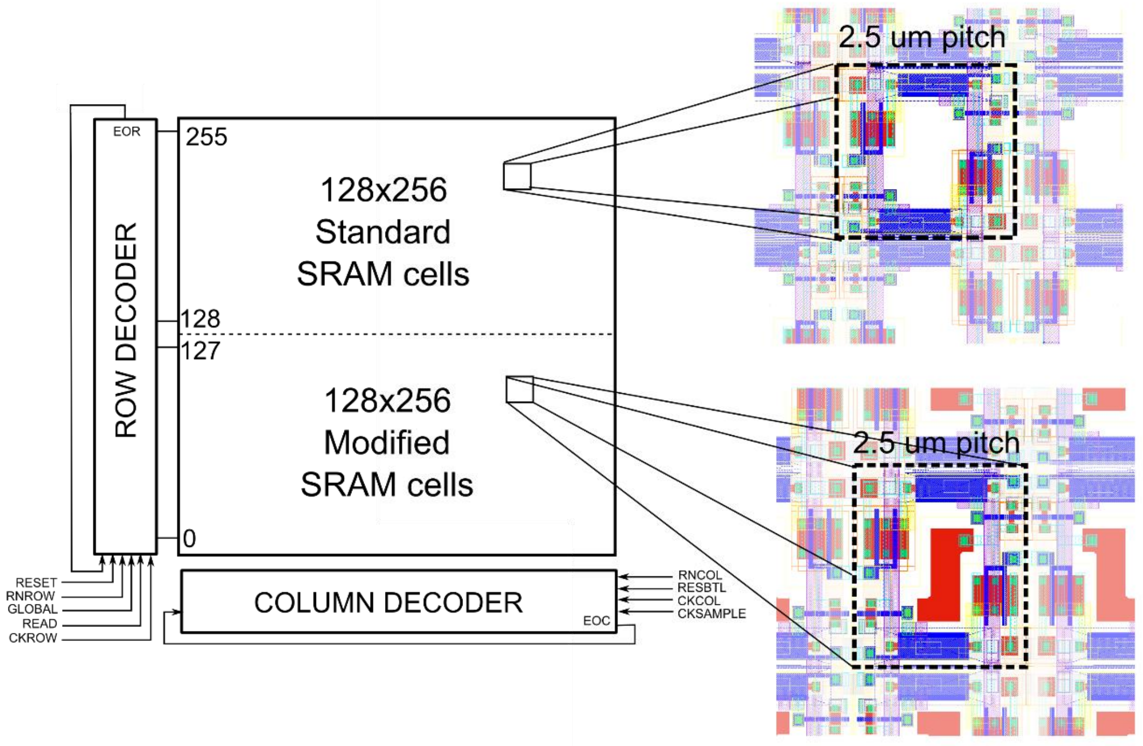
Realized in UMC 65nm low leakage technology, the chip contains four arrays:

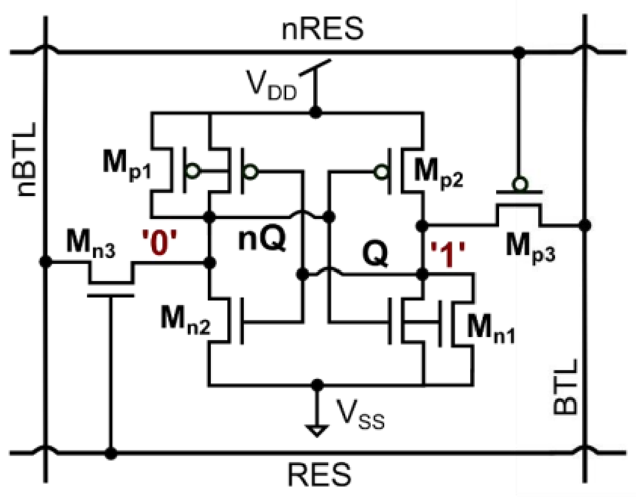
1. Standard array: 256x256 pixels consisting of standard SRAM with 2.5μm pitch
2. Custom array: 256x256 pixels consisting of a novel with 2.5μm pitch
3. Aggressive array: 256x256 pixels consisting of a novel circuit with 2 μm pitch
4. Exploratory array: 128x128 pixels based on different deeper junctions with 6.5 μm pitch

The chip can work in global or rolling shutter mode
Row and Column registers able to select each element of the array (for reading or reset specific row)

NOTE: because of internal bug, not all row and column Decoders of different arrays work properly (need to check One by one)

The reference memory circuit



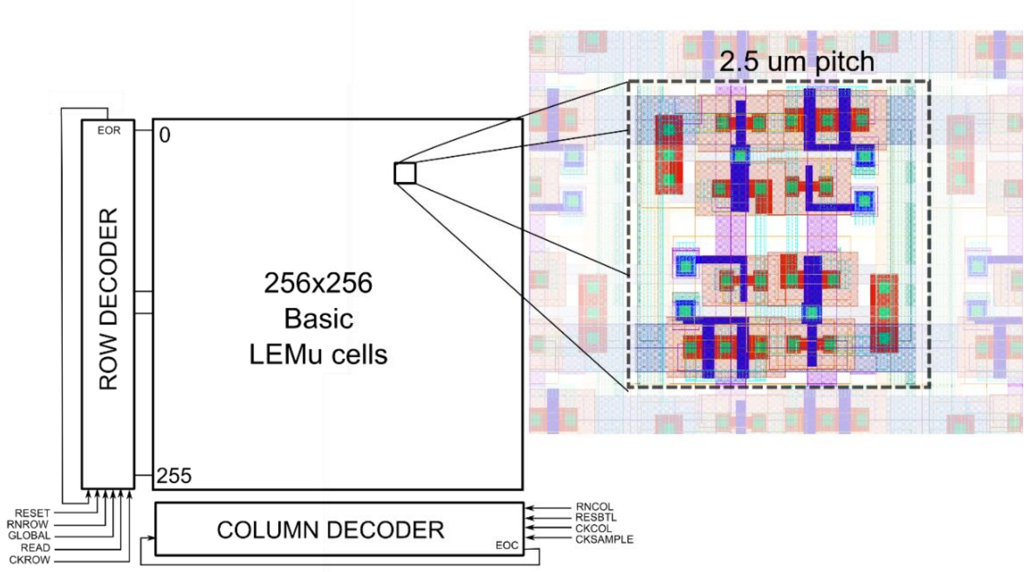


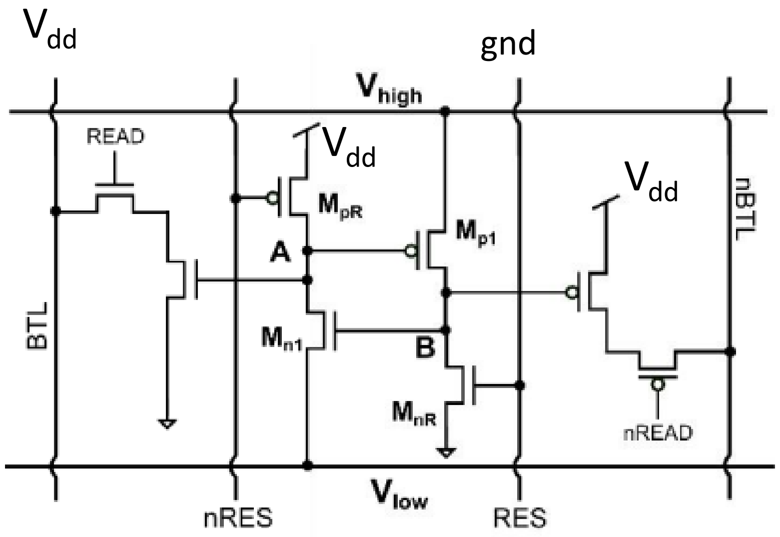
The pixel consists of a custom un-balanced SRAM:

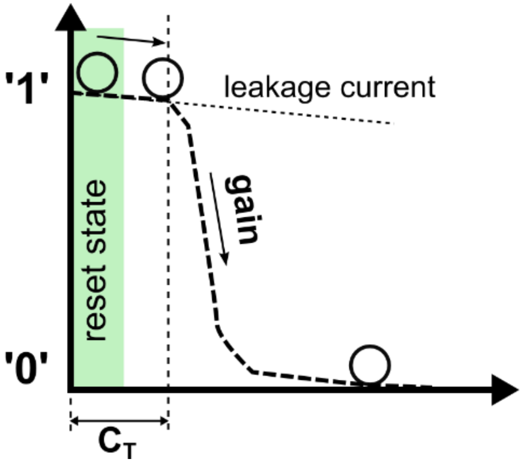
1. The memory is pre-set to a specific state (reset phase)
2. Presence of particle should change the state → Q_T is reduced by proper sizing the transistor memory

Two different layouts of the pixel have been implemented, including a junction extension to verify possible enhancing in the charge collection

The novel custom digital circuit

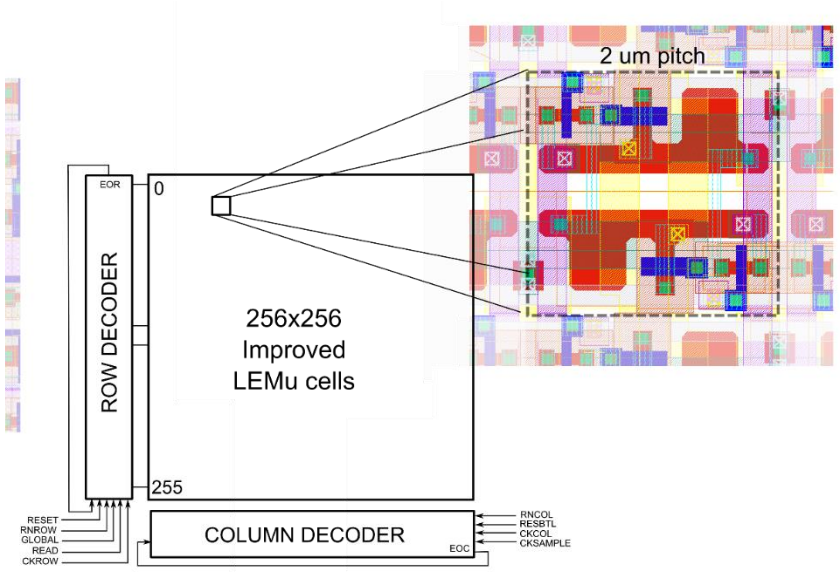


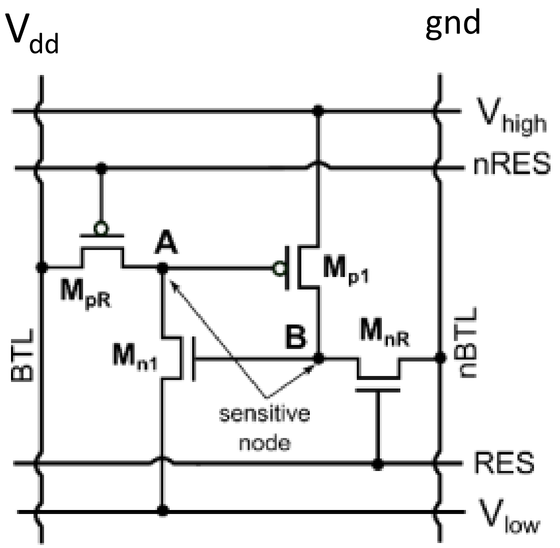


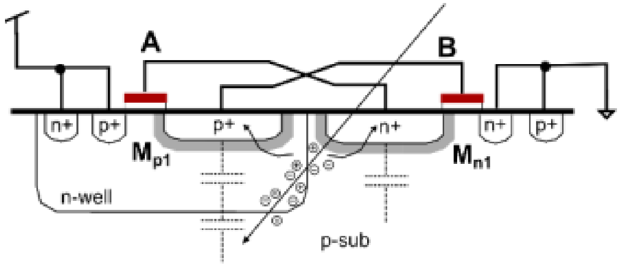


The custom cell now uses two transistors Mn1 and Mp1 as sensitive nodes:
During reset phase nodes A and B are pre-charged to V_{dd} and gnd respectively then left floating (initial state)
Presence of particle should move floating nodes, while a positive feedback guarantee to flip in the other state.
The cell is then readout a gain stage
ISSUE: Leakage current on nodes A and B can change the memory state even if there is no particle (false event)
→ To prevent this effect source of transistors Mn1 and Mp1 are connected to a V_{low} (>0) and V_{high} ($<V_{dd}$) value. Refresh is used to prevent unprovoked switching. $\Delta V = V_{dd} - V_{high} = V_{low}$ - gnd

“Aggressive” layout

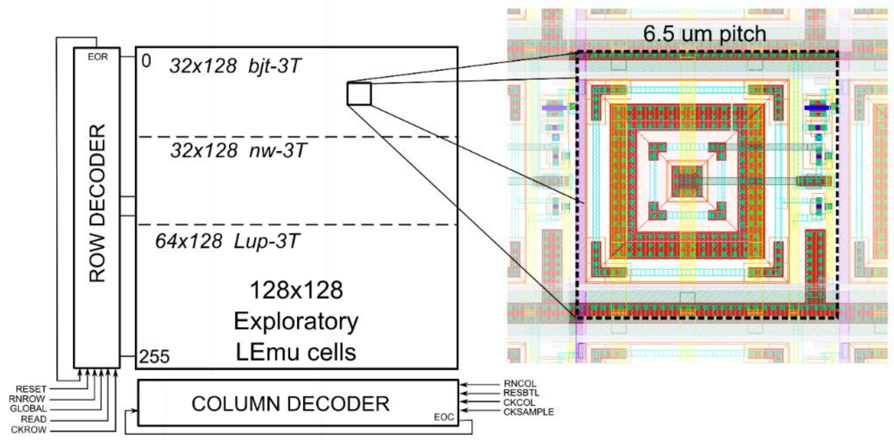


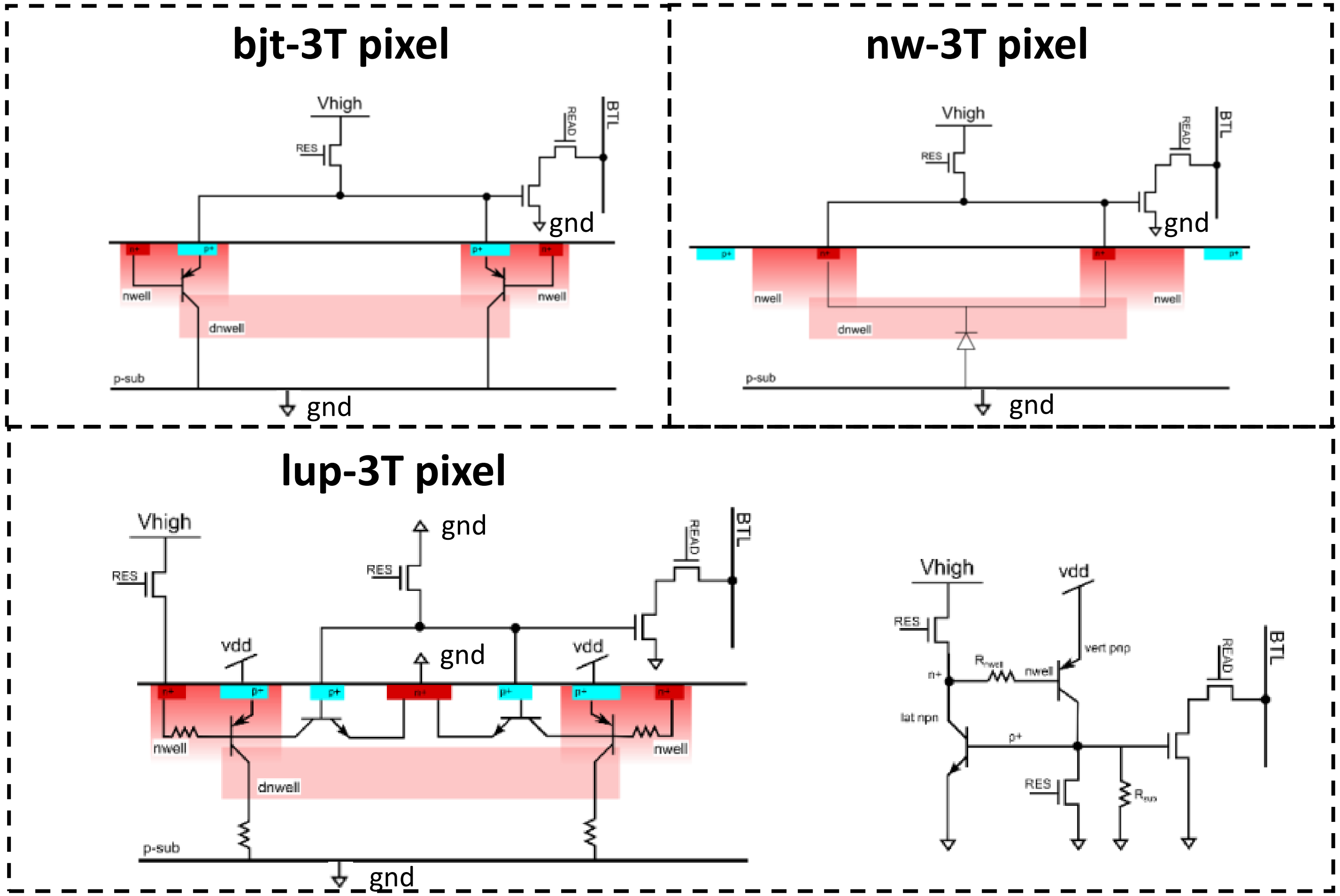




The aggressive design has only four transistors: Mn1 and Mp1 (memory block) and MnR and MpR (for reset and read)
During reset phase nodes A and B are pre-charged to V_{dd} and gnd respectively through the bitline then left floating
Presence of particle should move floating nodes, while a positive feedback flips to the other state
The cell value is then readout by a column level sense circuit.
ISSUE: Leakage current on nodes A and B can change the memory state even if there is no particle (false event)
→ Refresh is used to prevent unprovoked switching.

“Exploratory” layout





Definition of three different pixels:

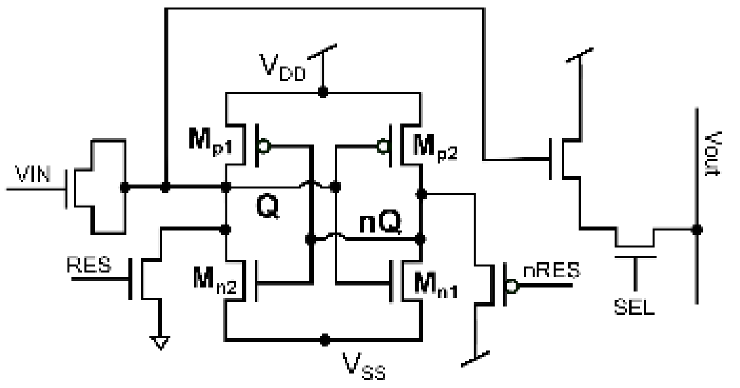
1. photo-transistor (3T pixel structure);
2. nwell junction (3T pixel structure);
3. “latch-up” (weak positive feedback) pixel (3T pixel structure);

Experimental results

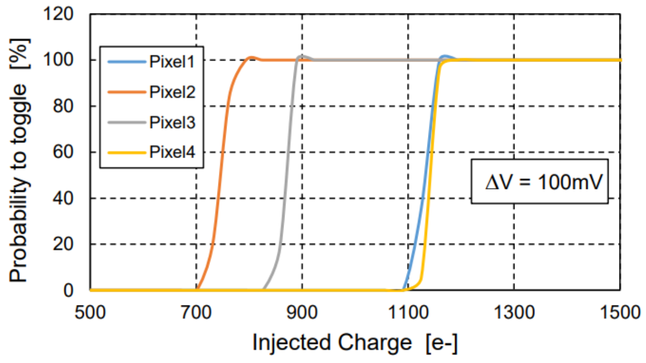
….. in terms of

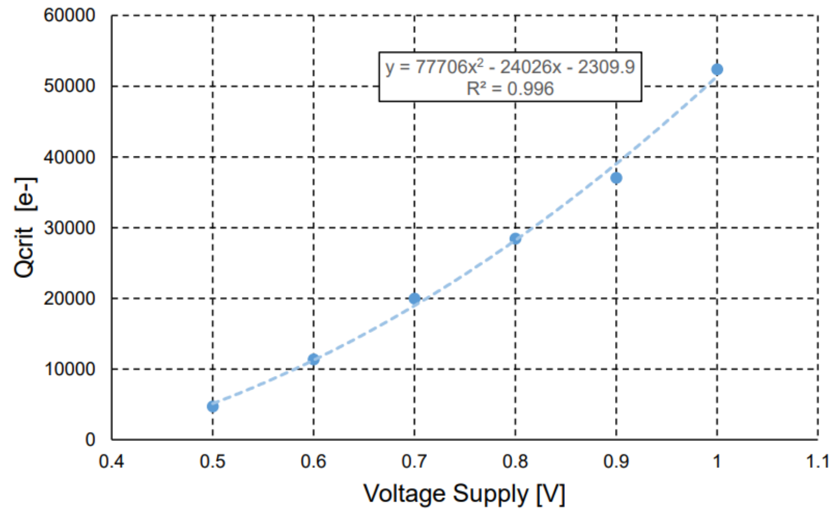
- analysis of test structures (charge injection for testing the charge needed for toggling the circuit – C_T)
- response to laser pulses (410nm)
- response to alpha particles

Experimental results: standard Array



Test structures



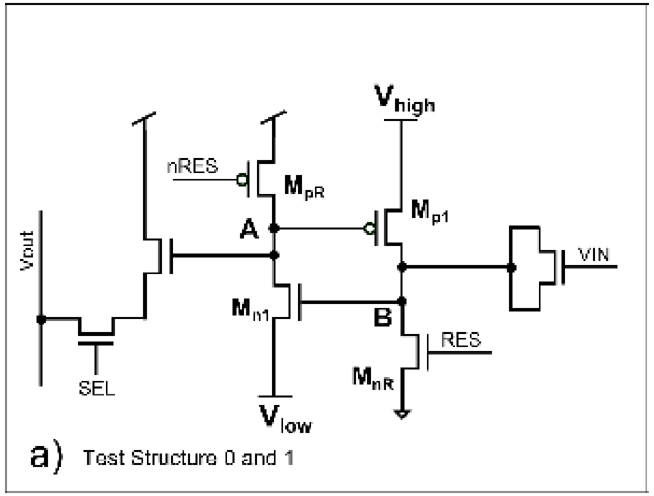


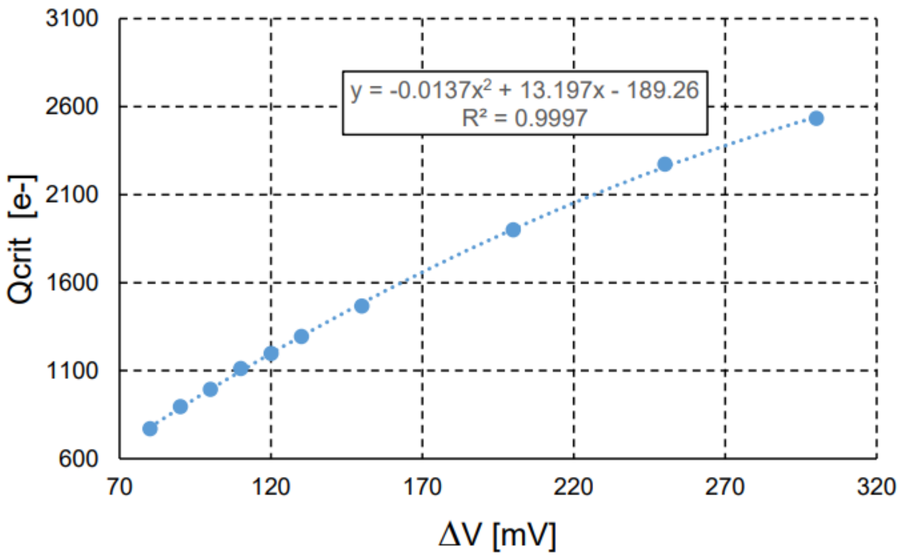
Test structure allows us to have an estimation of the minimum charge needed for changing the memory state

As expected Q_T reduces as the pixel voltage supply reduces, Q_T ~5 ke$^-$ working @ 0.5V → impact on the redout system

Not sensitive to α-particle. Not tested with laser.

Experimental results: custom array

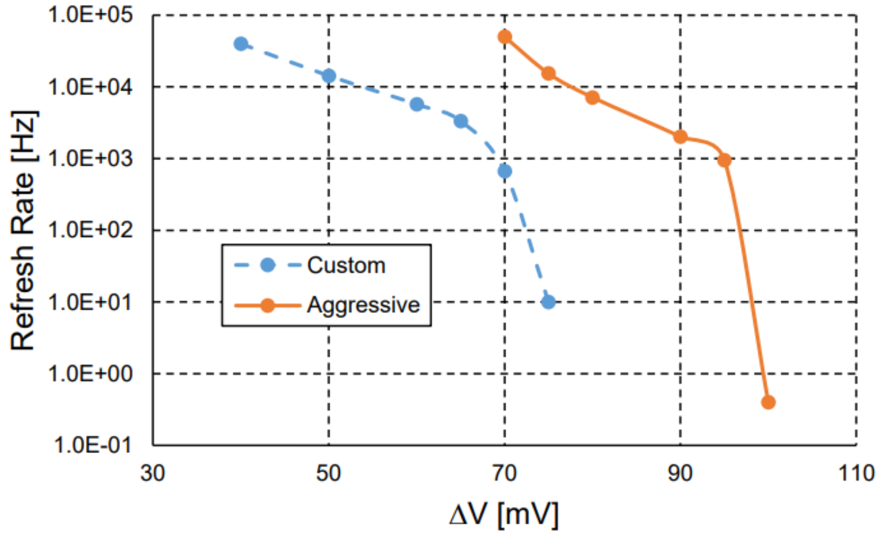


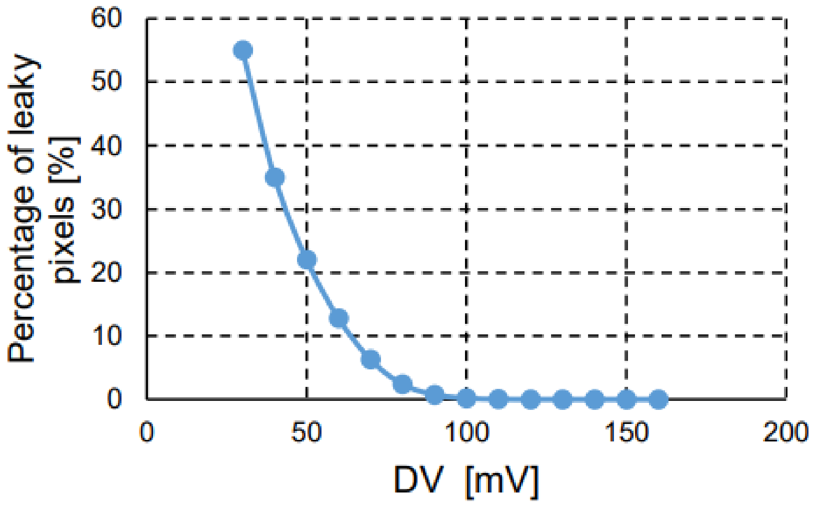


Q_T depends on ΔV and not any more on V_{dd}.
Test structure shows a minimum Q_T lower than 1ke$^-$
Not sensitive to α-particle. Not tested with laser.

Experimental results: aggressive array

Measurement



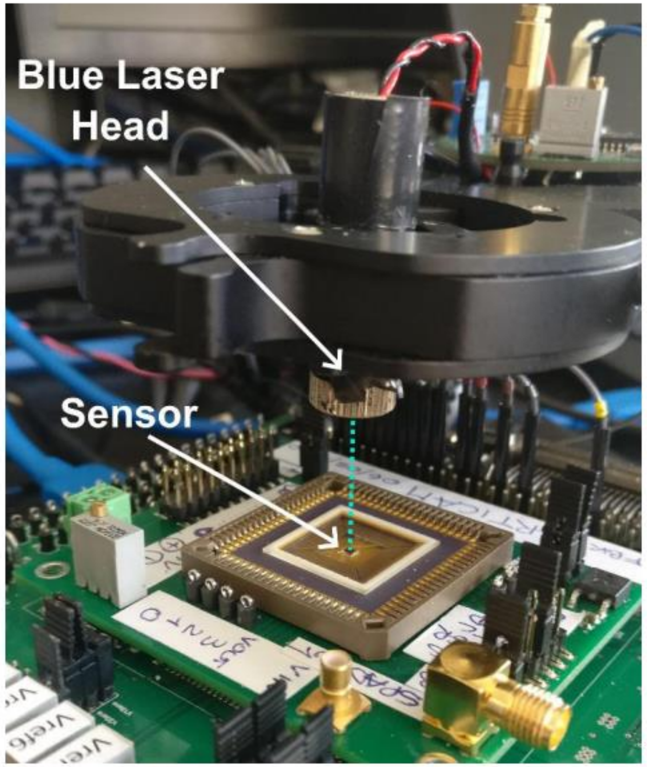


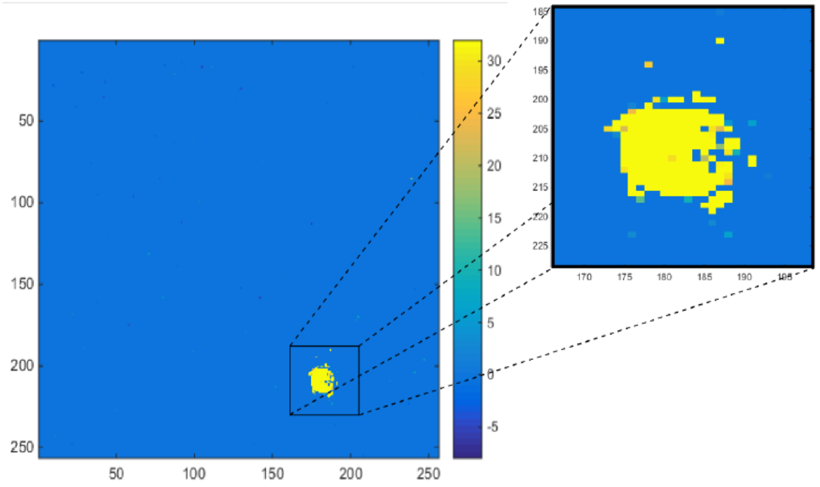
ΔV is a handle for increasing sensitivity, to be balanced with higher unprovoked switching (dark counts). Low values of ΔV induce more spurious events → tune the refresh rate (dependent on temperature).

Percentage of spurious events for different ΔV

Experimental results: aggressive array

Response to a pulsed (420 nm) focused laser

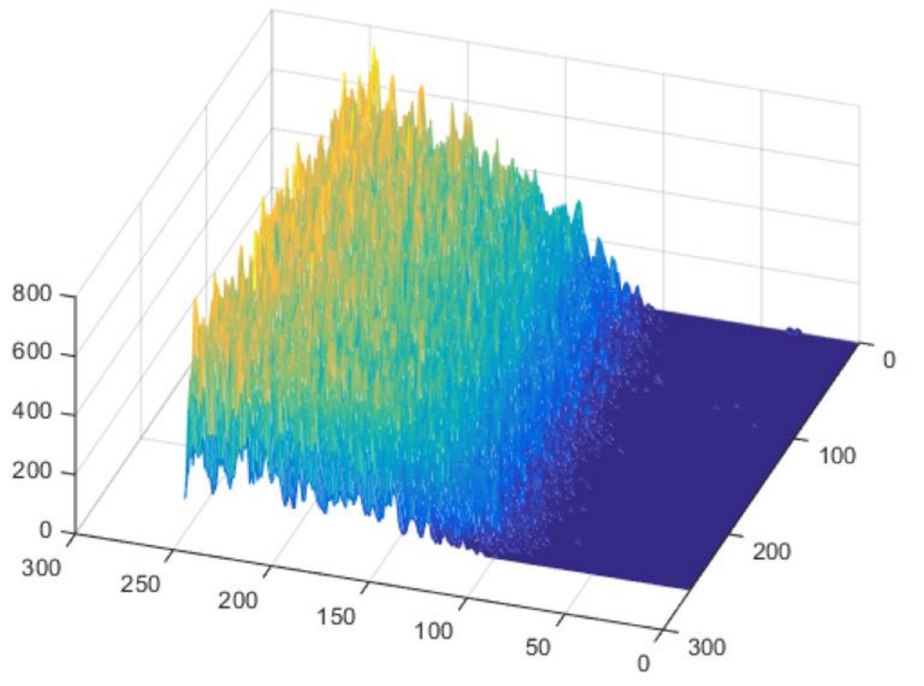




Response to a laser pulse: 10 pulses for each integration time (ΔV = 100mV) and multiple acquisitions

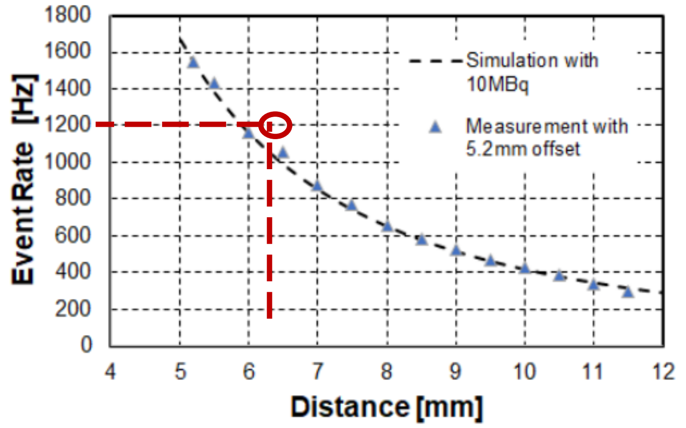
Experimental results: aggressive array

Response to α-particles



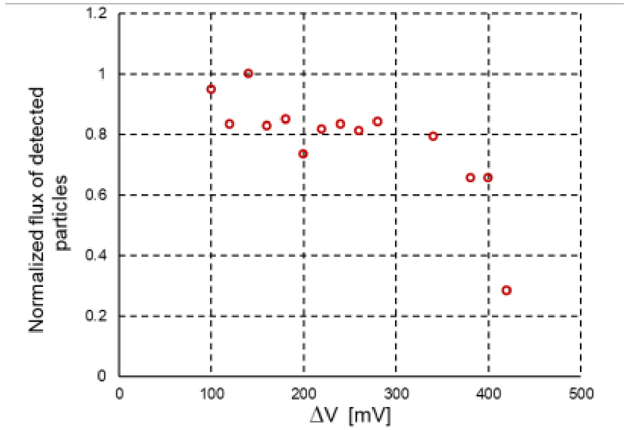
Response to alpha particle with a metallic shield interpose between the source and the detector

Detection efficiency



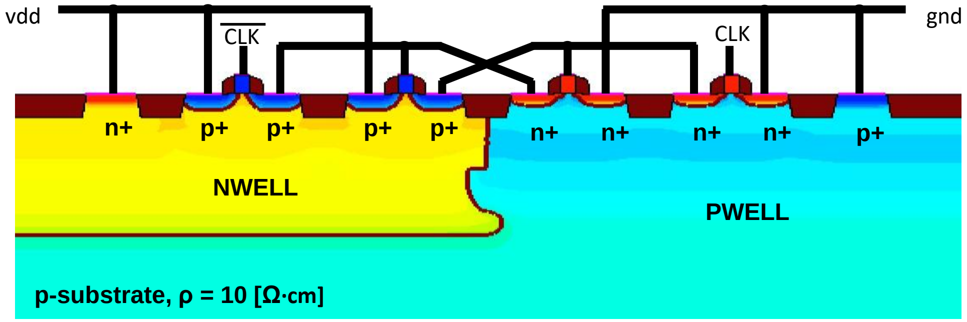
Expected flux and measured flux with a fast (FBK) fully depleted detector. Measured flux of PartiCam chip is about 100 Hz at roughly 6.5cm distance → efficiency **10 time** less

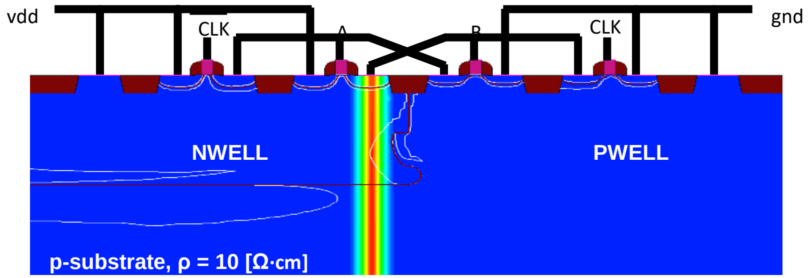
Sensitivity as a function of ΔV



Workable plateau for sensitivity. Drop for ΔV > 350mV

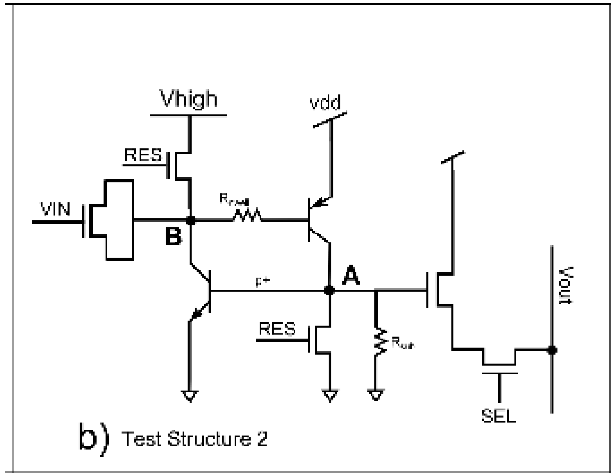
Reasons for reduced efficiency?

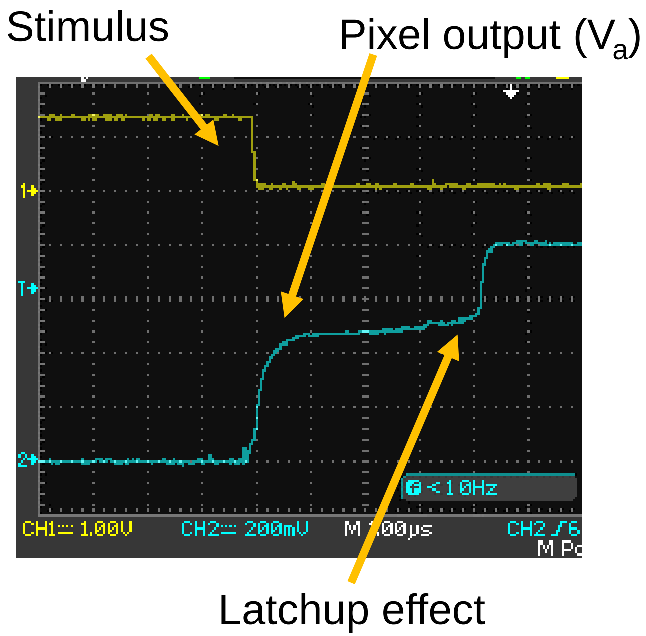




Experimental results: exploratory array

Injection pulse on test structures



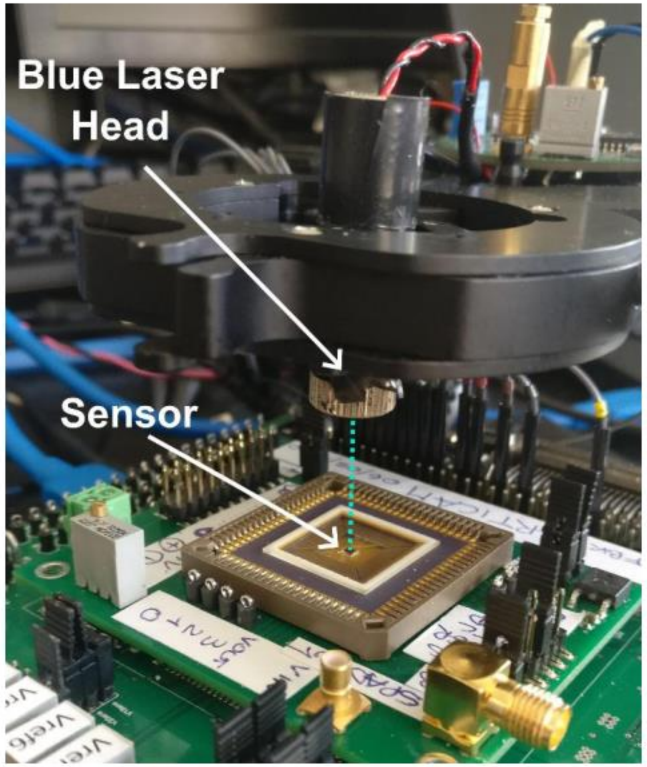


Difficult to measure the effective Q_T

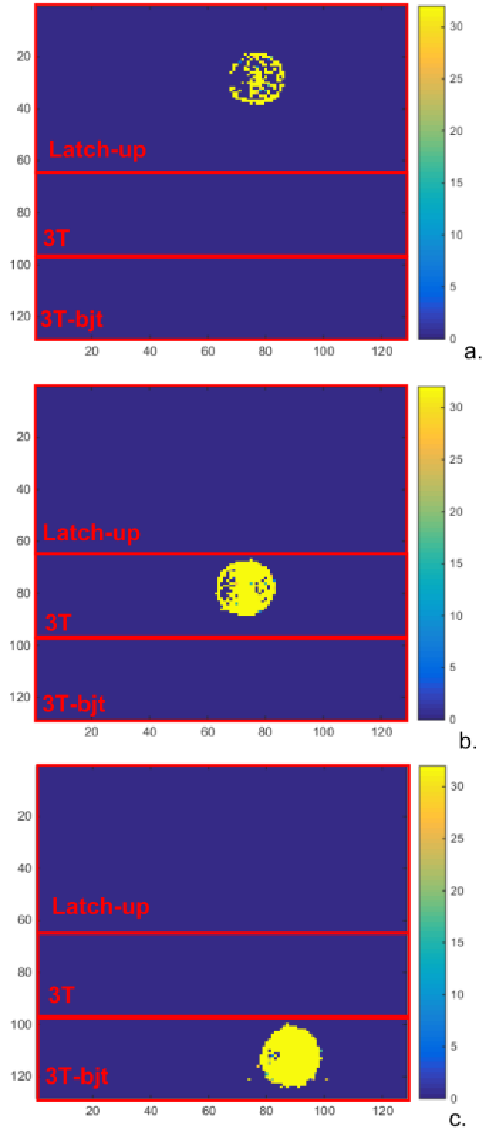
We observe of the activation of the positive feedback

Experimental results: exploratory array

Pulsed (410 nm) focused laser

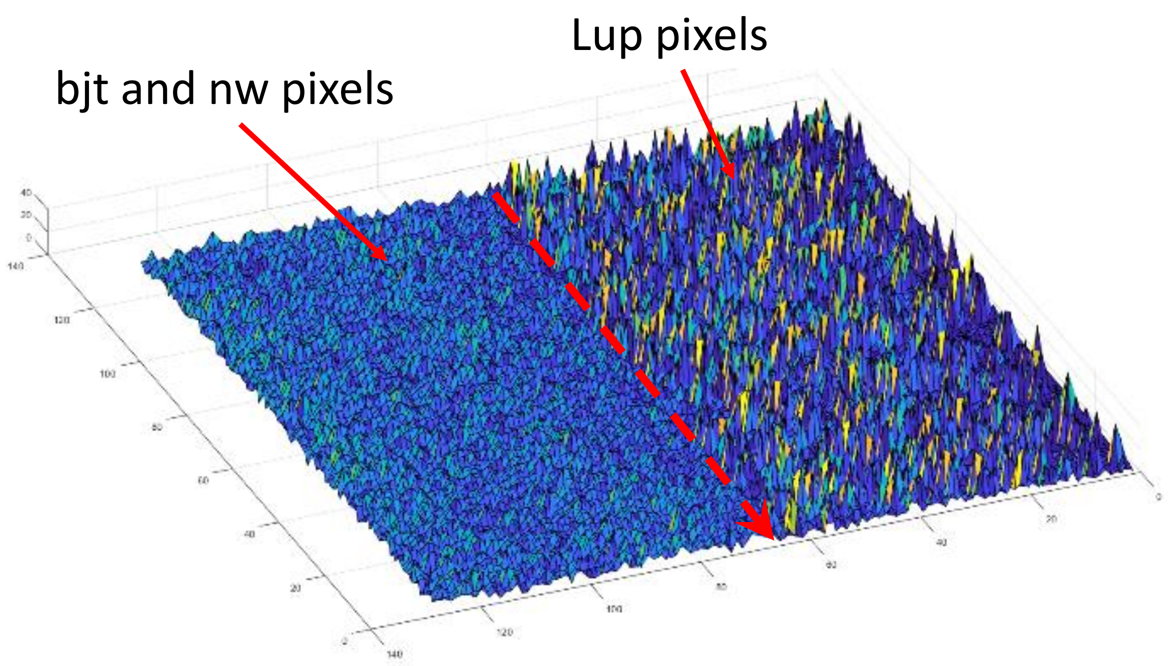


Response to four laser pulses per integration time

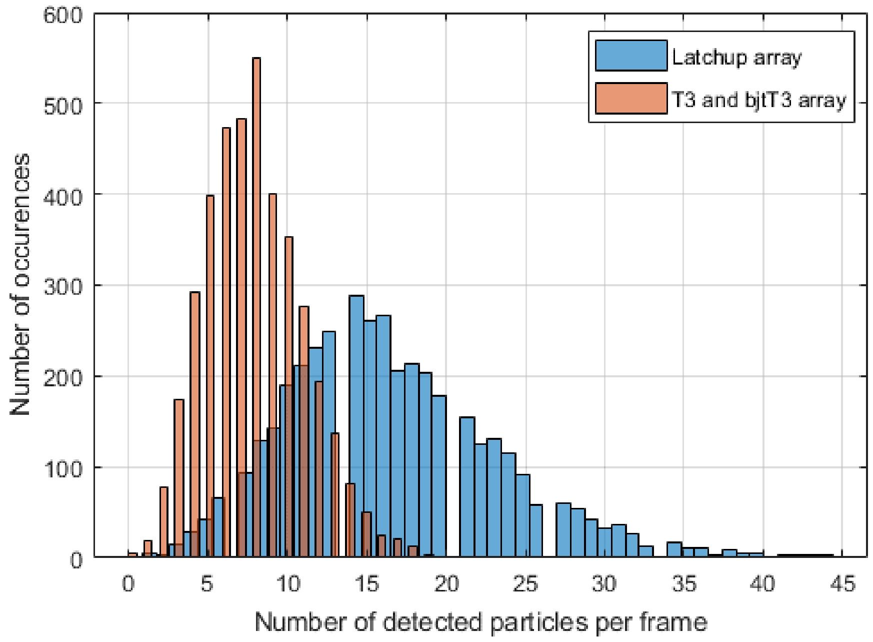


Experimental results: exploratory array

α-particle illumination



1000 acquisitions each having 35ms

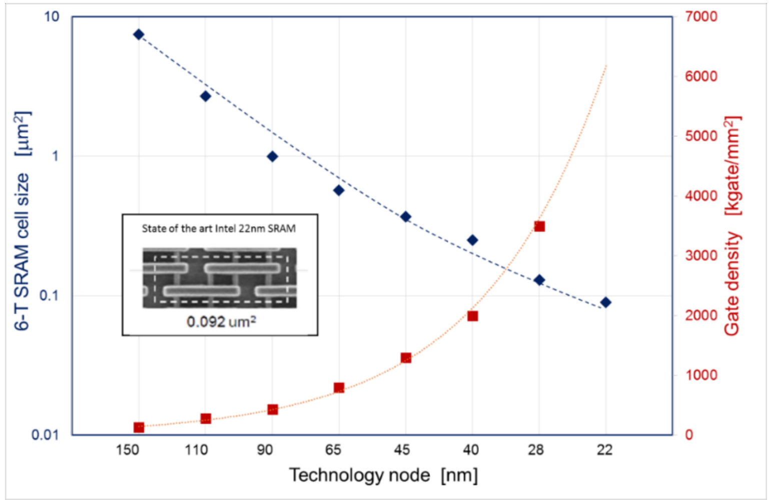


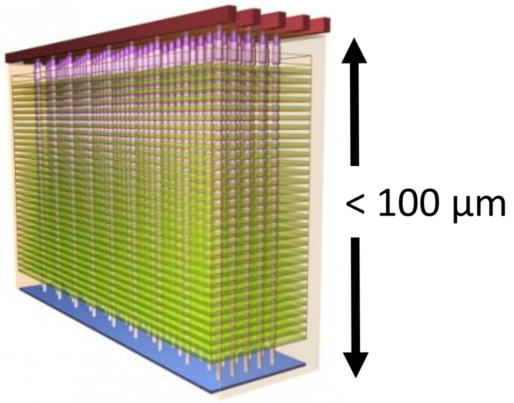
Lup pixel appears to be more sensitive wrt bjt and nw pixel.

OUTLOOK:

A novel design for position sensitive detectors without an analogue amplifier has been proposed and validated with signals from laser and alpha particle illumination.
A few variant have been implemented giving indication on the most efficient layout.
The limited efficiency to alpha particles was anticipated and it is further being investigated to confirm the reason (limited/no depth extension of the collecting junction).
Future steps:

- confirm the results achieved with a technology that allows for deeper charge collection at the collecting node (targeting sensitivity to minimum ionising particles).
- pursue a survey campaign of available small feature size CMOS nodes allowing for deeper depletion (higher substrate resistivity, SOI solutions, …).
- simulate the most promising technologies as accurately as possible
- proceed to design/simulate alternative layouts

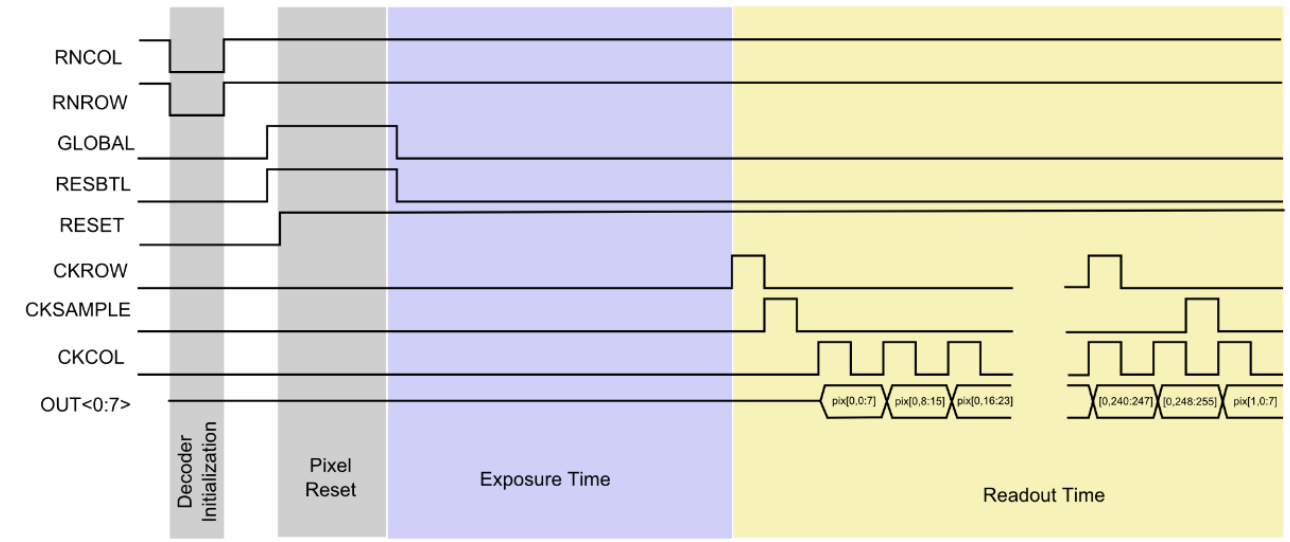




SPARE SLIDES

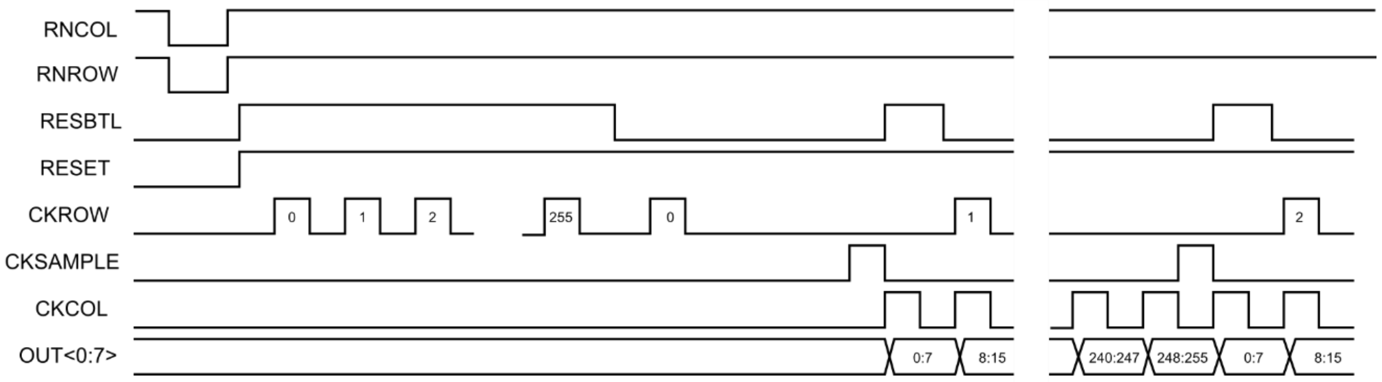
PartiCam chip

General Architecture



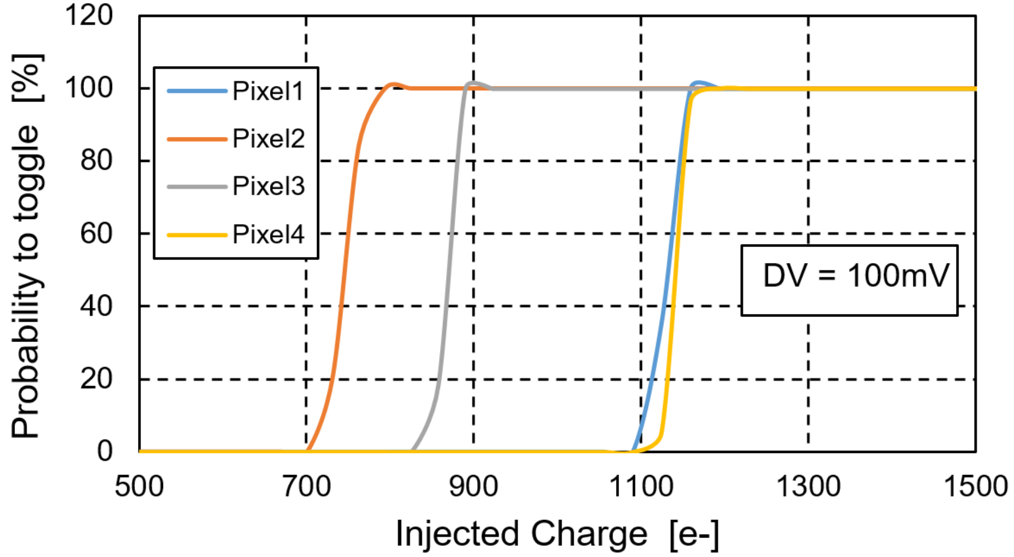
Global shutter:

- All pixels are reset at the same time and exposed to the radiation in parallel
- Pixel are then readout sequentially (detector dead time)



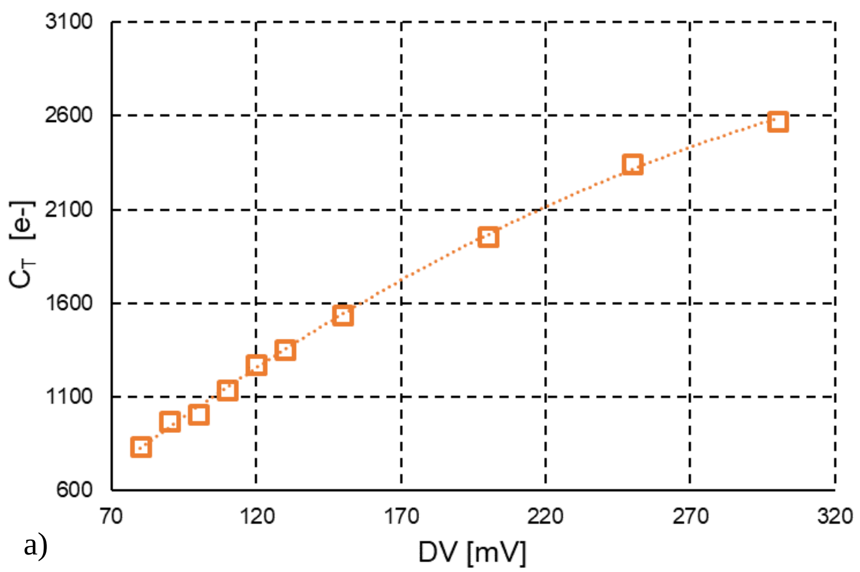
Rolling shutter:
Pixels are reset and starts integrating sequentially (do not see events in parallel)
Pixel are then readout sequentially (row dead time)

Implementing designs for an MPW UMC 65nm run

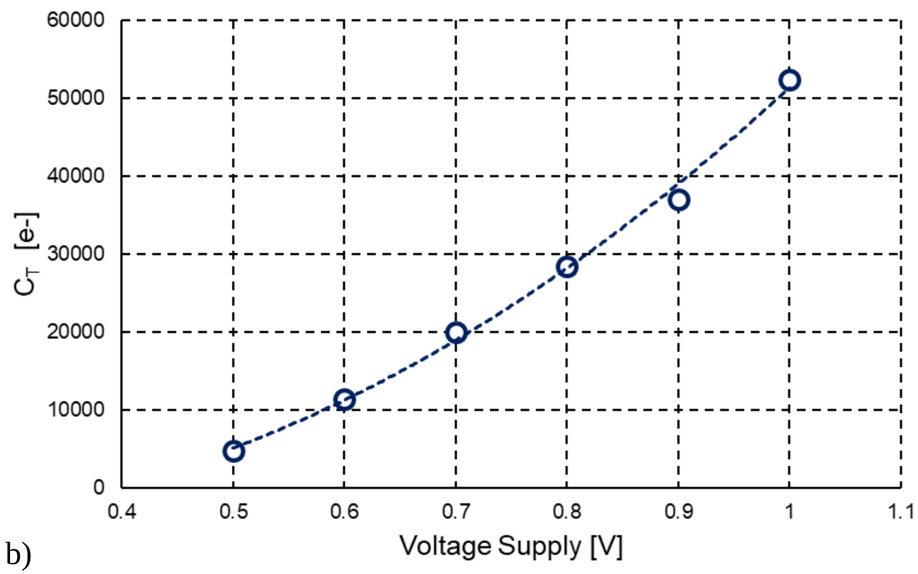


Typical switching probability of four test pixels (Lemu circuit) as a function of the injected charge, with DV fixed at 100 mV. The value of charge at which the curves cross the 50% probability is taken as C_T.

Results: injection circuit



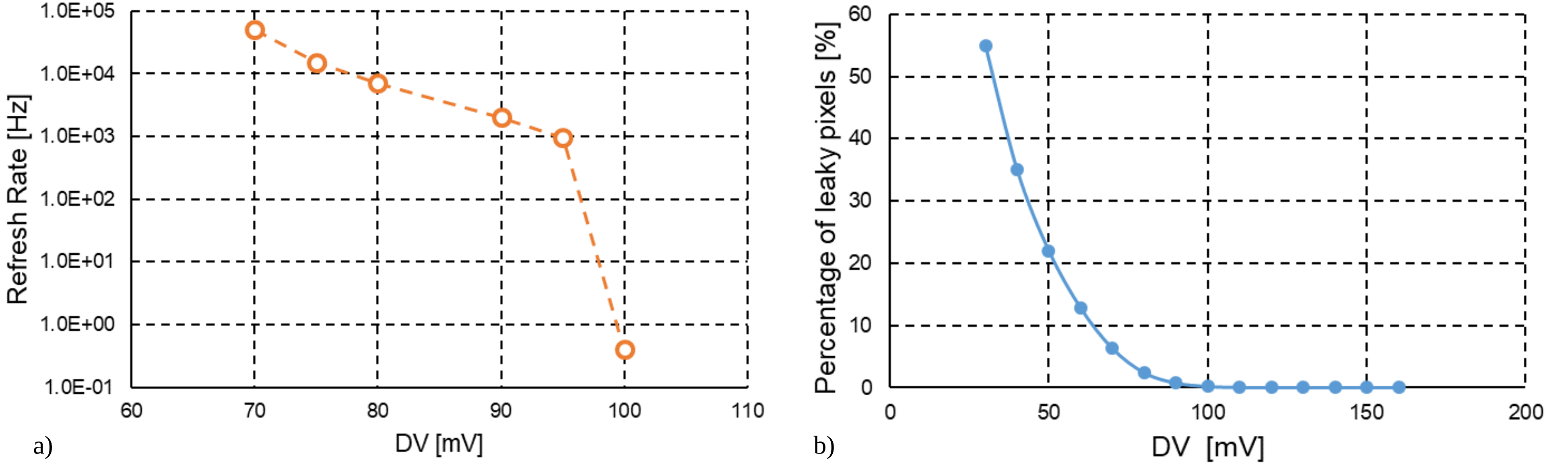
a)



b)

Threshold charge C_T as a function of DV for the LEmu cell (a) and C_T as a function of voltage supply (V_{DD}) for a modified SRAM (b). The measurement shows an improvement of roughly one order of magnitude going from a custom SRAM to the LEmu cell.

Results: dark runs



a) Refresh rate for false hit suppression as a function of DV for the LEmu layout; b) percentage of firing pixels in no-illumination conditions as a function of DV.