ToASt : a 64-channel ASIC for the readout of the Silicon Strip Detectors of the PANDA experiment

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The design of the Micro Vertex Detector (MVD) for the PANDA experiment is optimized for the detection of secondary vertices and maximum acceptance close to the interaction point. The MVD consists of a 4-layer barrel section, placed around the interaction point, and a 6-disks forward section, located in the forward position. The outermost layers of the MVD will be equipped with double sided Silicon Strip Detectors (SSDs). The SSD electronic readout must provide both the spatial position and the energy deposited by the impinging particles. Moreover, since PANDA is a triggerless experiment, each event must be tagged with its time of arrival (ToA).

In order to cope with these requirements a 64-channel dedicated ASIC, named ToASt, has been designed and tested. Each channel includes a charge-sensitiveamplifier, a current mode shaper, a linear time over threshold (ToT) stage and double threshold discrimination. A 12-bit time stamp is distributed to allchannels; its value at the two edges of the output comparator is stored, thus providing both ToA and ToT. The two values are immediately readout by a digital interface, formatted in 32-bit words and transmitted via two 160 MS/s serial links.

ToASt is designed in a commercial 110 nm CMOS technology. The die size is
4.4×3.2 mm^2; the input pads are located on one side of the die while all other pads are on the opposite side, thus allowing multiple dies being placed very close to each other. The digital logic has been triplicated for Single-Event Upset (SEU) protection.

ToASt has been extensively tested in laboratory standalone and connected to a detector, showing excellent performances. It has also been used in a beam test at the COSY facility in Juelich. Radiation tolerance tests for total dose and SEU have also been performed.

Collaboration

PANDA-FairNet

Role of Submitter

The presenter will be selected later by the Collaboration

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