

# The **MONOLITH** ERC Advanced project: towards **picosecond timing** with monolithic silicon

*Giuseppe Iacobucci* — Université de Genève



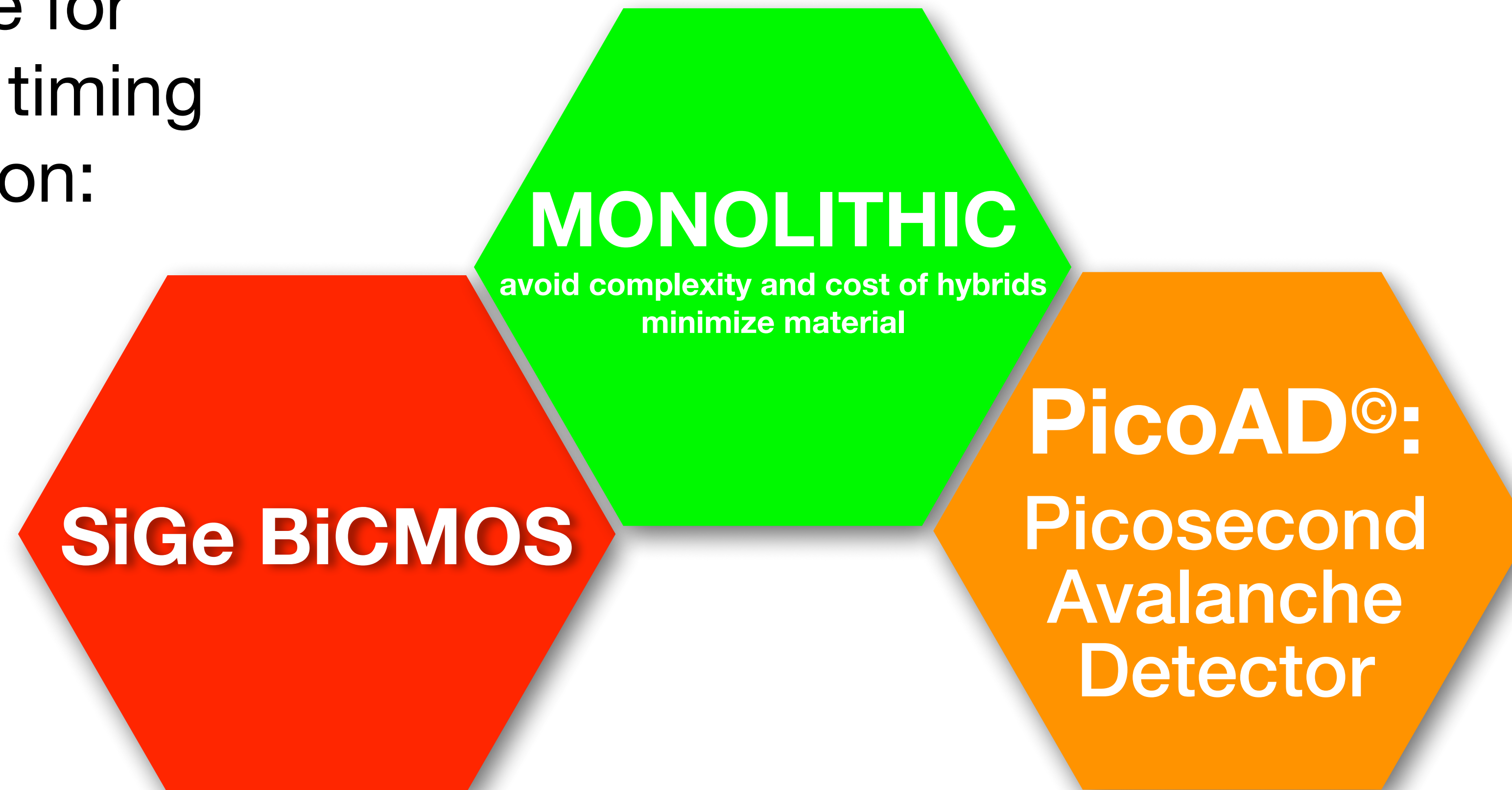
# The **MONOLITH** Project



European Research Council  
Established by the European Commission

Funded by the H2020 ERC Advanced grant 884447,  
**July 2020 - June 2025**

Our recipe for  
picosecond timing  
with silicon:

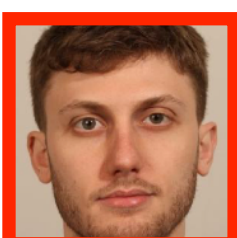




**Giuseppe Iacobucci**  
• project P.I.



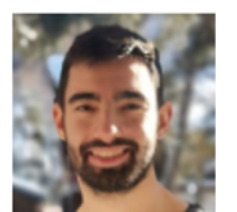
**Thanushan Kugathasan**  
• Lead ASIC design  
• Analog electronics



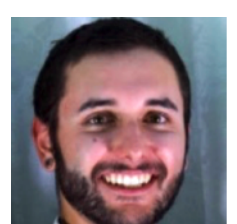
**Leonardo Cecconi**  
• ASIC design  
• Digital electronics



**Stefano Zambito**  
• Laboratory tests  
• Data analysis



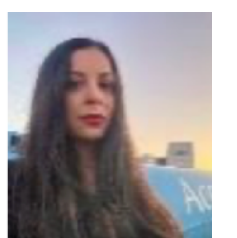
**Jordi Sabater Iglesias**  
• Detector simulation  
• Laboratory tests



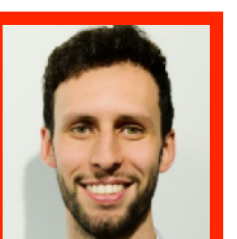
**Matteo Milanesio**  
• Laboratory tests  
• Data analysis



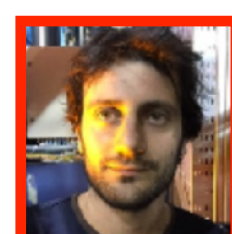
**Antonio Picardi**  
• ASIC design  
• Analog electronics



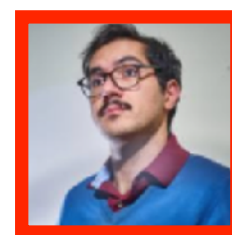
**Rafaella Kotitsa**  
• Sensor simulation  
• Data analysis



**Carlo Alberto Fenoglio**  
• Digital electronics  
• ASIC test



**Lorenzo Paolozzi**  
• Sensor design  
• Analog electronics



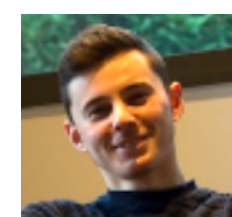
**Roberto Cardella**  
• Sensor design  
• Analog/Dig electronics



**Mateus Vicente**  
• System integration  
• Laboratory tests



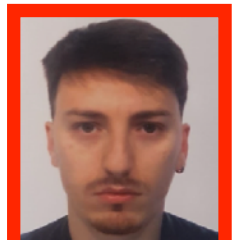
**Chiara Magliocca**  
• Laboratory tests  
• Data analysis



**Théo Moretti**  
• Laboratory tests  
• Data analysis



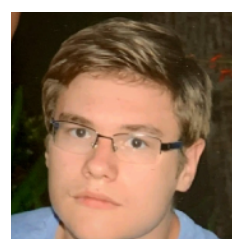
**Jihad Saidi**  
• Laboratory tests  
• Data analysis



**Luca Iodice**  
• Analog electronics  
• ASIC test



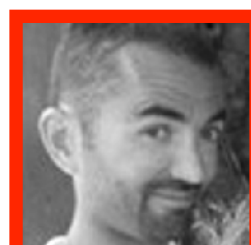
**Andrea Pizarro Medina**  
• Data analysis  
• Laboratory tests



**Ivan Semendyaev**  
• Data analysis  
• Laboratory tests



**Didier Ferrere**  
• System integration  
• Laboratory tests



**Yannick Favre**  
• Board design  
• RO system



**Sergio Gonzalez-Sevilla**  
• System integration  
• Laboratory tests



**Stéphane Débieux**  
• Board design  
• RO system

## Main research partners:



**Roberto Cardarelli**  
INFN Rome2 & UNIGE



**Holger Rucker**  
IHP Mikroelektronik



**Marzio Nessi**  
CERN & UNIGE



**Matteo Elviretti**  
IHP Mikroelektronik

## Funded by:



**Swiss National  
Science Foundation**



**European Research Council**  
Established by the European Commission

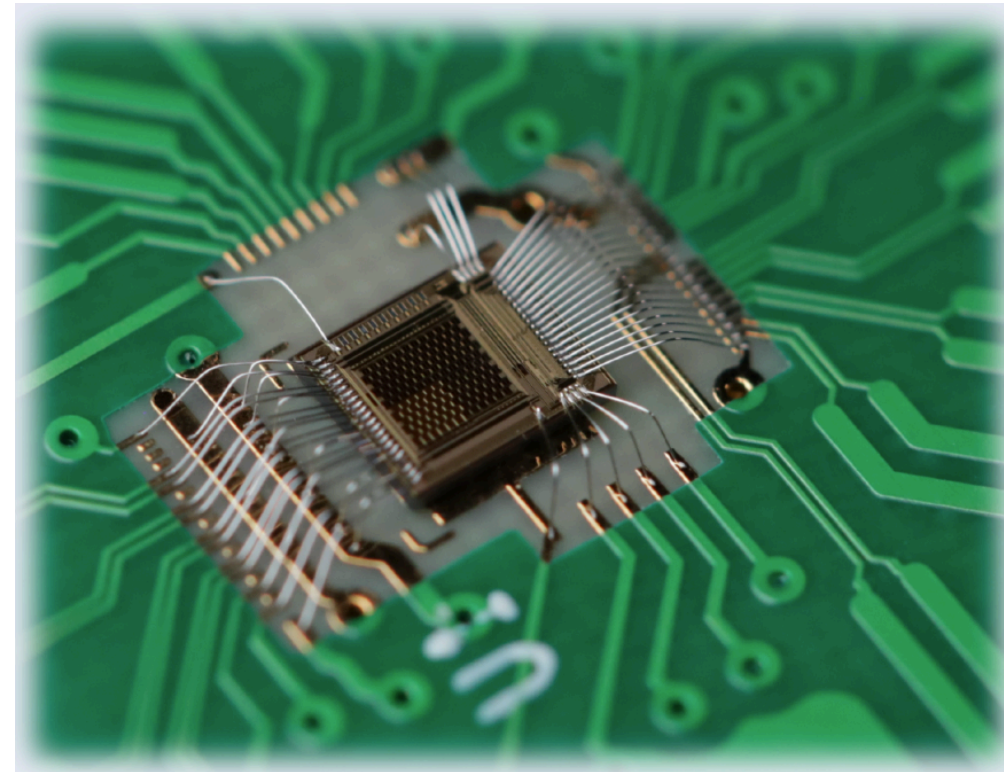


**Sinergia**

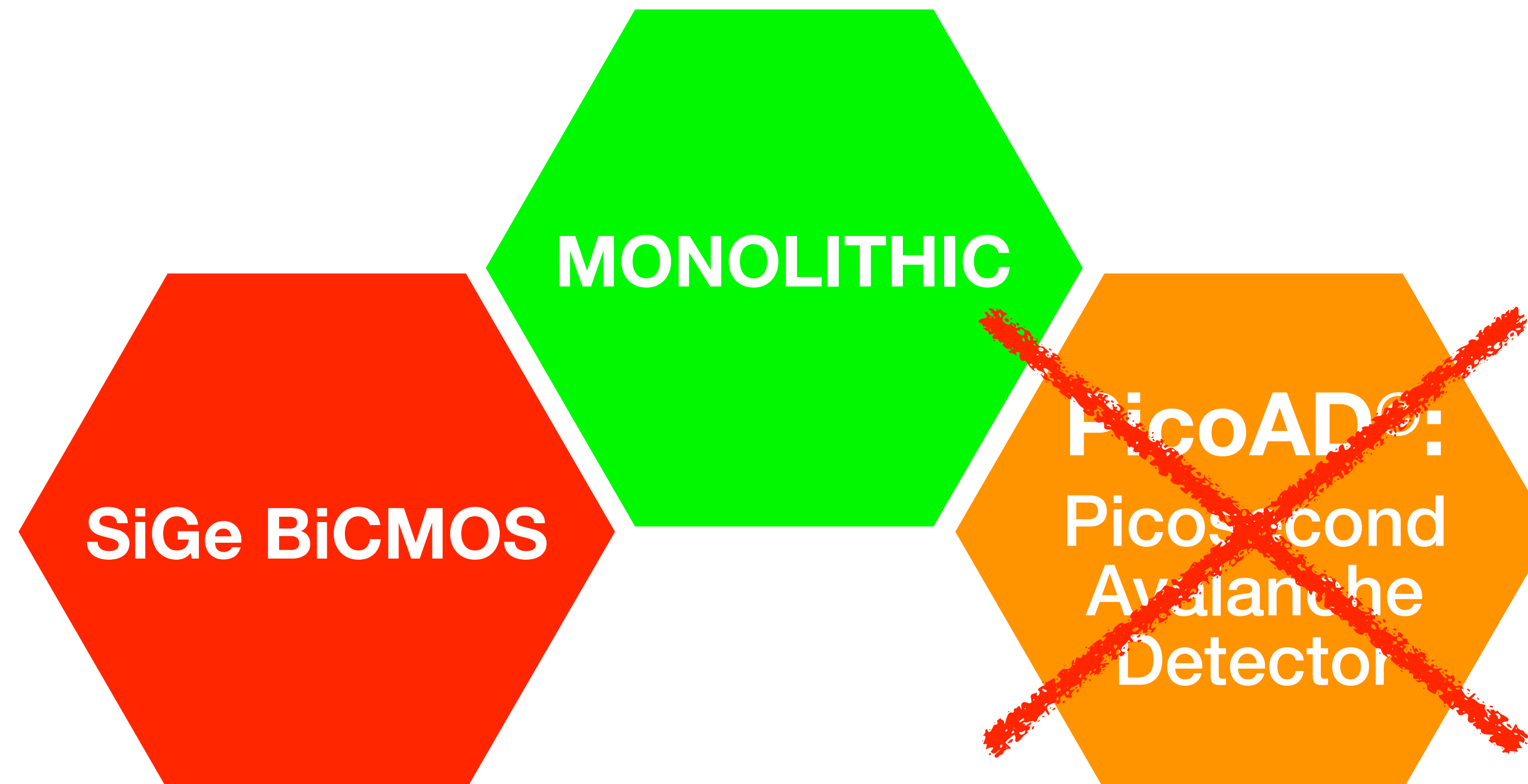


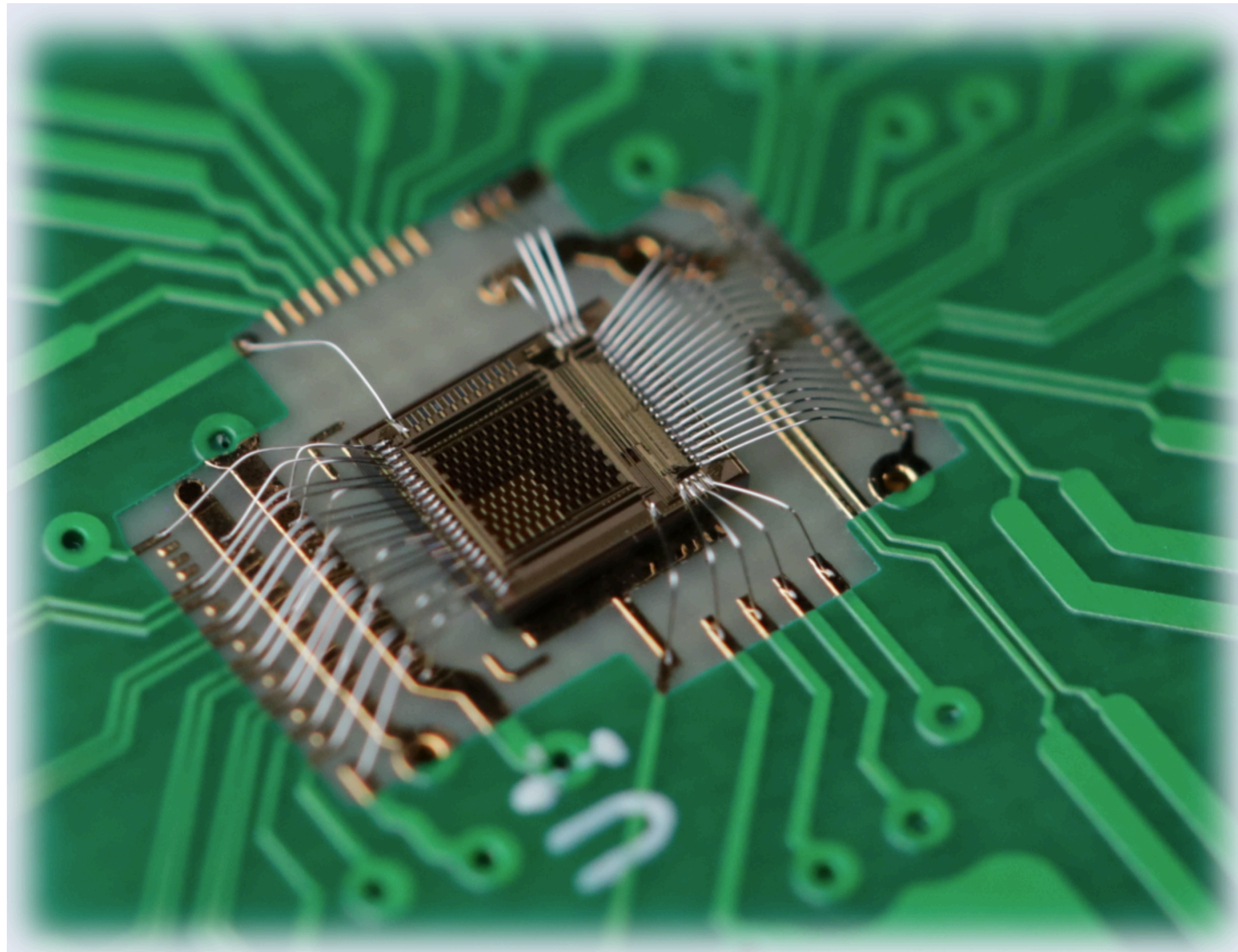
**UNIVERSITÉ  
DE GENÈVE**

**UNITEC**

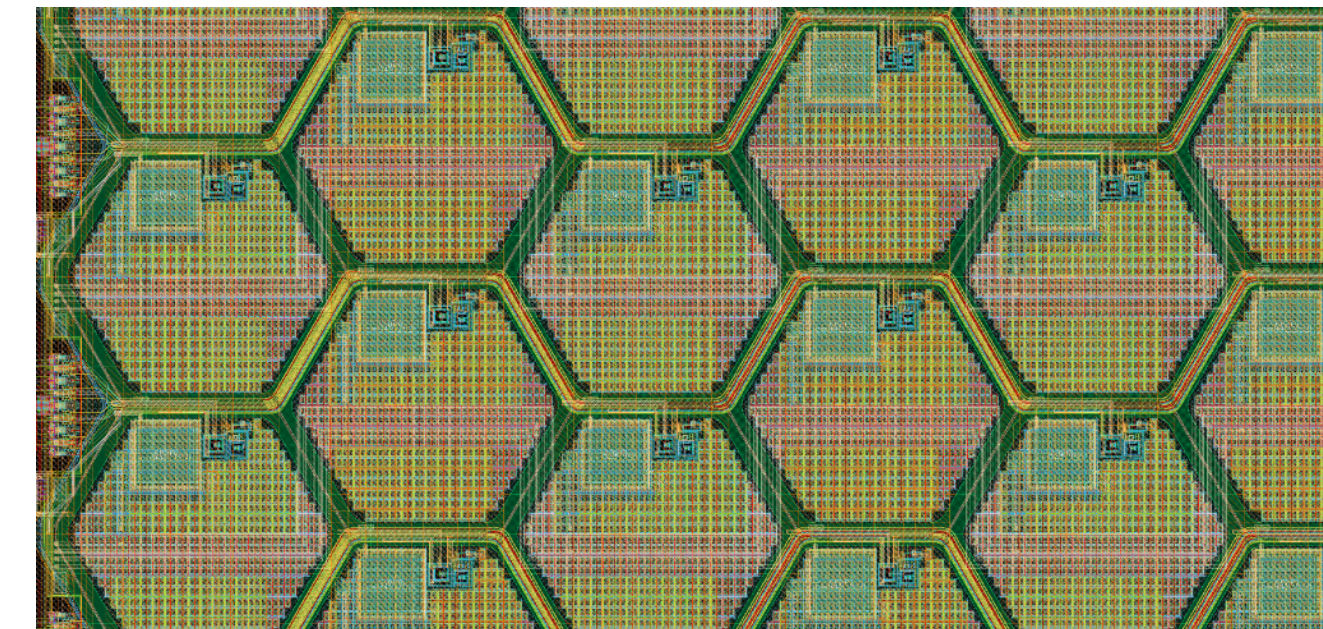


# 2022 prototype without gain layer





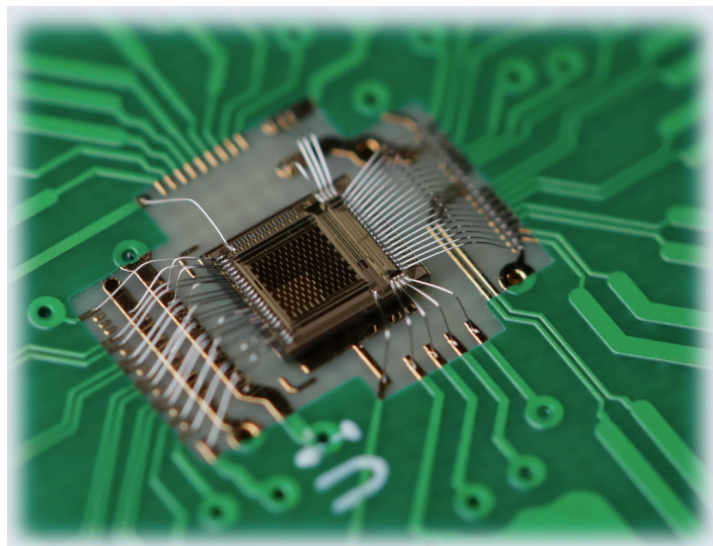
- ▶ **Sensor:** epilayer  $350\Omega\text{cm}$ ,  $50\mu\text{m}$  thick
  - ➔ simple pn junction, no gain layer
- ▶ **Electronics:** SiGe HBT frontend



- ▶ matrix of: 12x12 hexagonal pixels  
100 $\mu\text{m}$  pitch
- ▶ results from 4 analog channels

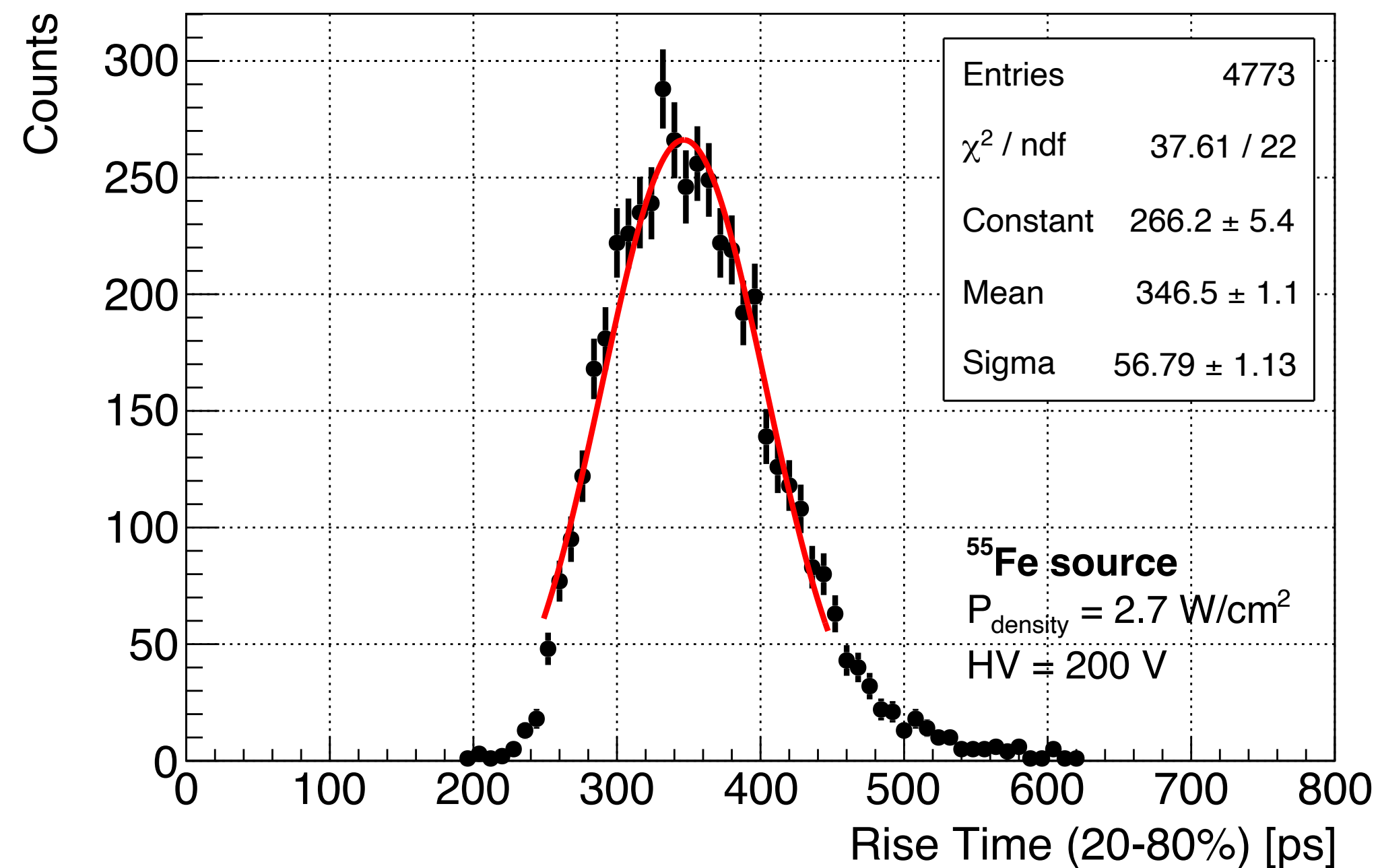


Leading-edge **IHP SG13G2** technology, **130 nm** process featuring **SiGe HBT**

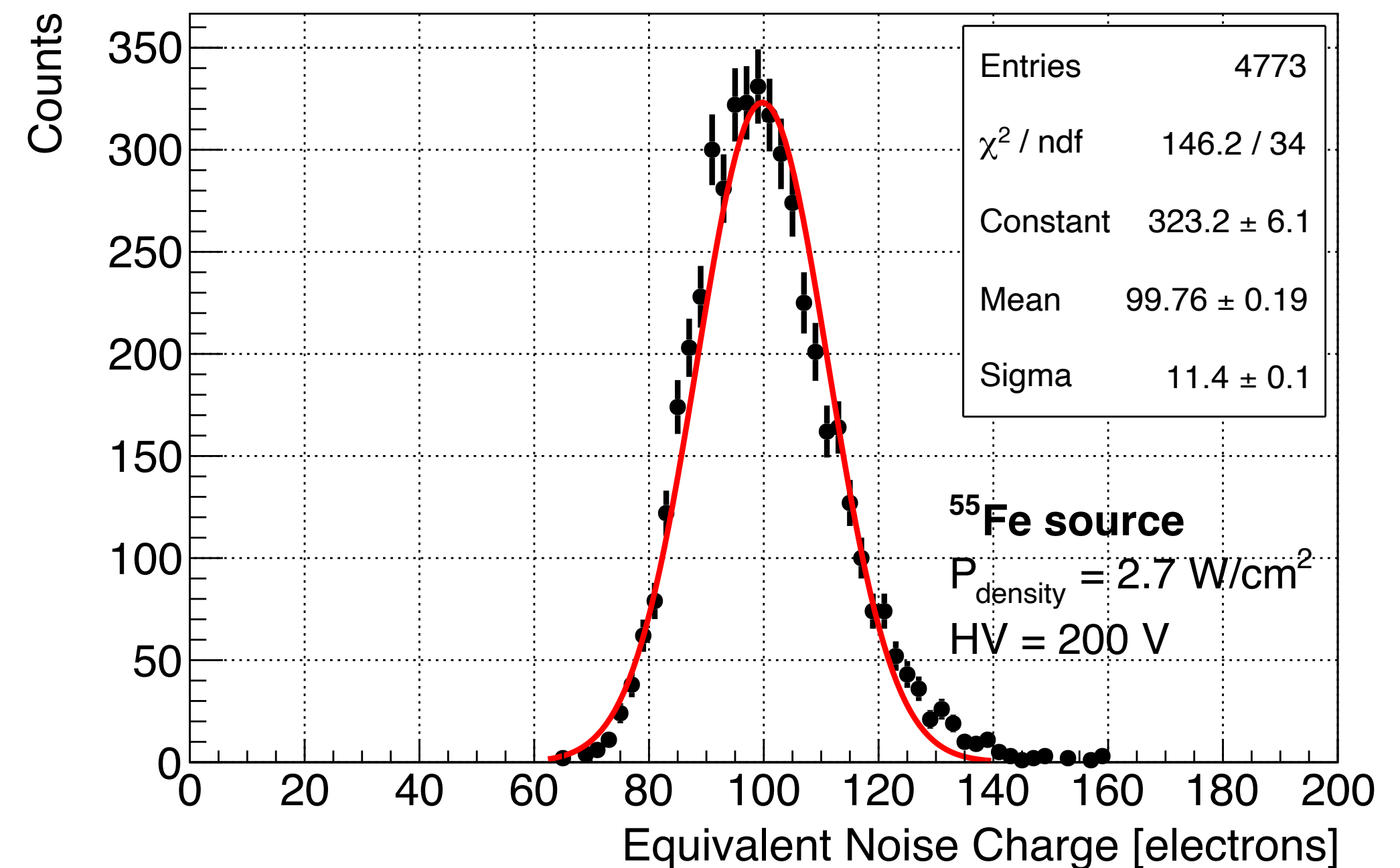


## <sup>55</sup>Fe measurements in cleanroom:

**Risetime (20%–80%)  $\approx$  350 ps**

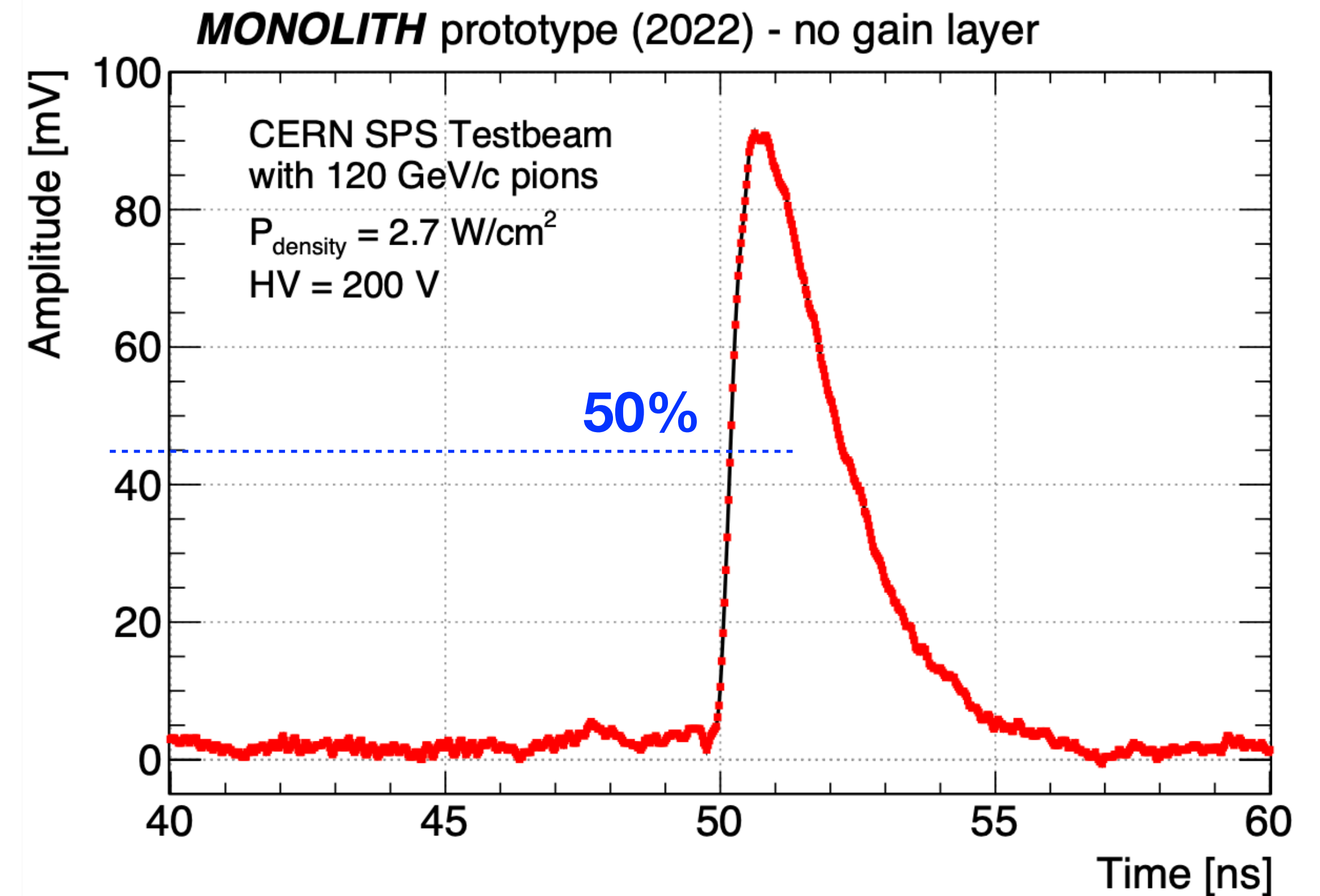


**ENC  $\approx$  100 e<sup>-</sup>**



We performed a **very simple analysis** of the data taken with the **analog channels**:

1. **Linear interpolation** of oscilloscope samplings (25ps)
2. Time Of Arrival taken at **50% of signal height**
3. **No further time-walk correction applied**

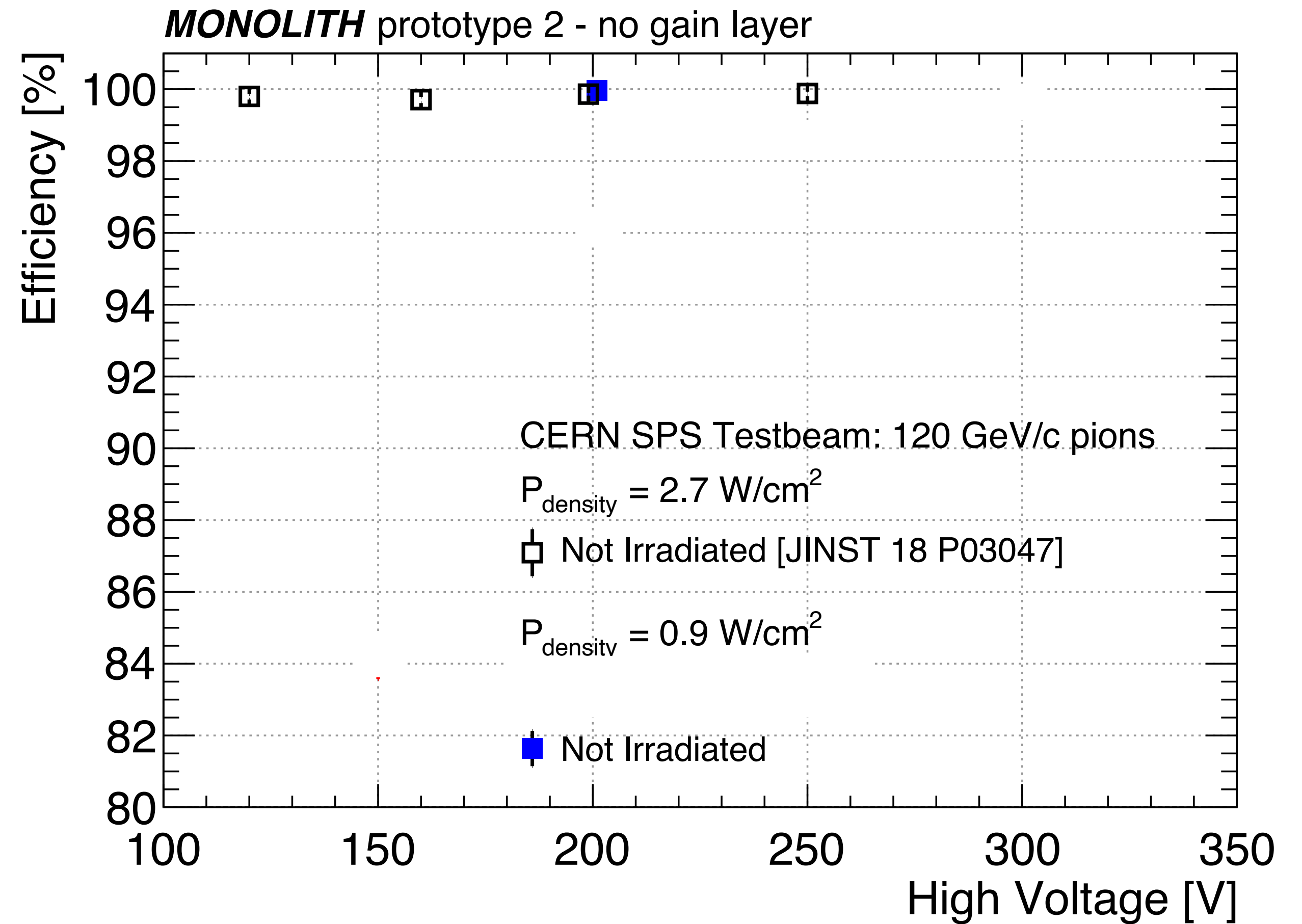


## CERN SPS testbeam results:

□ Unirradiated:

Efficiency =  $(99.96 \pm 0.02)\%$

at HV = 200 V

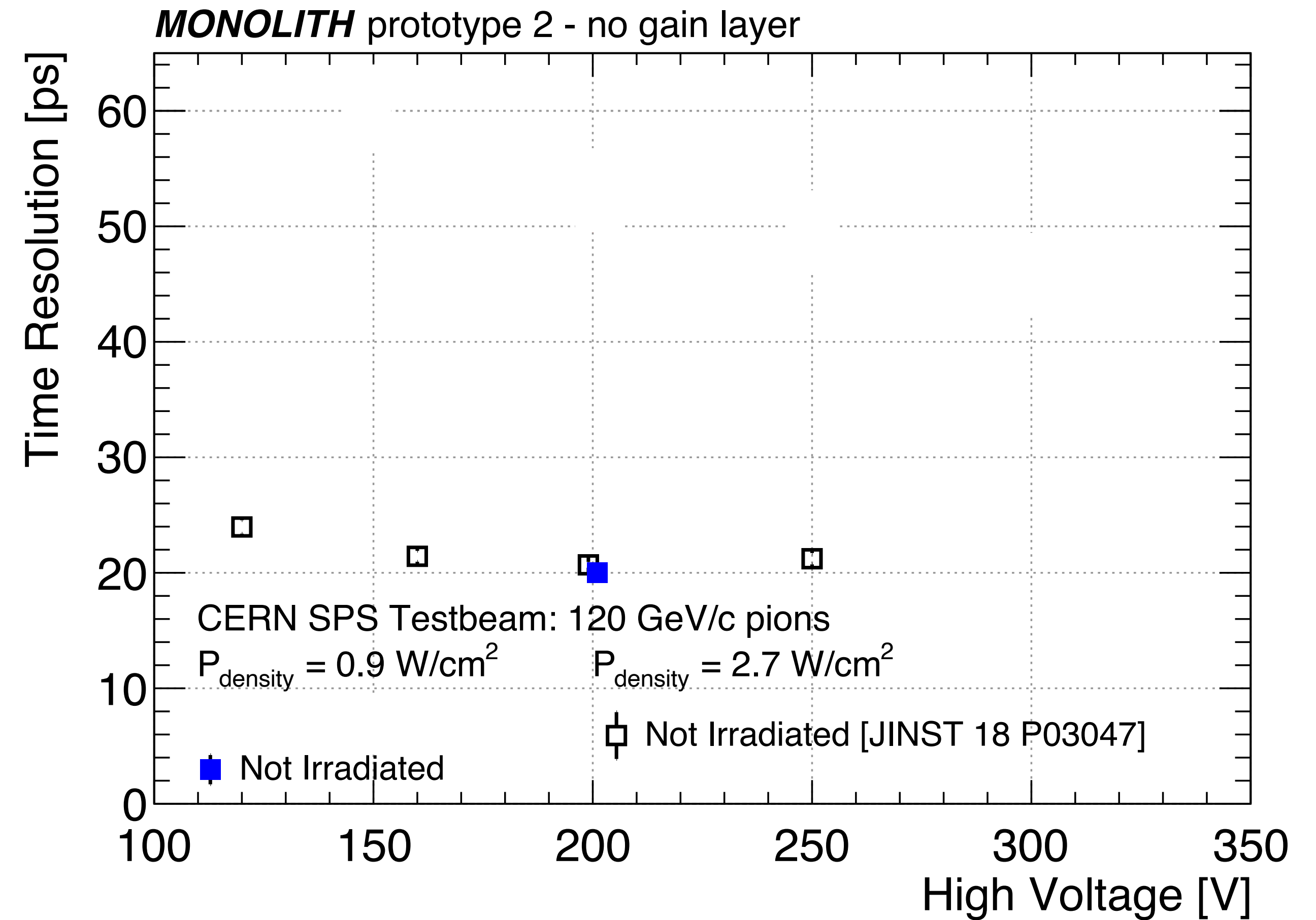




## CERN SPS testbeam results:

□ Unirradiated:

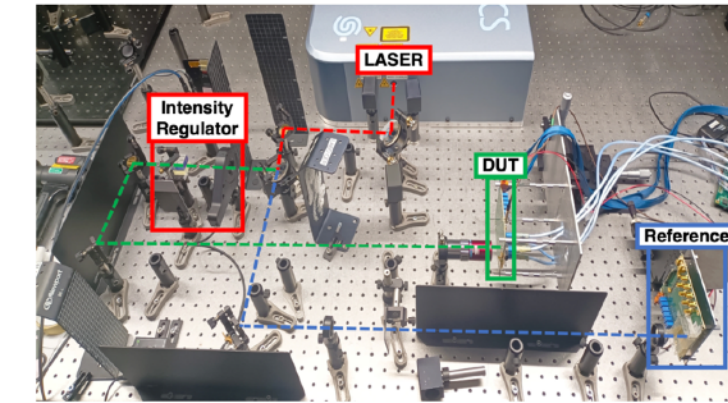
**20 ps** at HV = 200 V



**20 ps without gain layer**  
at 0.9 W/cm<sup>2</sup>

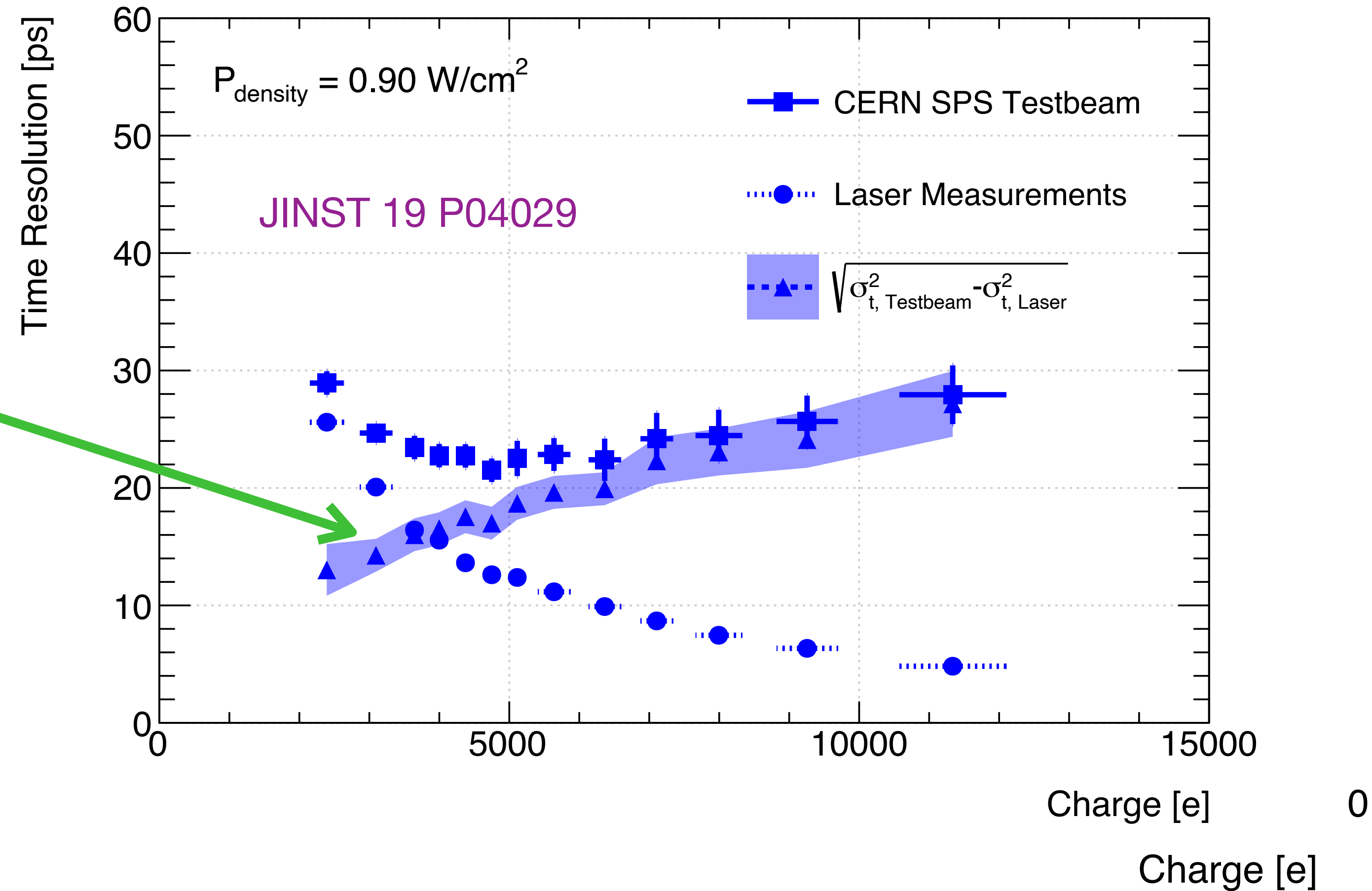
**Question # 1:**

**Is this the limit without gain layer ?**



Laser Measurement

MONOLITH prototype2 (2022) - no gain layer



The band estimates the charge-collection ("Landau") noise

**20 ps is pretty close the limit** of a PN junction without gain layer, due to Landau noise

Full efficiency and 20 ps  
at  $0.9 \text{ W/cm}^2$   
without gain layer

Question # 2:

**what is the key to success ?**



# what is the key to success ?



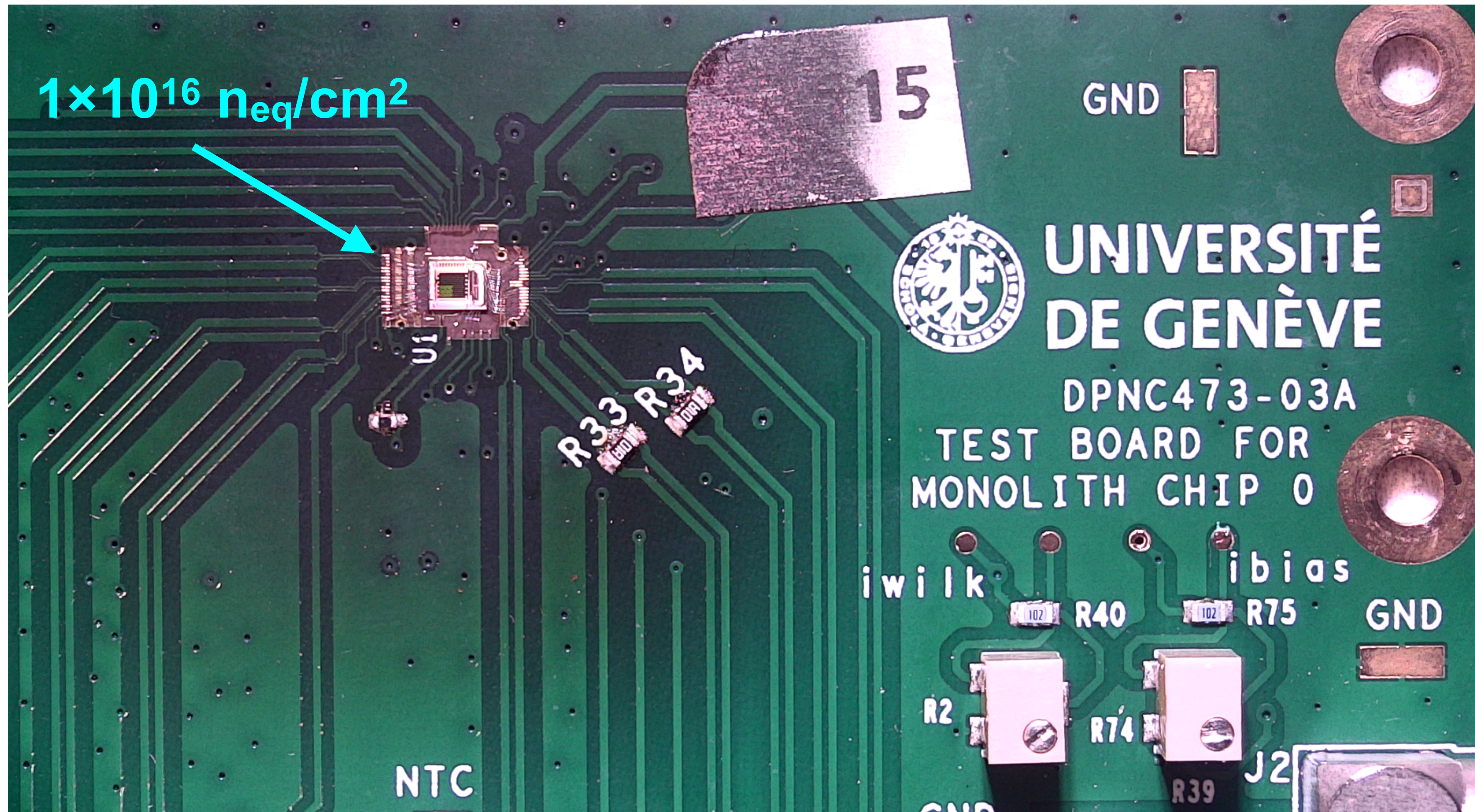
Should **SiGe BiCMOS** processes  
be considered  
for future 4D trackers ?

**Question # 3:**

**Is SiGe radiation hard ?**

Radiation tolerance studies in collaboration with **KEK** and **IHP** colleagues.

**8 samples** of MONOLITH prototype2 were irradiated with **protons** in Japan **up to  $1 \times 10^{16} n_{eq}/cm^2$**



Radiation tolerance studies in collaboration with **KEK** and **IHP** colleagues.

**8 samples** of MONOLITH prototype2 were irradiated with **protons** in Japan **up to  $1 \times 10^{16} \text{ n}_{\text{eq}}/\text{cm}^2$**

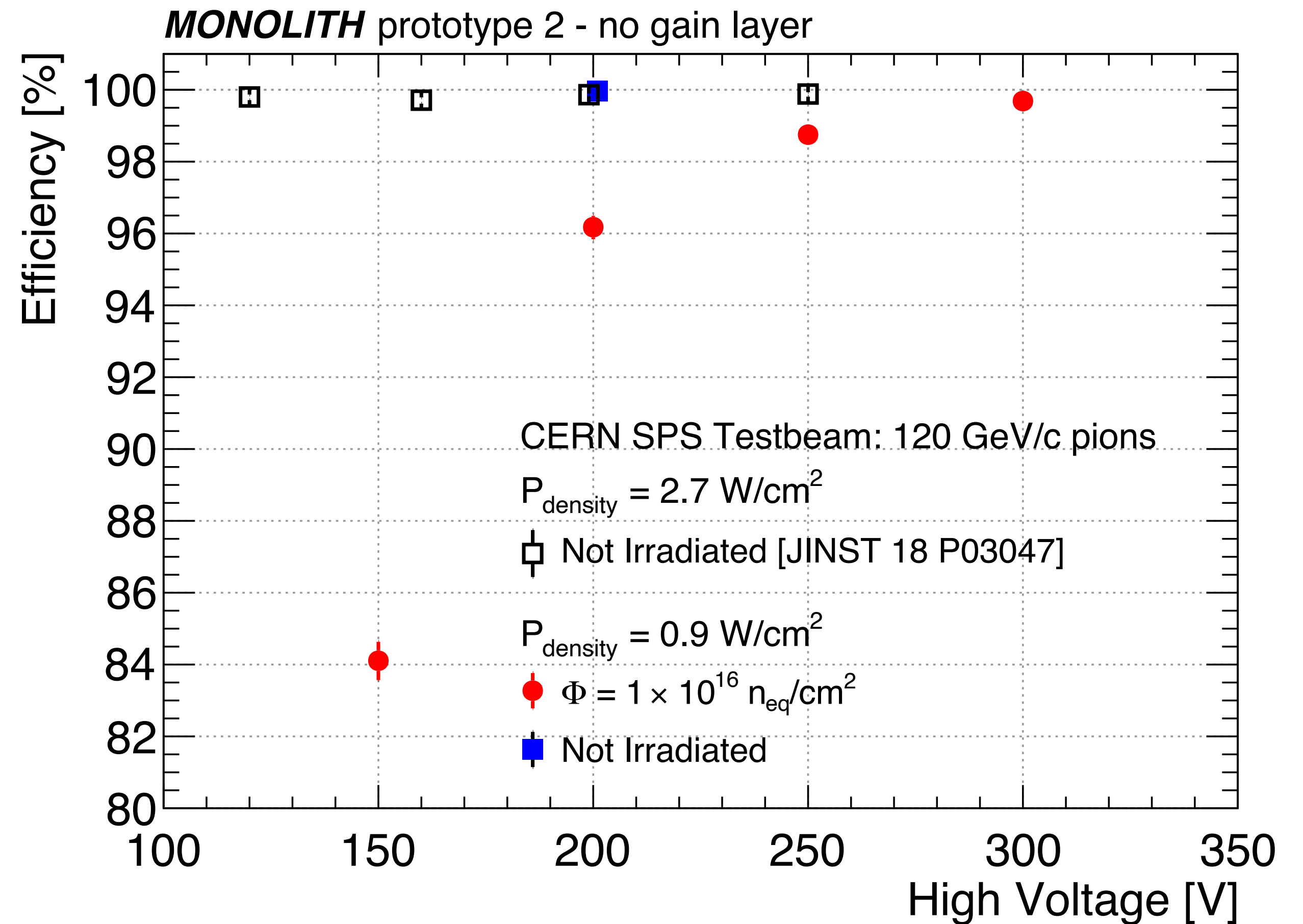
7 out of the 8 irradiated boards had **damaged voltage regulators**:  
we had to **bypass** them with wire bonds

Board Name	Fluence [1 MeV $\text{n}_{\text{eq}}/\text{cm}^2$ ]
M23	$2 \cdot 10^{13}$
M22	$9 \cdot 10^{13}$
M21	$6 \cdot 10^{14}$
M19	$6 \cdot 10^{14}$
M18	$3 \cdot 10^{15}$
M17	$3 \cdot 10^{15}$
M16	$1 \cdot 10^{16}$
M15	$1 \cdot 10^{16}$



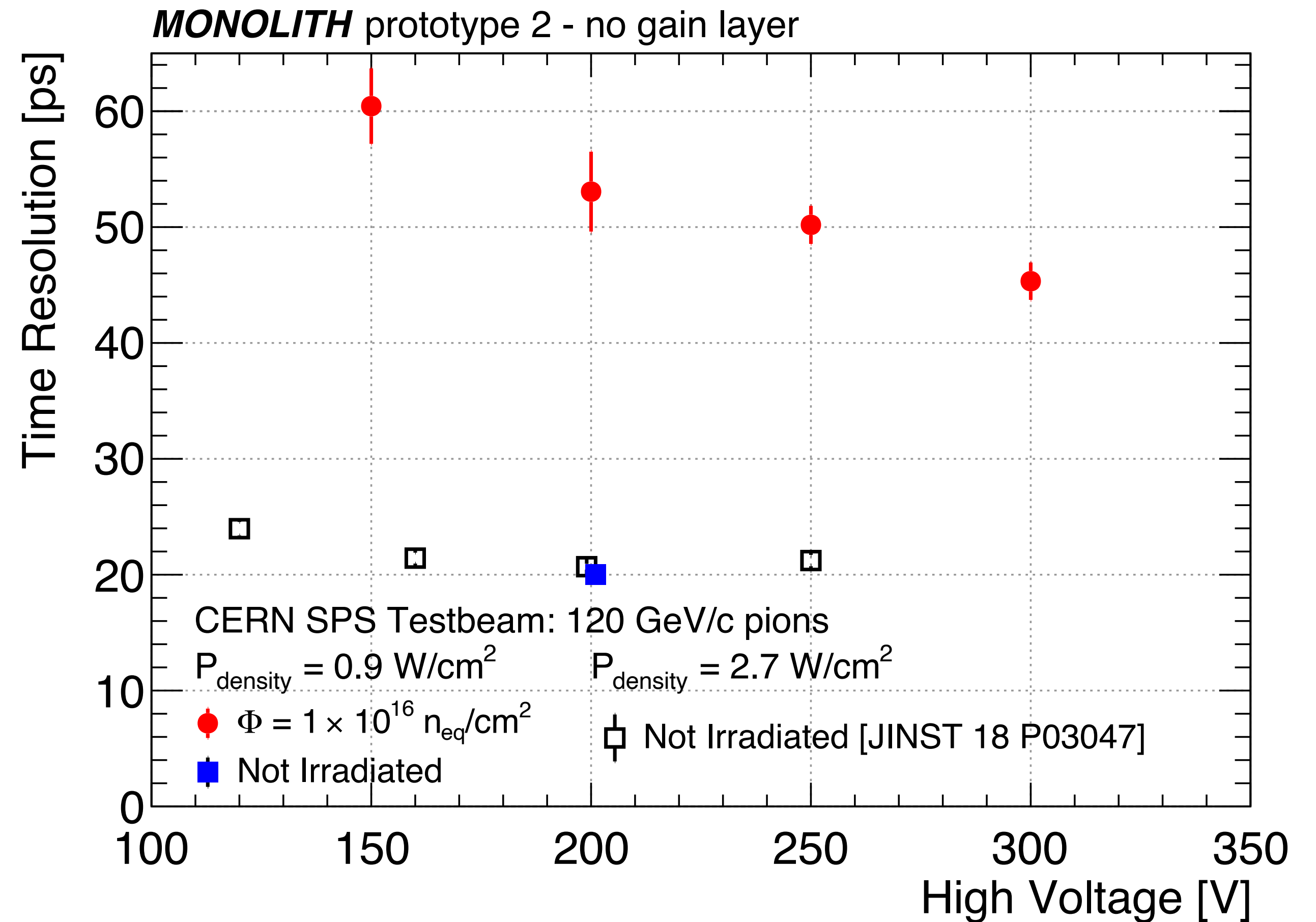
## CERN SPS testbeam results:

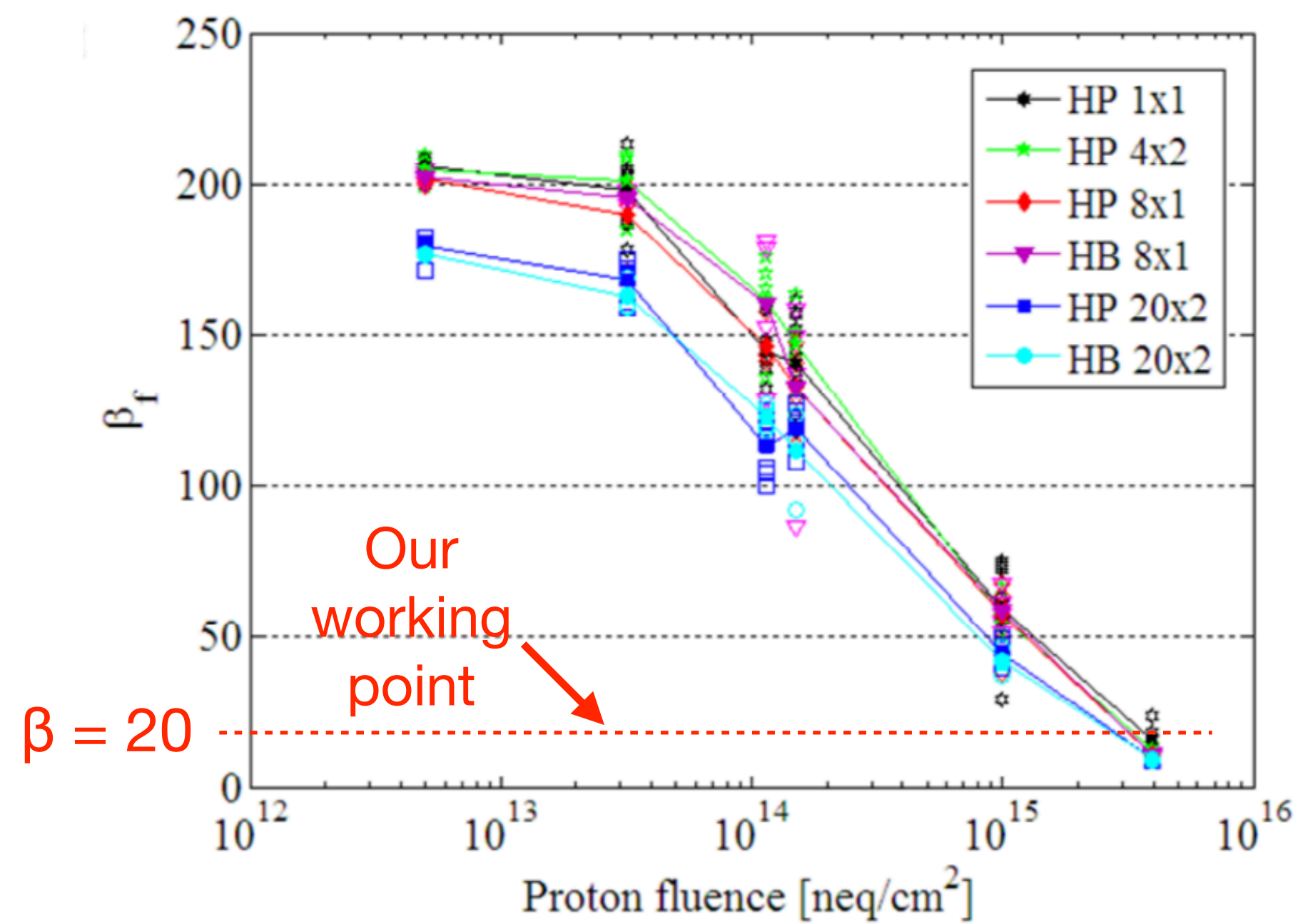
- Unirradiated:**  
 Efficiency =  $(99.96 \pm 0.02)\%$   
 at HV = 200 V
  
- $1 \times 10^{16} \text{ n}_{\text{eq}}/\text{cm}^2$ :**  
 Efficiency =  $(99.7 \pm 0.1)\%$   
 at HV = 300V  
 (higher HV still to be exploited)



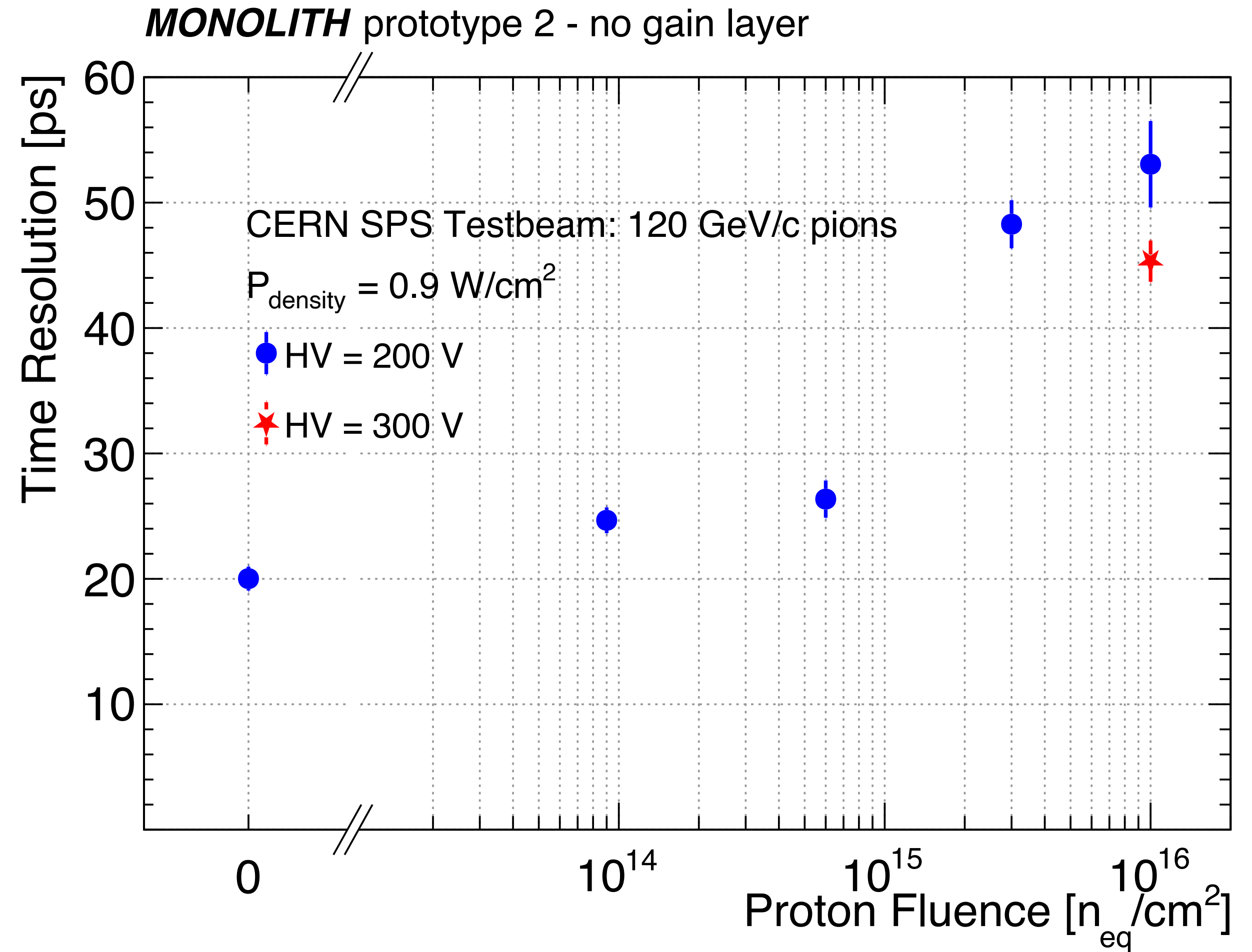
## CERN SPS testbeam results:

- Unirradiated:  
**20 ps** at HV = 200 V
- $1 \times 10^{16} \text{ n}_{\text{eq}}/\text{cm}^2$ :  
**45 ps** at HV = 300V  
(higher HV still to be exploited)





S. Díez et al, IEEE Nuclear Science Symposium & Medical Imaging Conference, Knoxville, TN, 2010, pp. 587-593, doi: 10.1109/NSSMIC.2010.5873828.



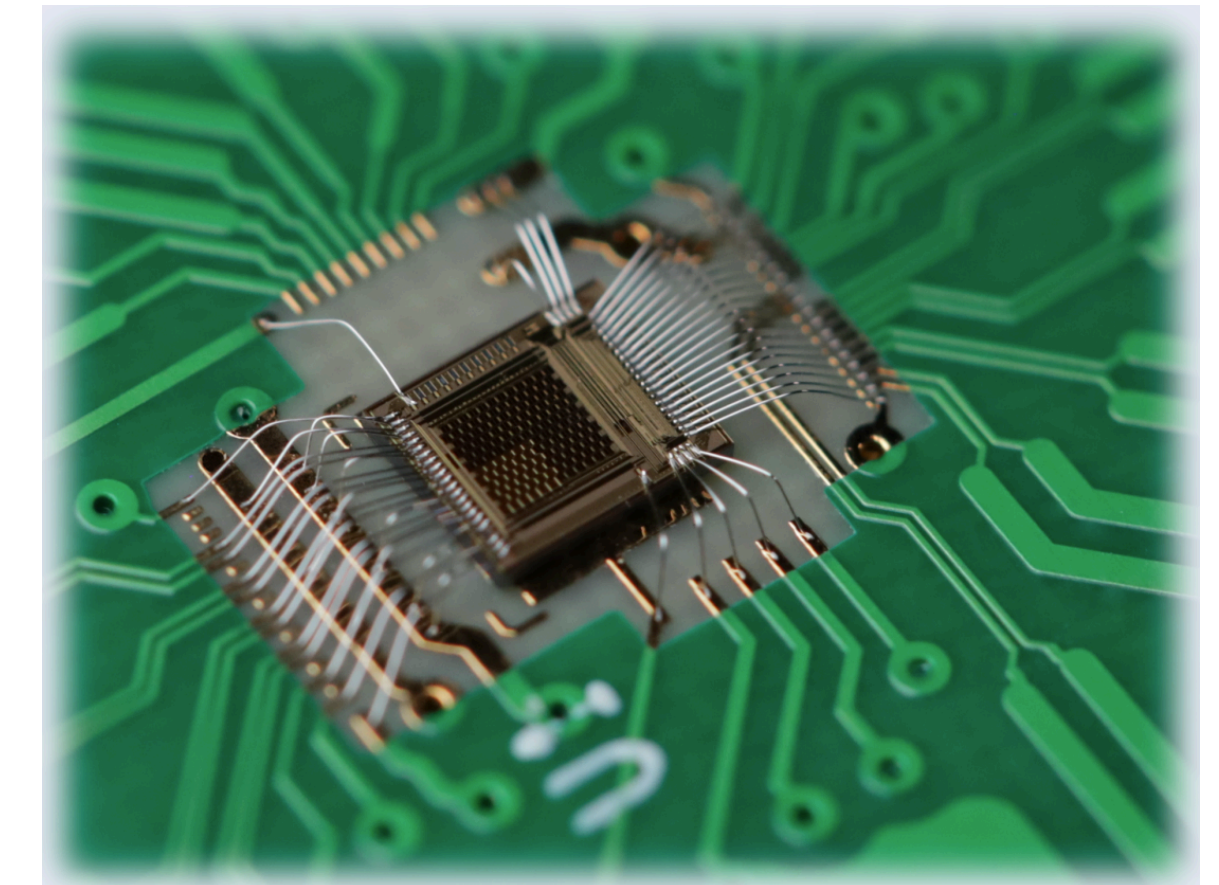
The UniGe monolithic SiGe BiCMOS prototype ASIC provided:

- ▶ Not irradiated: **Efficiency = 99.9%** and **time resolution = 20 ps** limited by Landau noise
- ▶  **$1 \times 10^{16} n_{eq}/cm^2$** : **Efficiency = 99.7%** and **time resolution = 45 ps (200 → 300V)**

This performance was obtained with a 50  $\mu m$  thick sensor

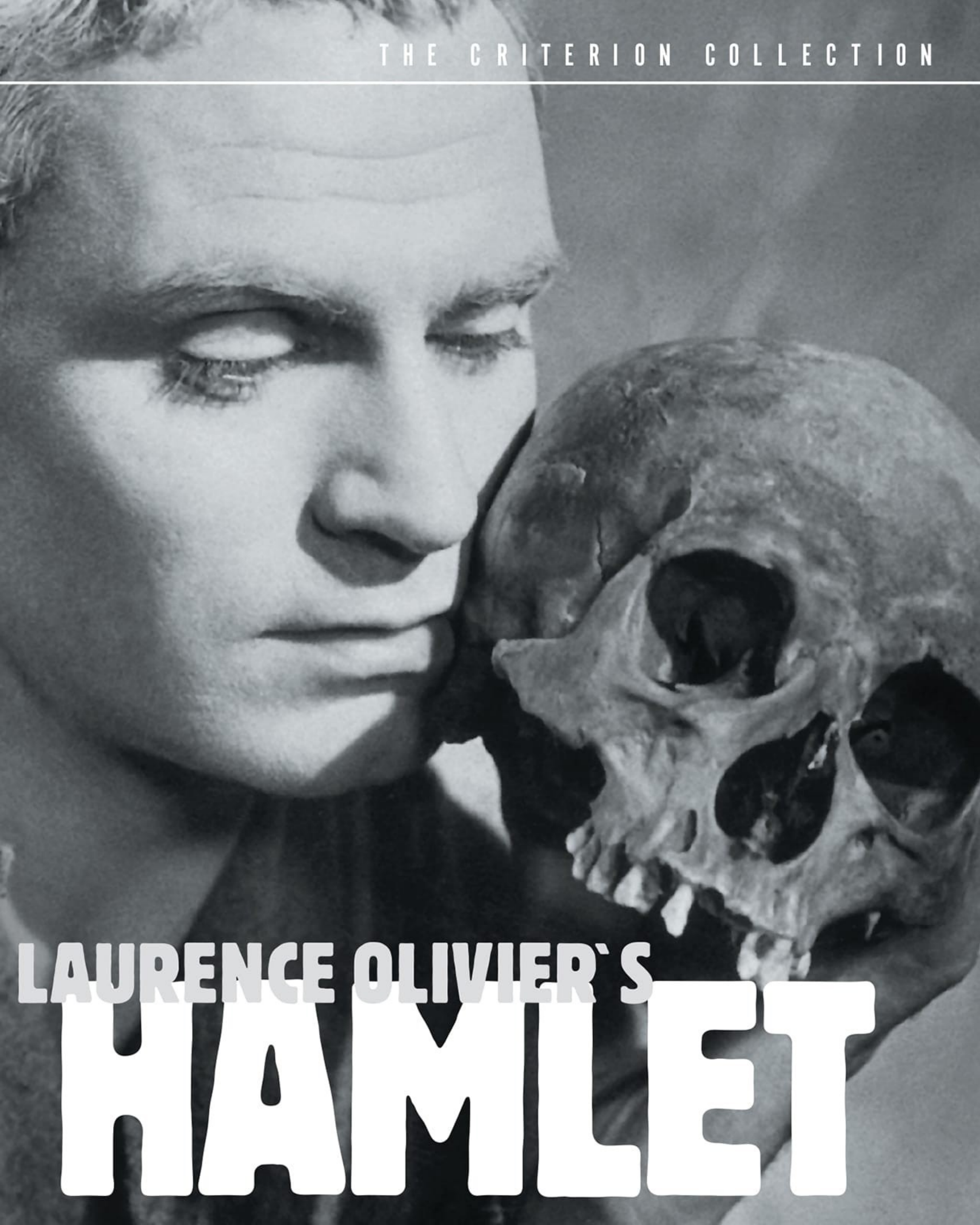
**without gain layer**

**using SiGe HBT electronics**



If the **radiation tolerance of gain layers** remains a concern, particle-physics experiments can do excellent timing **without** gain layer

THE CRITERION COLLECTION



LAURENCE OLIVIER'S  
**HAMLET**

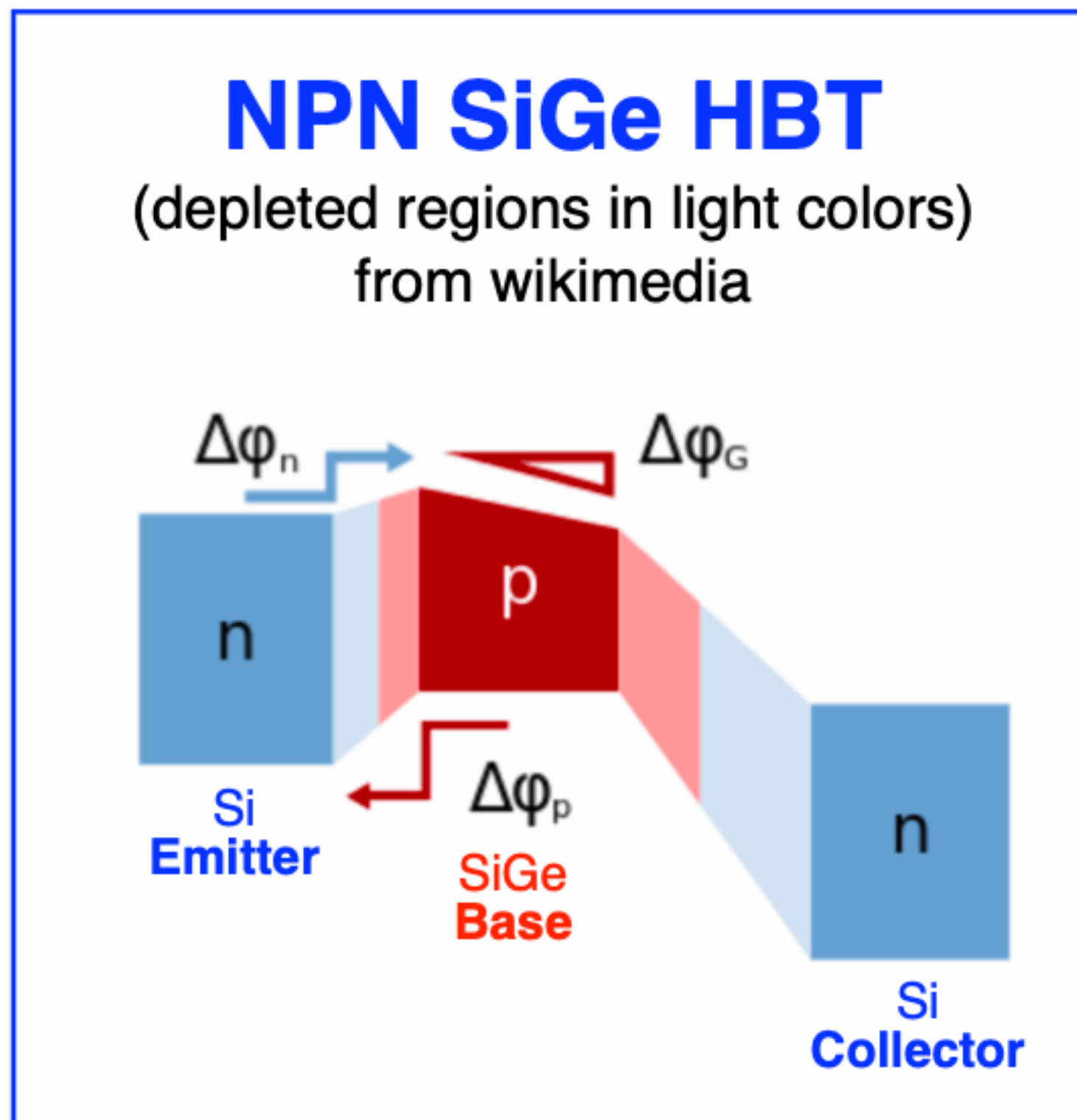
Question # 4:

28 nm CMOS

or

130 nm SiGe BiCMOS





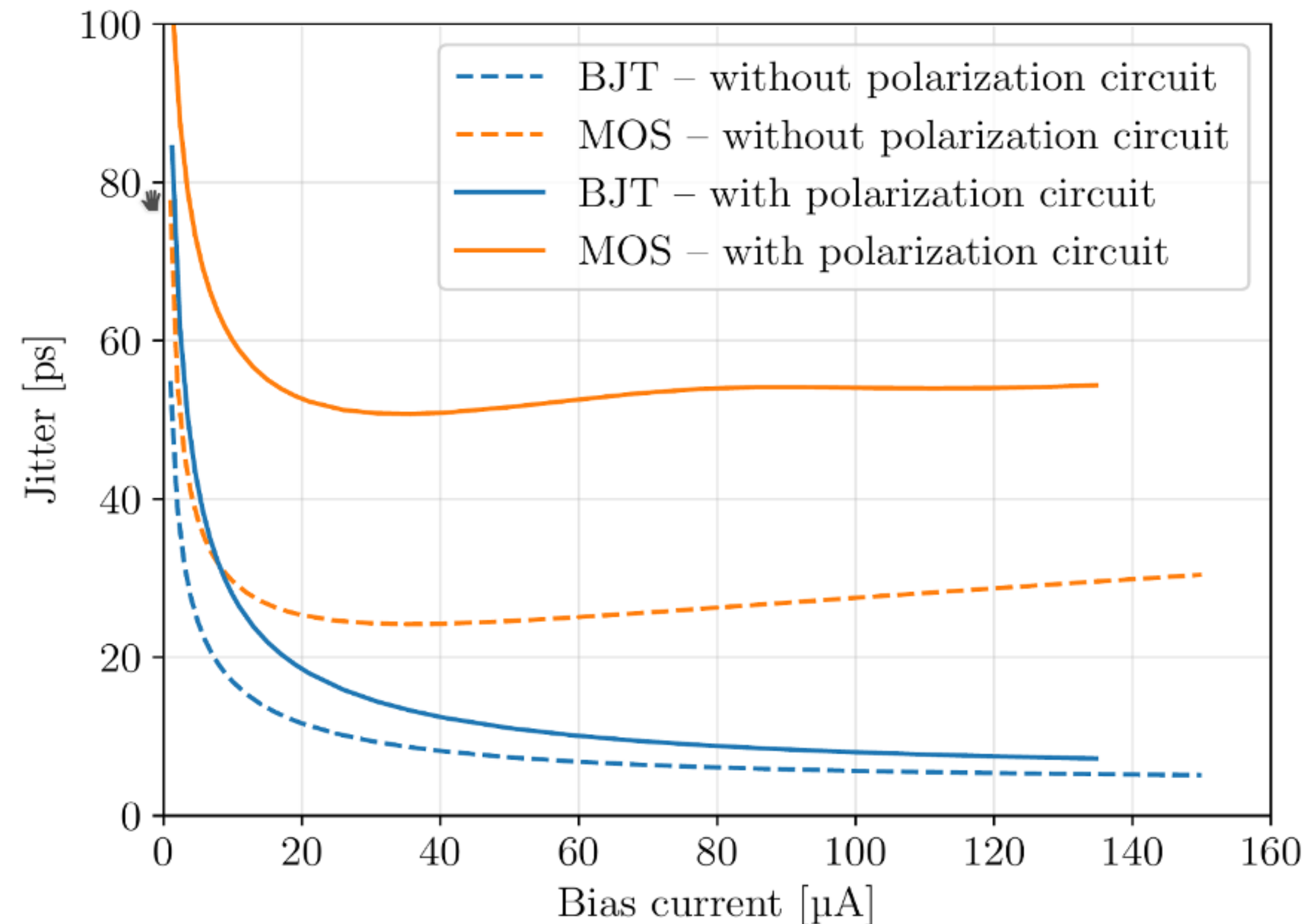
**SiGe HBT = BJT with Germanium as base material.**

**Grading of Ge doping in base:**

- charge-transport in base via **drift**
  - reduced charge-transit-time in base
  - **high current gain  $\beta$**
- **High doping in base is possible:**
  - thinner base
  - **reduced base resistance  $R_b$**

$$ENC_{series\ noise} \propto \sqrt{k_1 \frac{C_{tot}^2}{\beta} + k_2 R_b C_{tot}^2}$$

Intrinsic **amplifier jitter**:  
common emitter (source) configuration  
in a 130nm technology

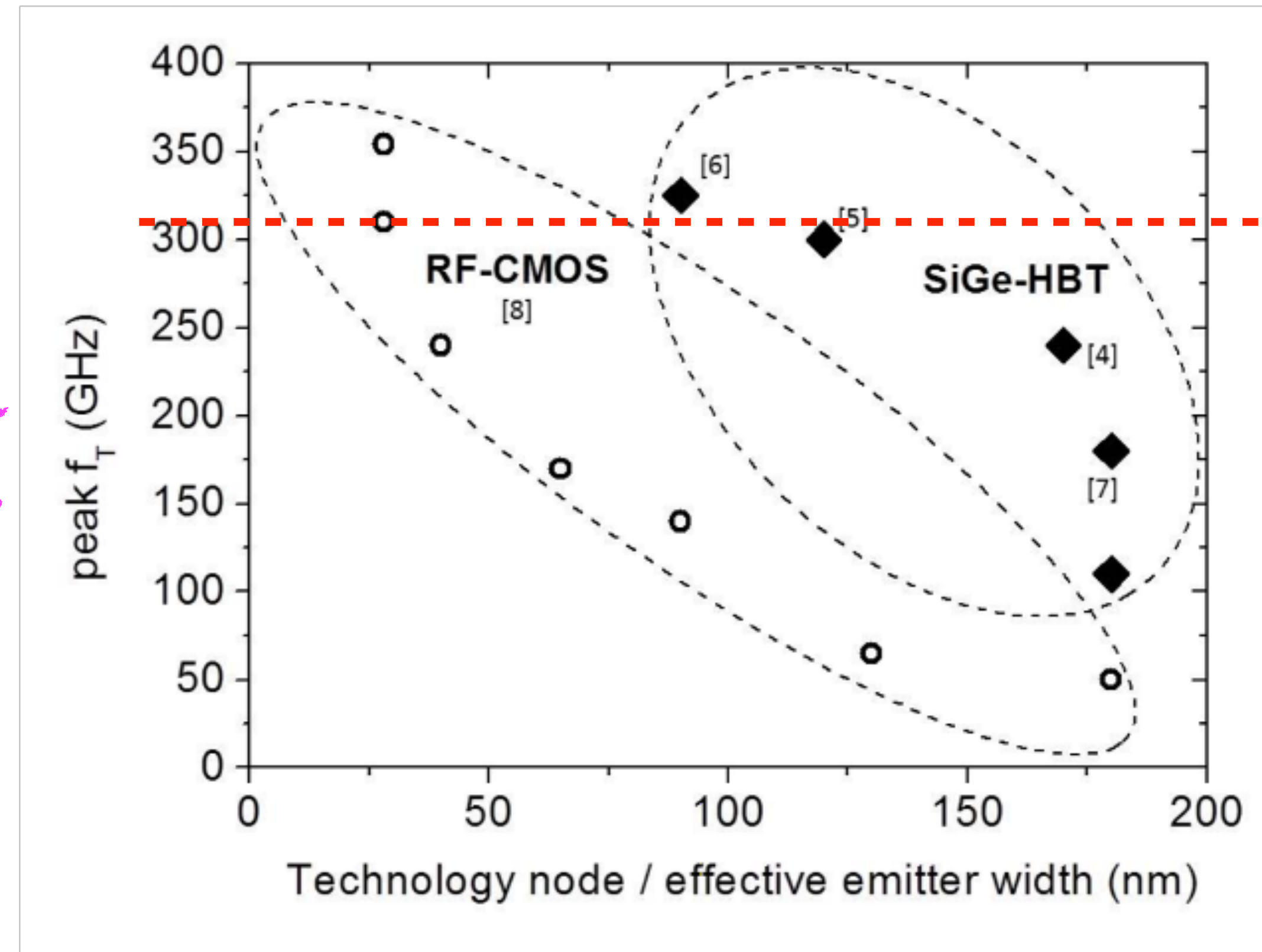


At equal node size,  
SiGe HBT  
has much smaller jitter than  
CMOS

L. Paolozzi et al.,  
Time resolution and power consumption of a monolithic silicon pixel prototype in SiGe BiCMOS technology,  
JINST 15 (2020) P11025, <https://doi.org/10.1088/1748-0221/15/11/P11025>

## Peak transition frequency vs. technology node

signal speed

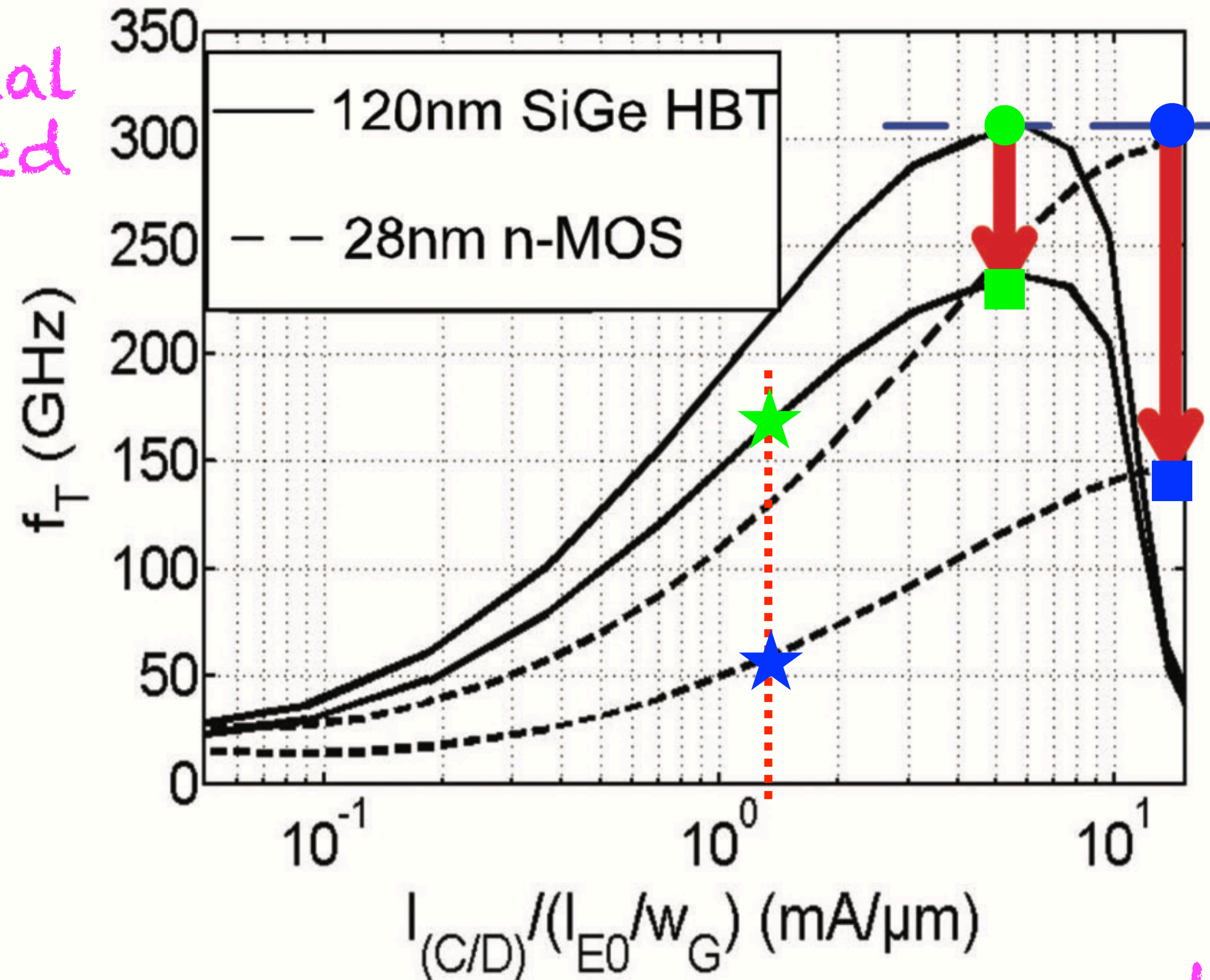


28 nm CMOS  
and  
130 nm SiGe HBT  
have  
same peak  $f_T$

A. Mai and M. Kaynak,  
SiGe-BiCMOS based technology platforms for mm-wave and radar applications.  
DOI: [10.1109/MIKON.2016.7492062](https://doi.org/10.1109/MIKON.2016.7492062)



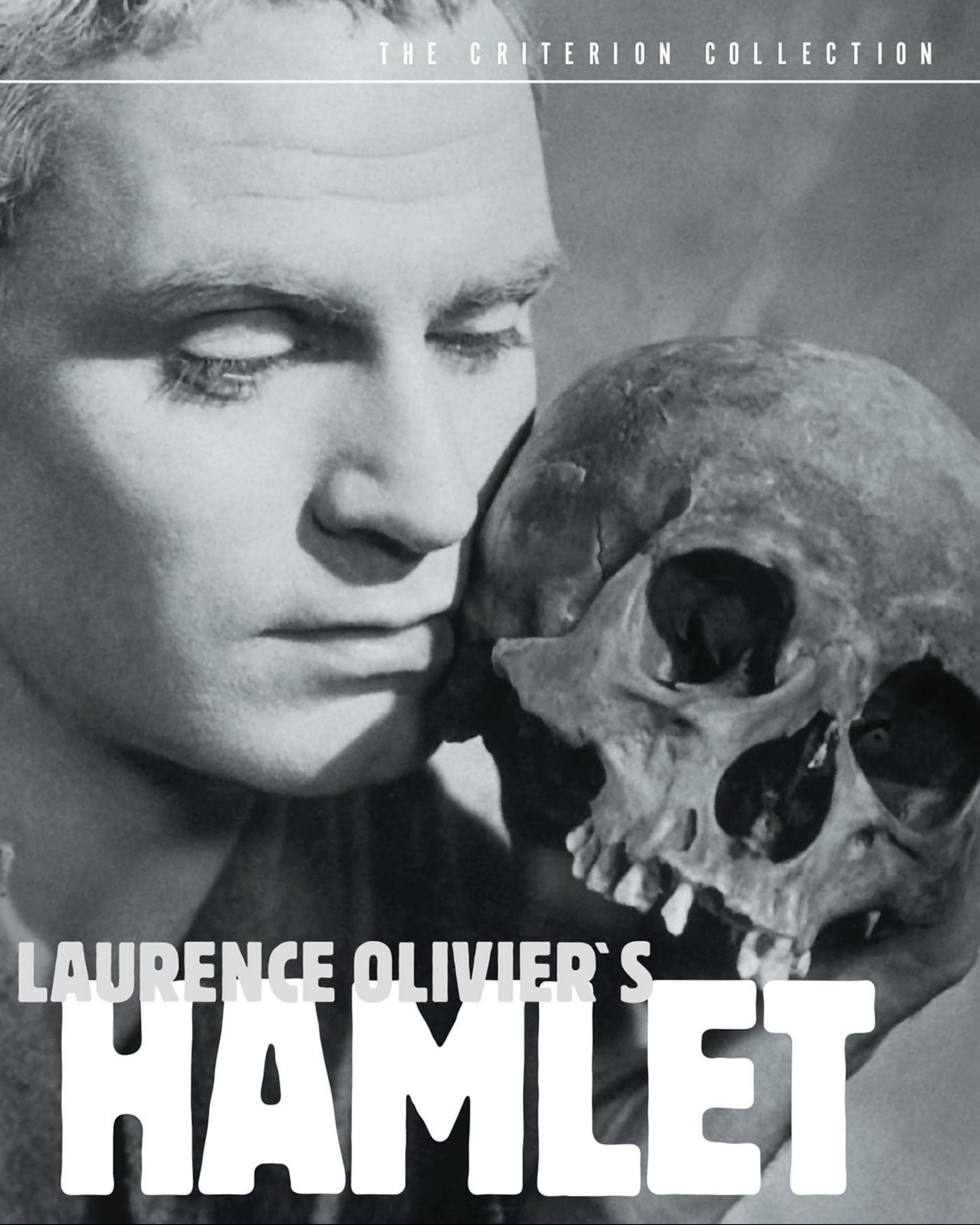
<https://doi.org/10.13052/rp-9788793519602>, March 2018, page 311



- at peak  $f_T$  (without a load): three times less power for same timing
- at peak  $f_T$ , if you put a load: three times less power for twice better timing
- at equal (lower) power: SiGe HBT  $\approx$  3 times faster (**but** size of CMOS transistors would become **prohibitively large**)

CMOS-transistor size

THE CRITERION COLLECTION



LAURENCE OLIVIER'S  
**HAMLET**

**Hamlet,**  
for best timing,  
you better chose SiGe.

At UniGe, we have no doubt.

Markets served  
by SiGe BiCMOS:



Optical fiber  
networks



Smartphones



IoT Devices



Microwave  
Communication



Automotive:  
LiDAR, Radar and  
Ethernet



HDD preamplifiers,  
line drivers, Ultra-high  
speed DAC/ADCS

source: <https://towerjazz.com/technology/rf-and-hpa/sige-bicmos-platform/>

Several large-volume foundries offer SiGe processes:

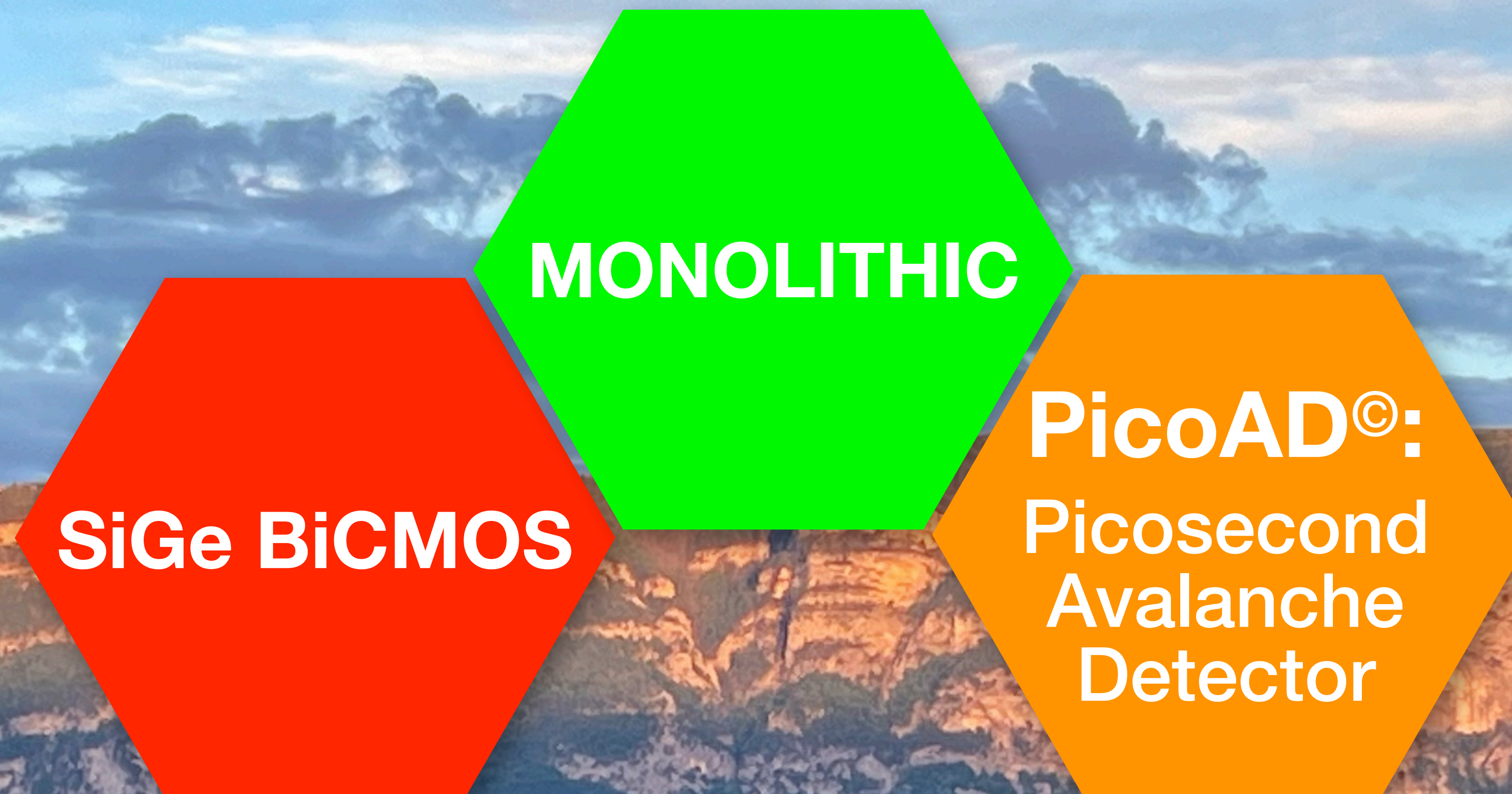


, ...

## Fast growing technology:

1. new IHP process SG13G3Cu, now available through **EUROPRACTICE**, includes transistor with  $f_T/f_{max} = 500/700$  GHz ( $f_T/f_{max} = 350/450$  GHz for SG13G2 process)
2. **ST Microelectronics** offers a **55nm** process, with HBT with  $f_T/f_{Tmax} = 320/370$  GHz

# The **MONOLITH** Project



Results with **PicoAD** prototypes (with gain layer)

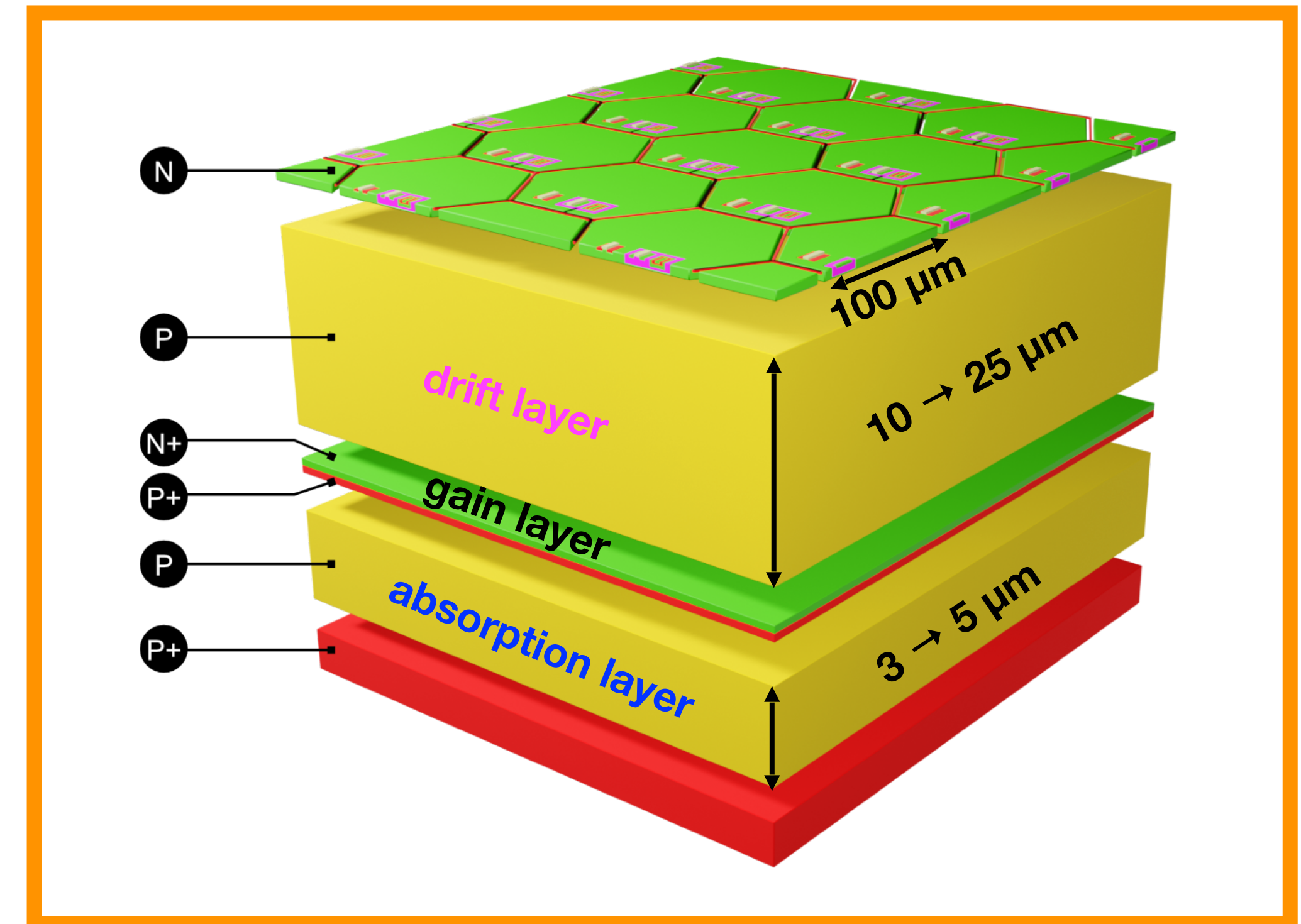
## PicoAD:

### Multi-Junction Picosecond-Avalanche Detector©

with continuous and deep gain layer:

- De-correlation from implant size & geometry  
→ **high pixel granularity and full fill factor**  
(to get homogeneous efficiency and timing)
- Only the small fraction of charge produced in the thin **“absorption layer”** gets amplified  
→ **reduced charge-collection (Landau) noise**  
(to enhance timing resolution, like a very thin LGAD)
- Landau noise of initial part of the signal is minimal  
→ **keep threshold low** (to enhance timing resolution)

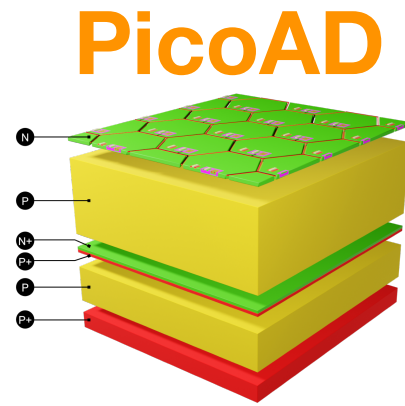
© G. Iacobucci, L. Paolozzi and P. Valerio. Multi-junction pico-avalanche detector;  
**European Patent** EP3654376A1, **US Patent** US2021280734A1, Nov 2018



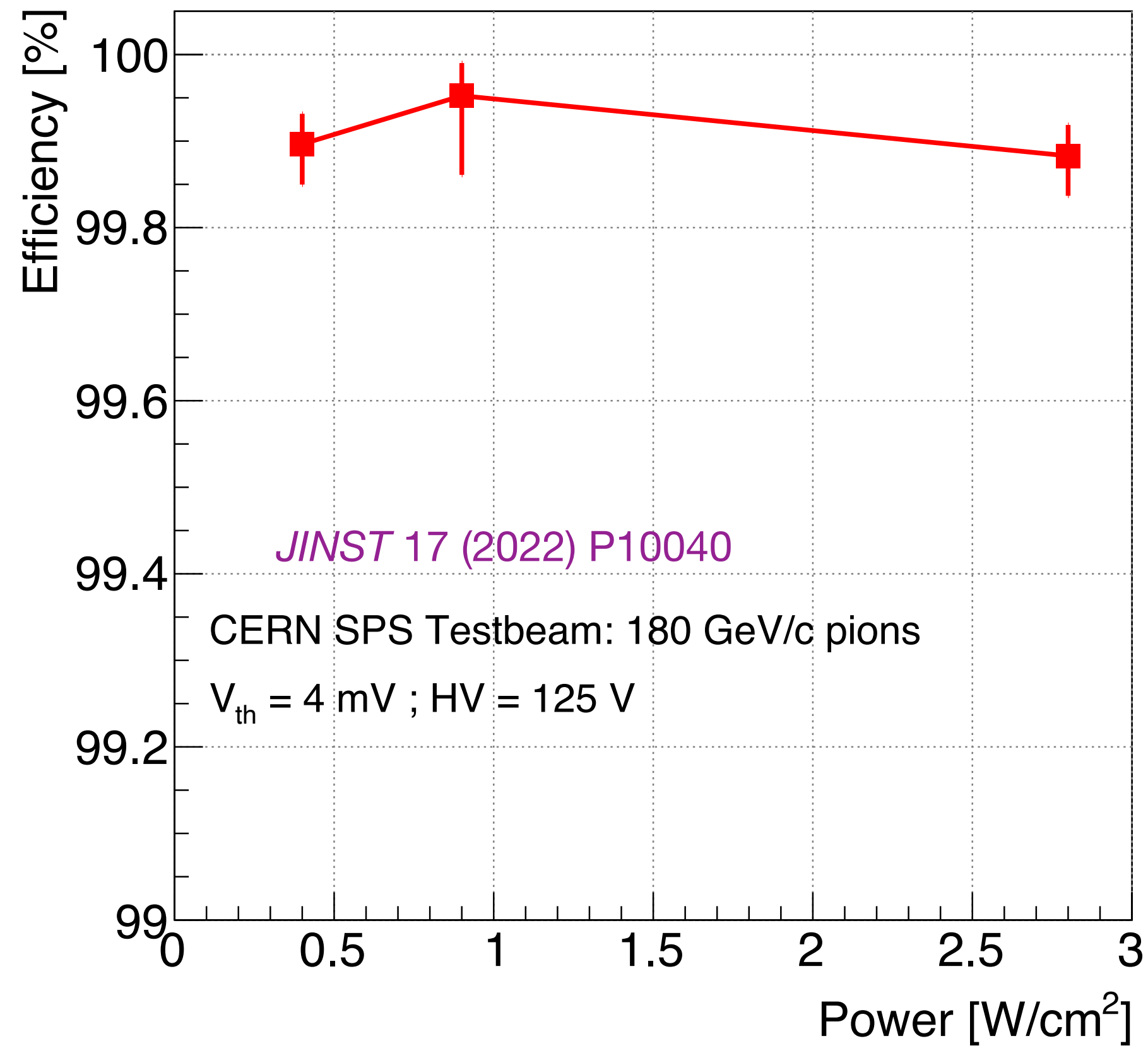
Monolithic PicoAD **proof-of-concept** ASIC produced in 2022 →

**99.9% for all power consumptions**

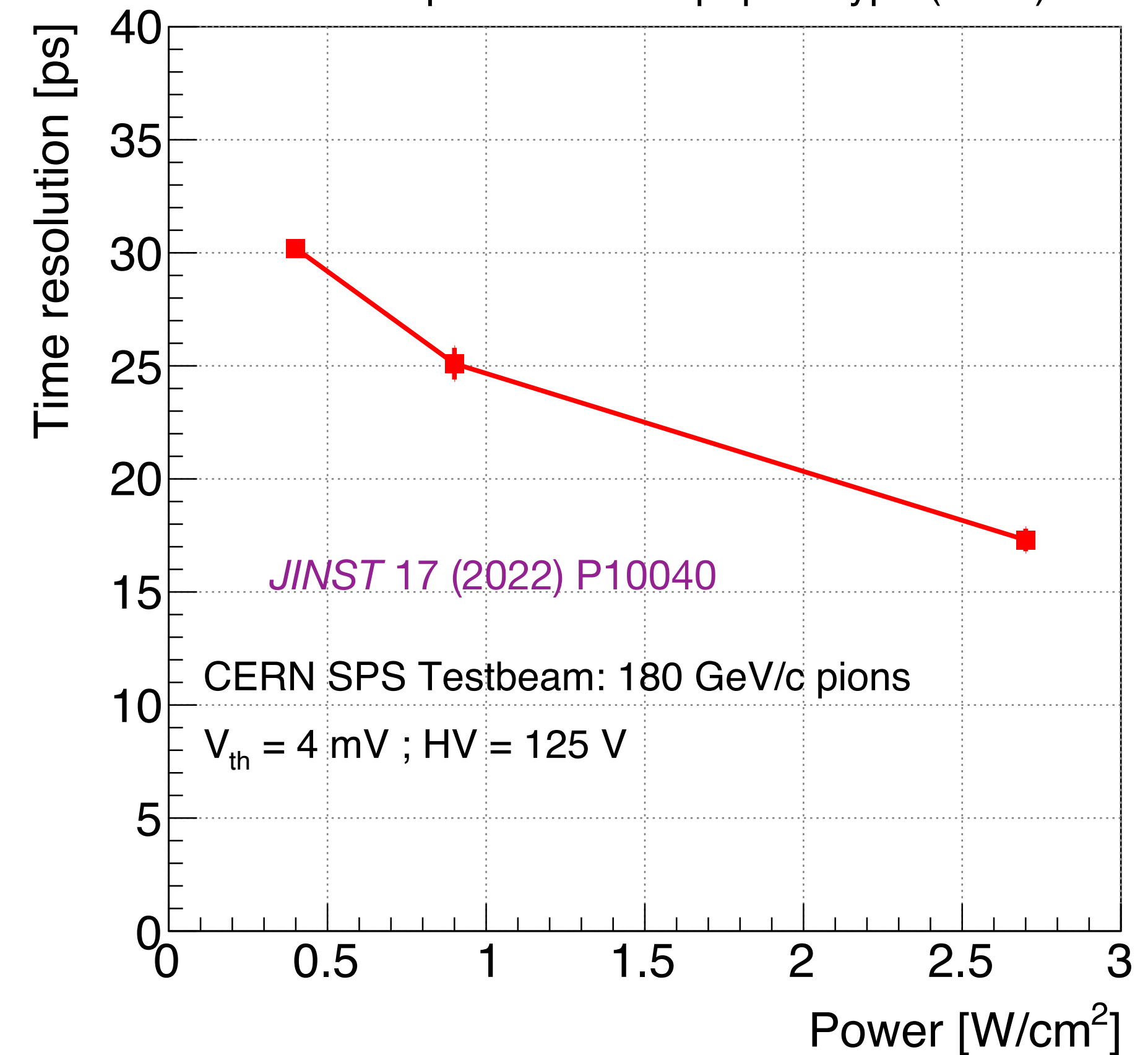
**30 ps at 0.4 W/cm<sup>2</sup>**  
**17 ps at 2.7 W/cm<sup>2</sup>**



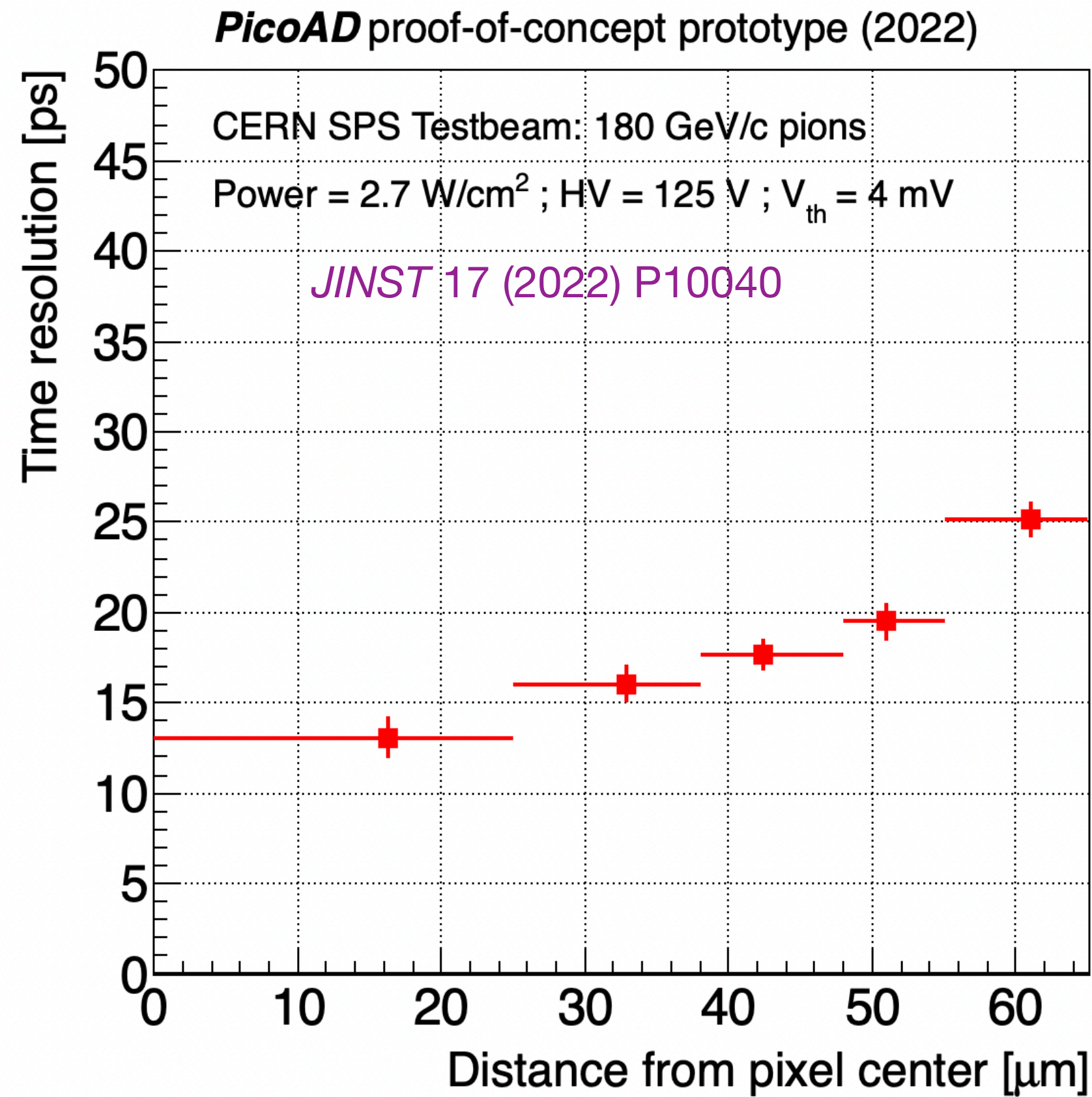
*PicoAD* proof-of-concept prototype (2022)



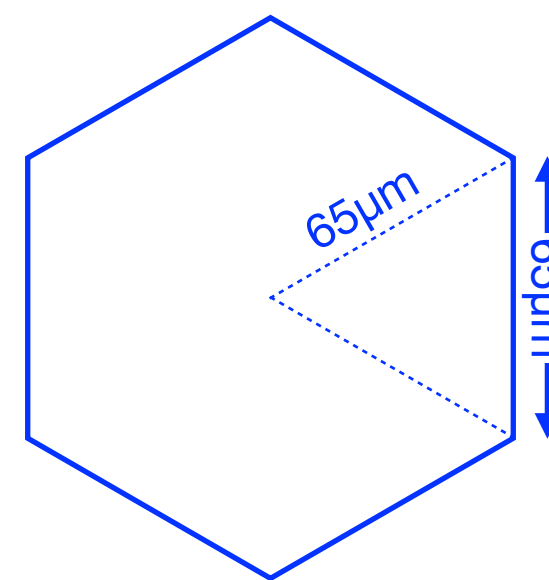
*PicoAD* proof-of-concept prototype (2022)



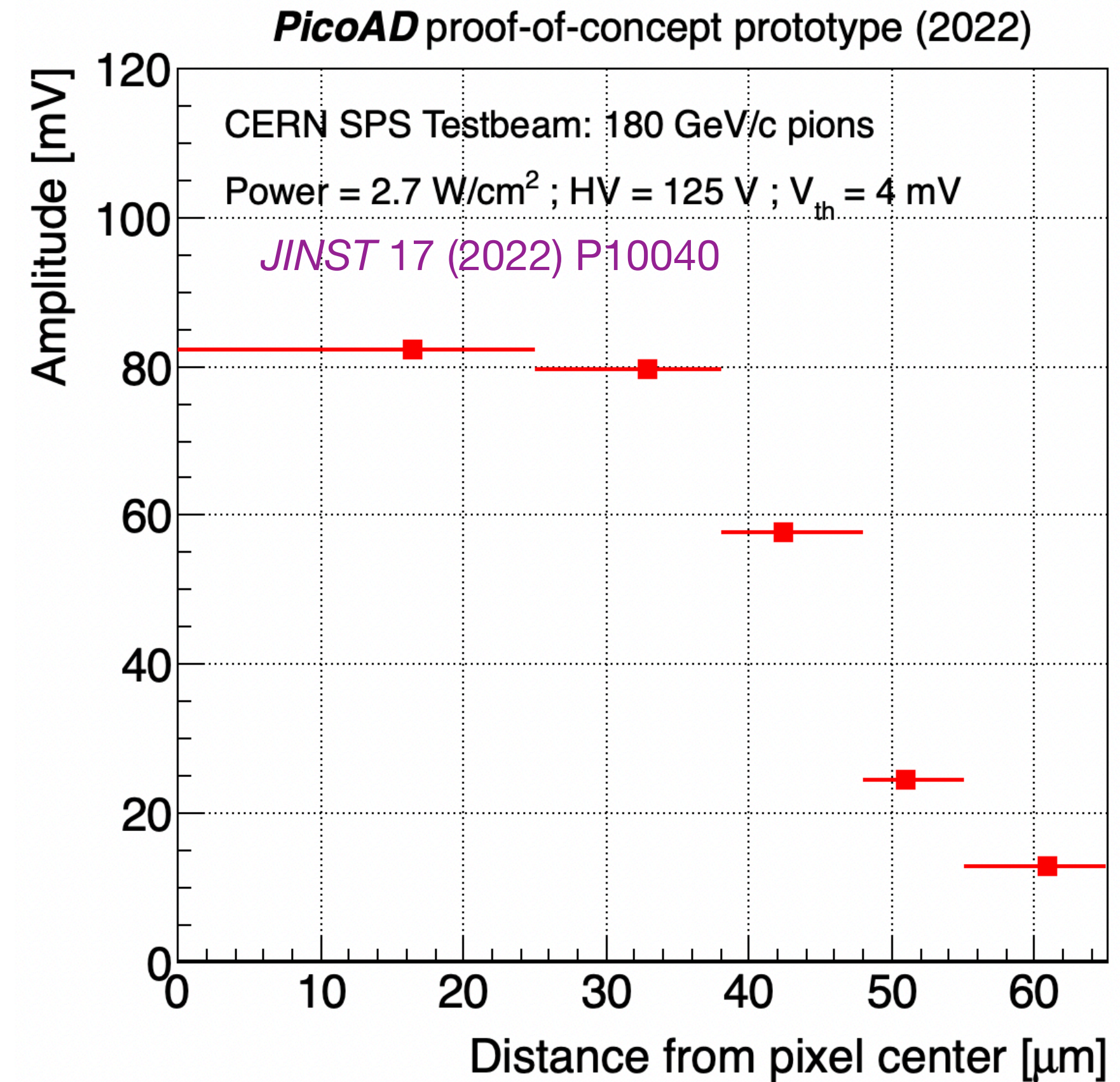
## Time resolution



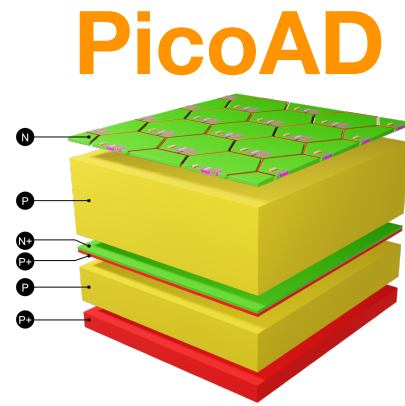
**13 ps** at the pixel center  
**25 ps** at the pixel edge



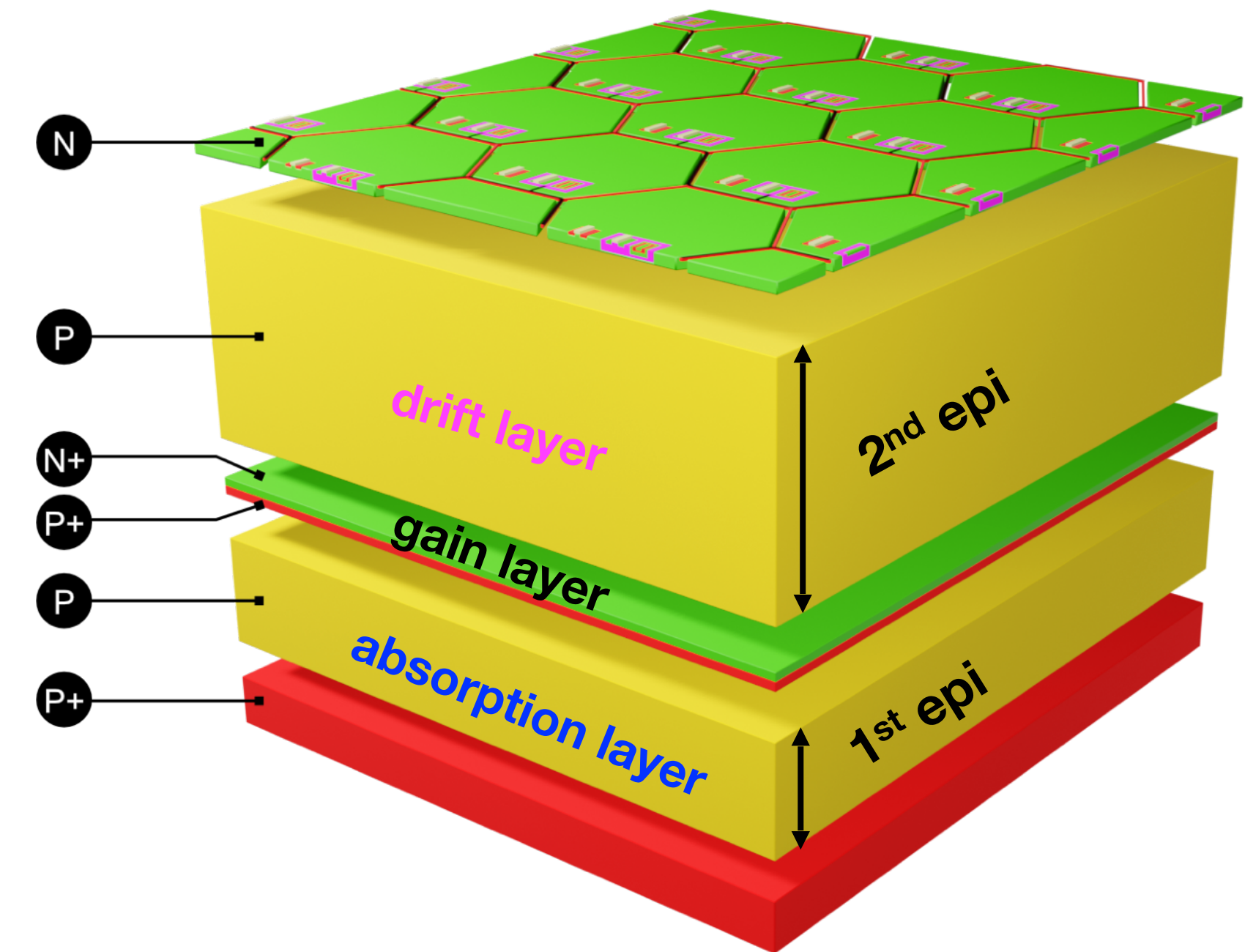
## Signal MPV amplitude



strong decrease of signal amplitudes  
at the edge of the pixel. **Problem to solve.**  
New prototypes devised to improve this dependence



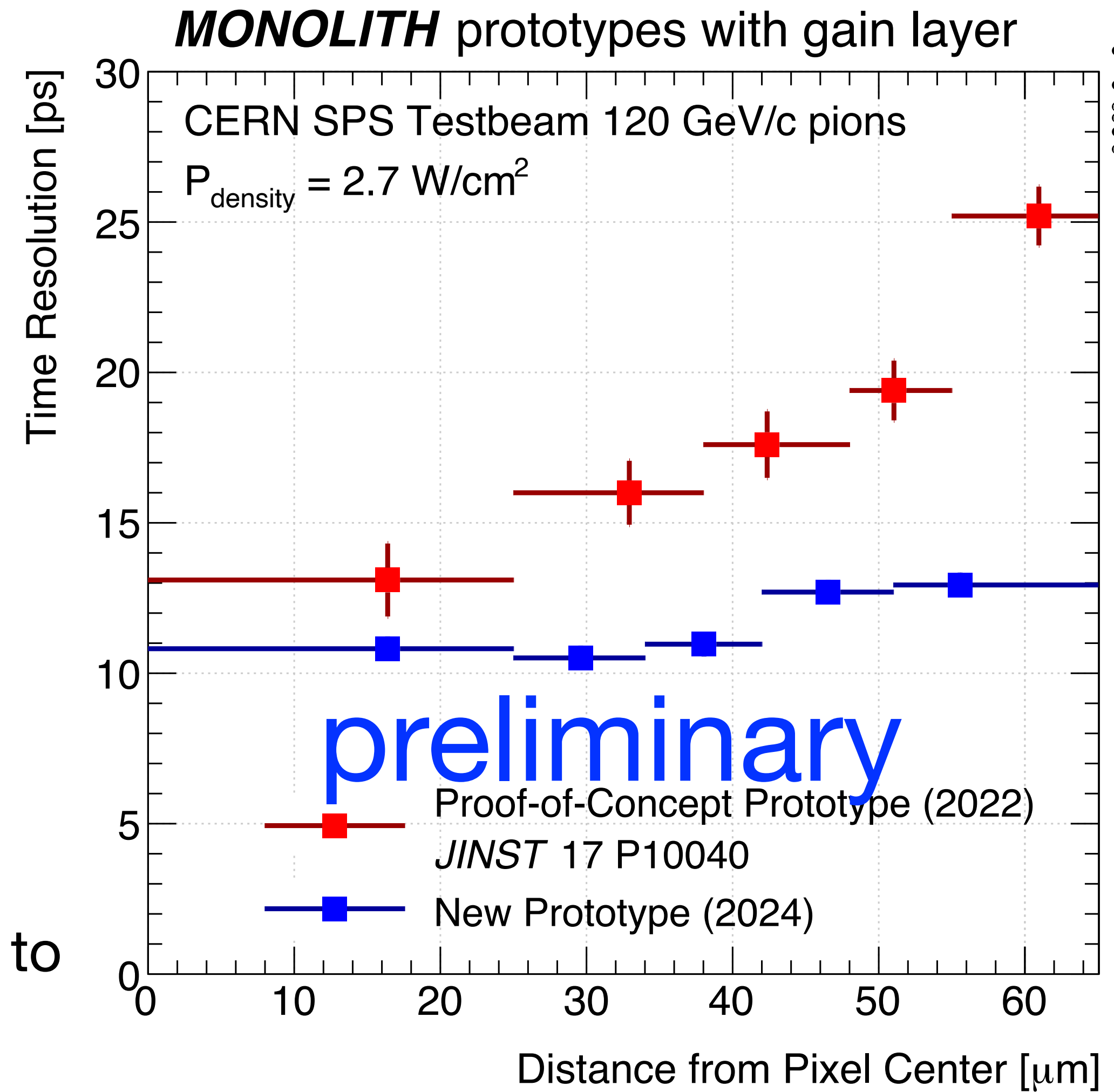
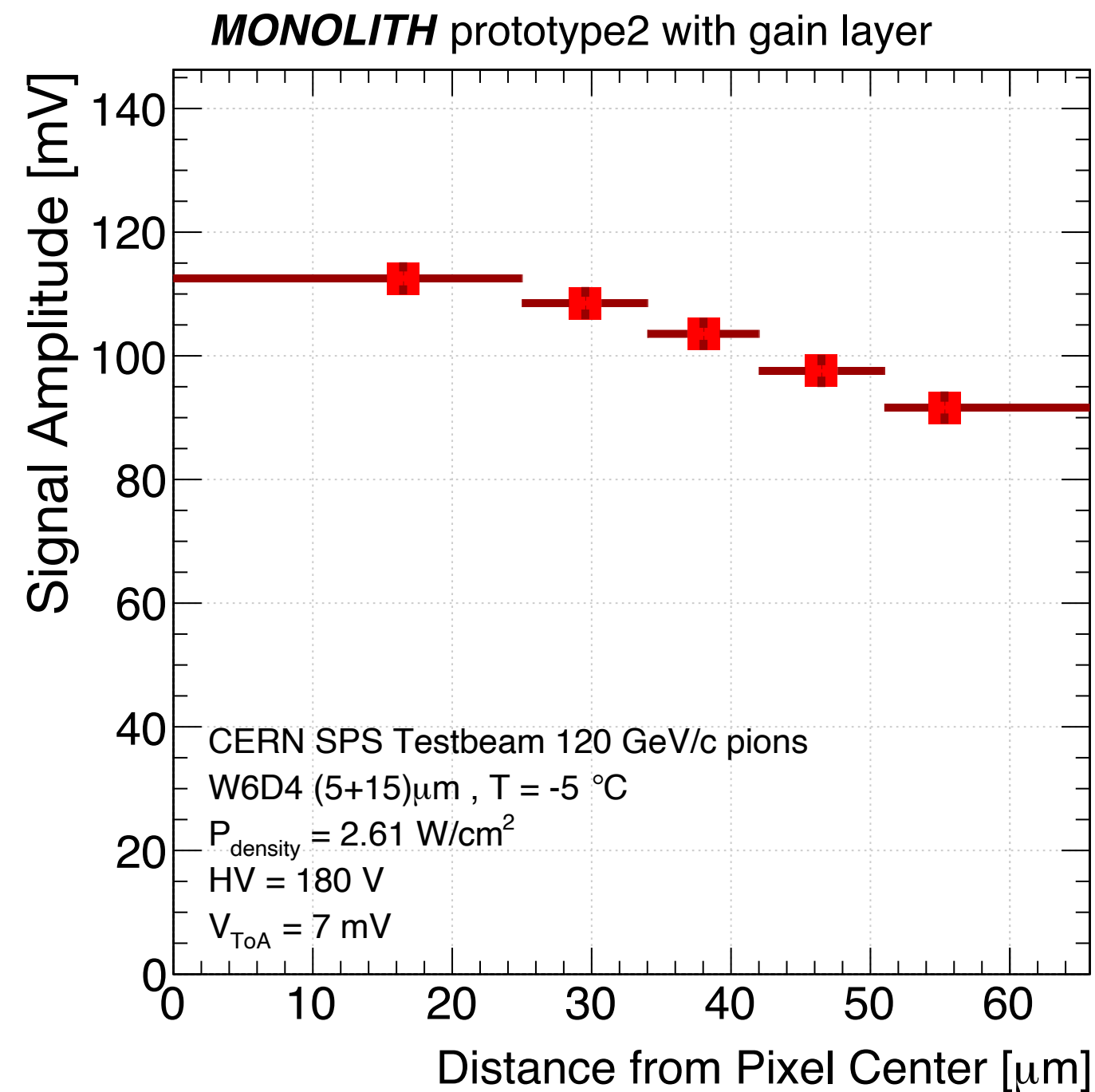
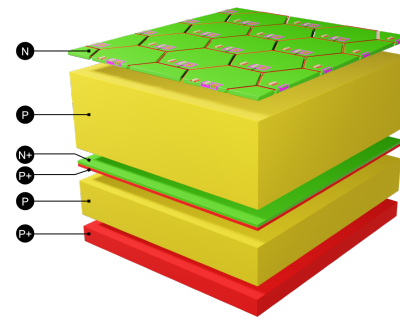
Wafer	1 <sup>st</sup> epi thickness [ $\mu\text{m}$ ]	2 <sup>nd</sup> epi thickness [ $\mu\text{m}$ ]	Gain-layer implant dose
3	3	15	3
			3.5
			4
4	3	25	3.5a
			3.5b
			4.75
5	3	25	4
			4.5
			5
6	5	15	3
			3.5
			4
7	5	25	4
			4.5
			5



15 different flavours produced;  
in 4 geometries.

Some of them presently at CERN testbeam.

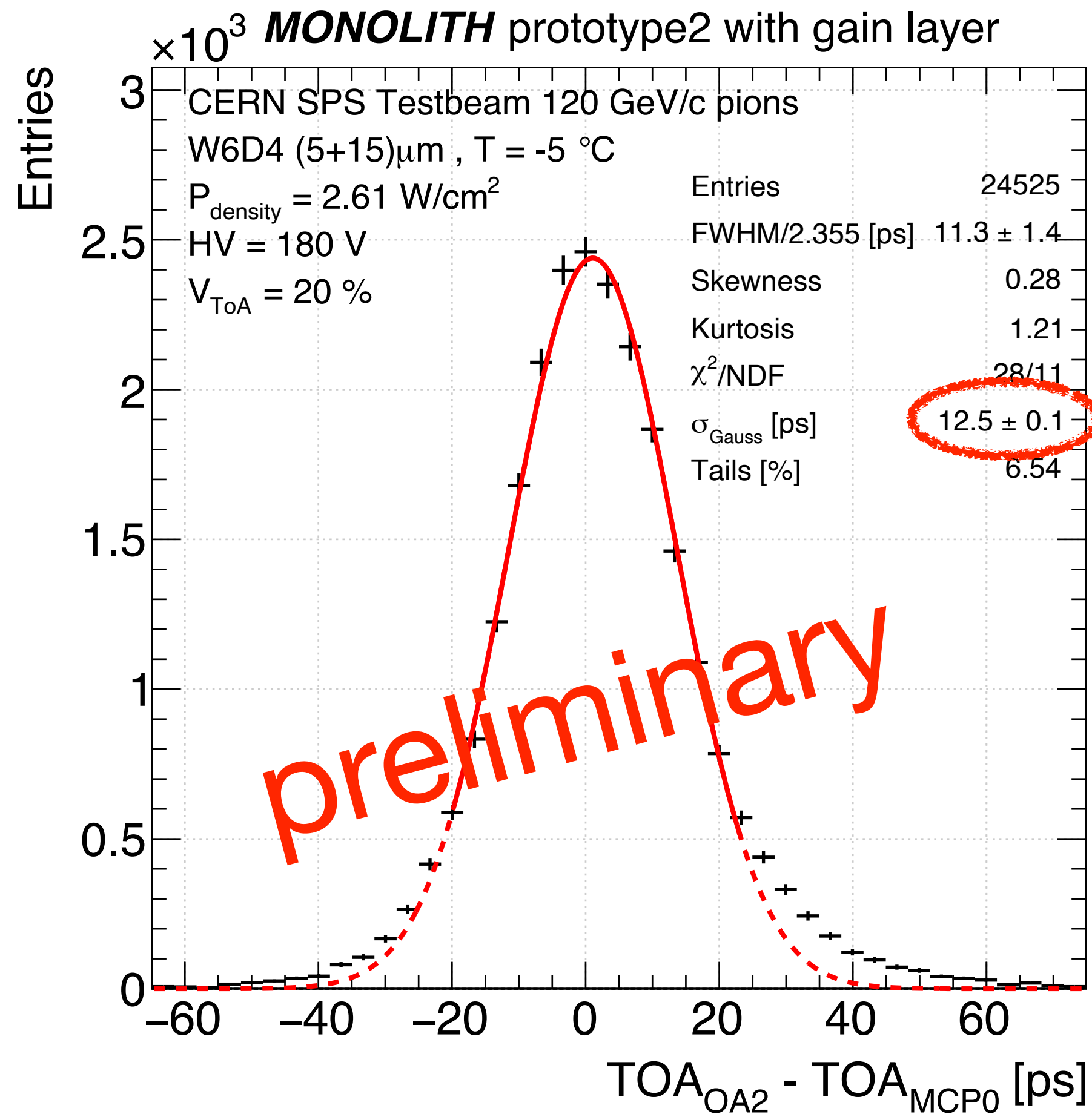




Much improved uniformity of the electric field due to

1. larger “drift” epilayer (10  $\rightarrow$  15  $\mu\text{m}$ )
2. larger resistivity (50  $\rightarrow$  350  $\Omega\text{cm}$ ).

produced an avalanche detector that gains everywhere.



Preliminary full offline analysis  
for one working point gives :

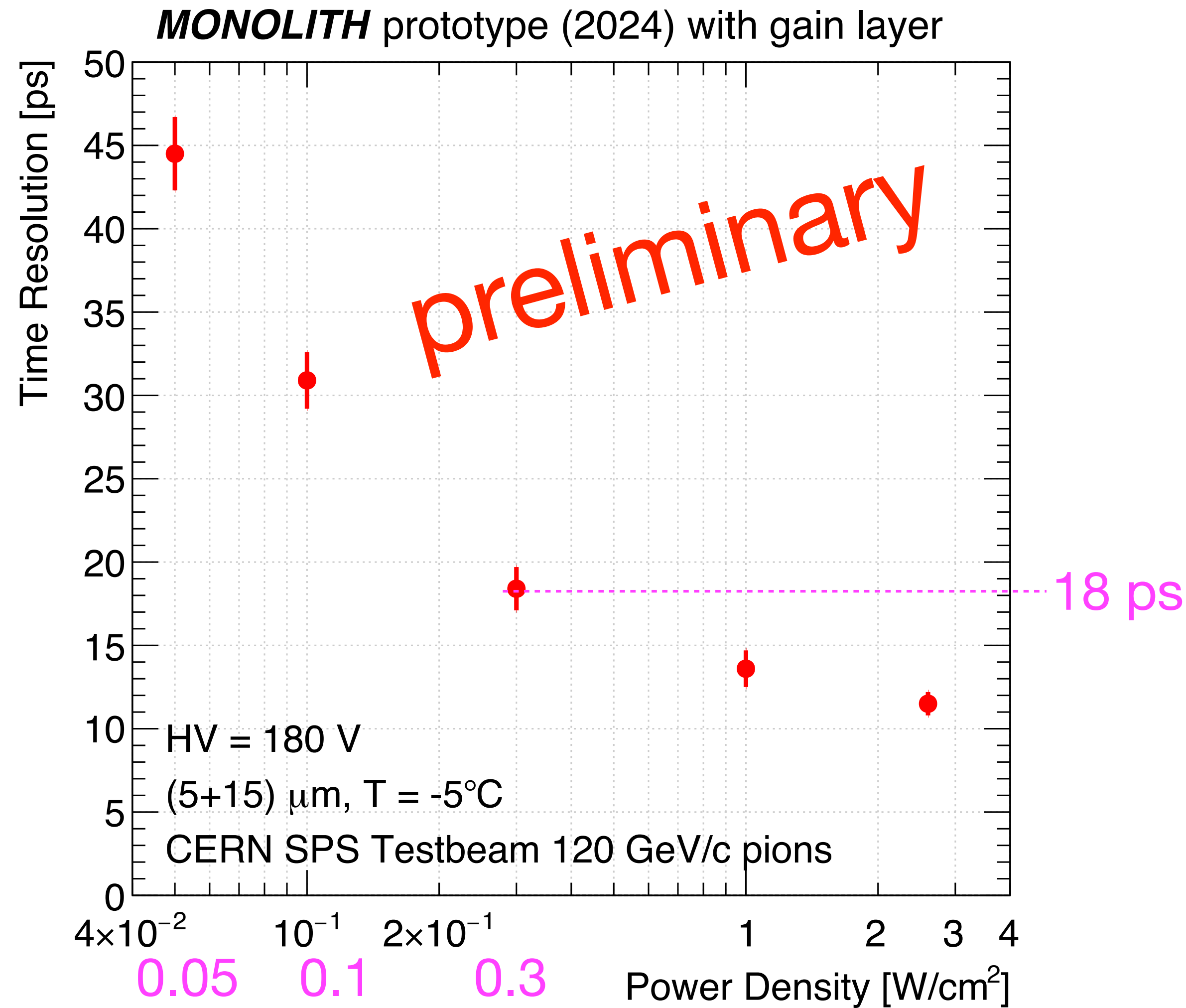
$$\text{ToA}_{\text{PicoAD}} - \text{ToA}_{\text{MCP}} = \mathbf{12.5 \text{ ps}}$$

Subtraction in quadrature of MCP contribution

$$\sigma_t = \sqrt{12.5^2 - 4.9^2} = 11.5 \text{ ps}$$

MCP resolution

(it was 17 ps with the proof-of-concept prototype)



18 ps achieved at 0.3  $\text{W}/\text{cm}^2$

The **PicoAD<sup>©</sup>** sensor works *(JINST 17 (2022) 10 P10032 ; JINST 17 (2022) 17 P10040)*

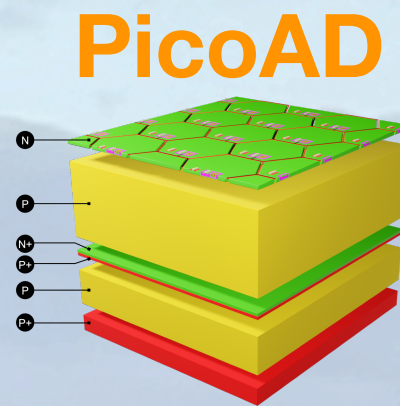
Testbeam of the monolithic ASIC provided:

- ▶ **Efficiency = 99.9 %** including inter-pixel regions
- ▶ **Time resolution  $\sigma_t = 11.5$  ps**

Measurements still going on.

We produced a **fully efficient** avalanche detector with **homogeneous gain everywhere**

Although the UNIGE research programme concentrated so far on monolithic detectors, **standalone PicoAD sensors** can be produced to be hybridised on a readout ASIC (discussions started with a manufacturer leader in the field of silicon sensors)



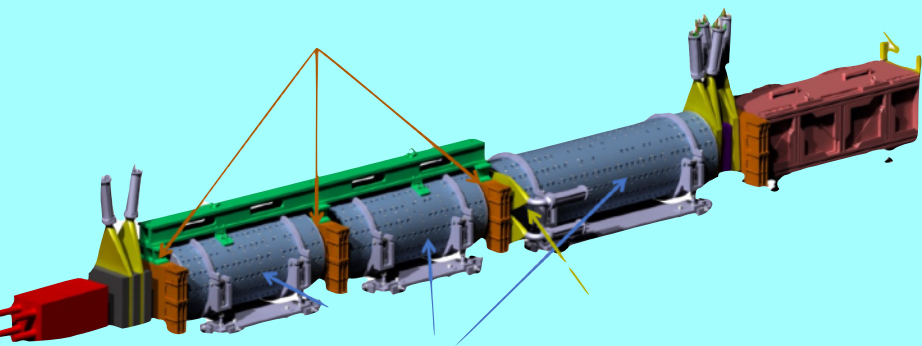


# UniGe monolithic SiGe BiCMOS ASICs



European Research Council  
Established by the European Commission


**FASER** experiment: **W-Si high-resolution pre-shower**



2022 **JINST 16 P12038**

2023 pre-production ASIC (full column)

2024 **FASER production ASIC**



future possibilities

high-radiation tolerance  
high granularity  
timing layers  
for **particle physics**

**Timing prototypes (no gain layer):**

2016 **200ps** *JINST 13 P02015*

2018 **50ps** *JINST 14 P11008*  
*JINST 15 P11025*

2020 **36 ps** *JINST 17 P02019*

2022 **20 ps** *JINST 18 P03047* *JINST 19 P04029*  
*JINST 19 P01014* *arXIV:2404.12885*

**without gain layer**

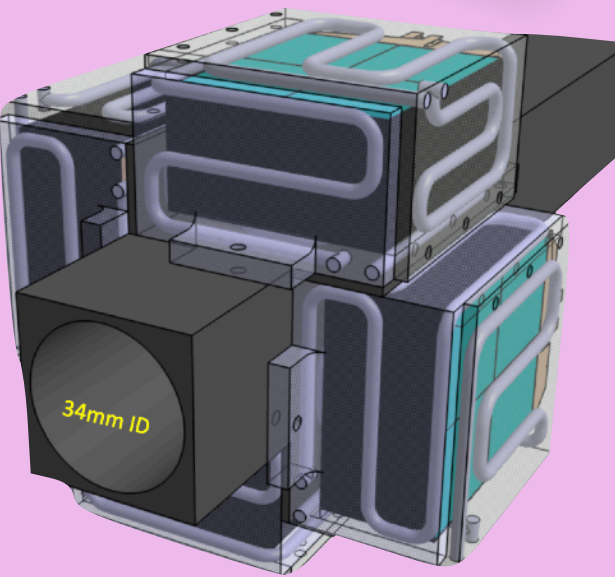
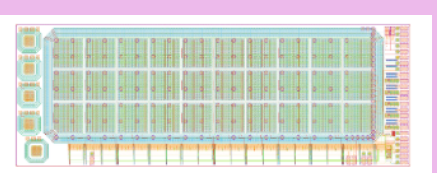

prototypes production is now complete

moderate radiation level  
extremely thin  
timing layers,  
e.g. **mu3e experiment**  
(Lorenzo Paolozzi)

**Medical: TT-PET and 100μPET projects**

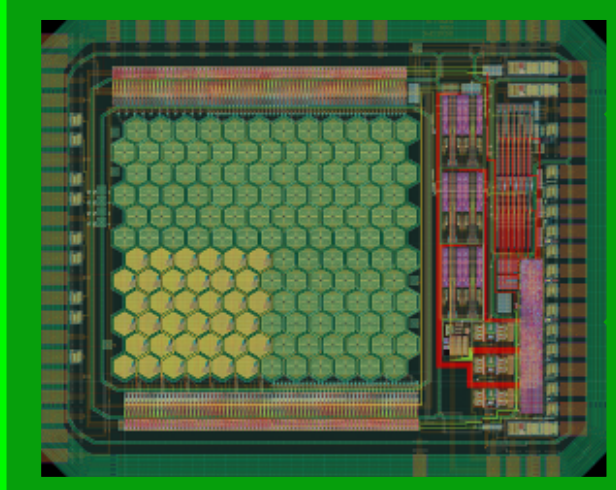
2017 **110ps** *JINST 14 P02009*  
*JINST 14 P07013*

2024 **100μPET production ASIC full reticle**

**PicoAD<sup>©</sup> (gain layer)**

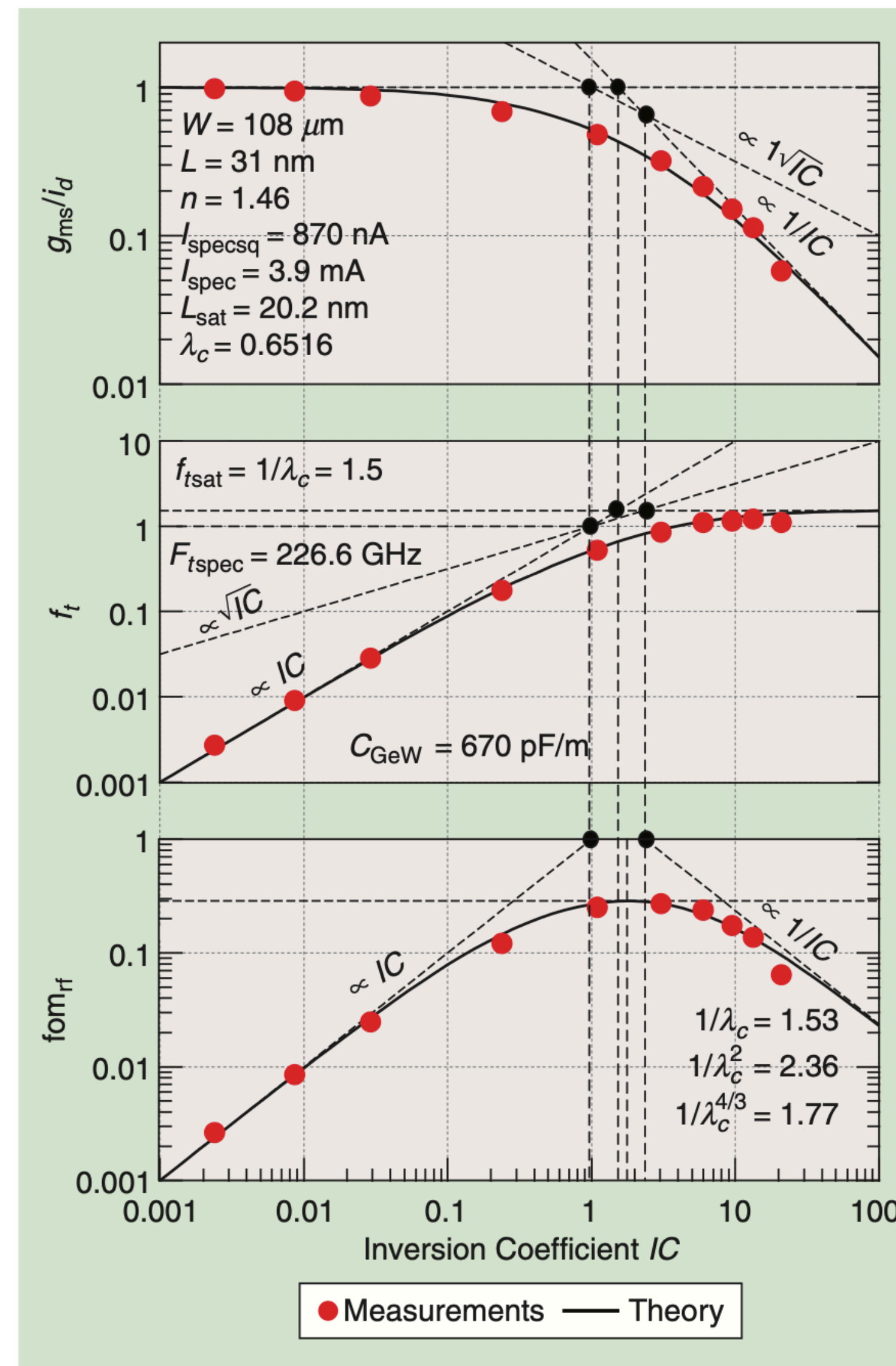
**12 ps** *JINST 17 P10032*  
*JINST 17 P10040*  
+ paper in preparation



**photonics**  
(Thanushan Kugathasan)  
(Roberto Cardella)

**Extra Material**

C. Enz, et al., "Nanoscale MOSFET Modeling",  
*IEEE Solid-State Circuits Magazine*, vol. 9, no. 4, pp. 73-81, 2017,  
doi: 10.1109/MSSC.2017.2745838



**FIGURE 12:**  $g_{ms}/i_d$ ,  $f_t$  and  $fom_{rf}$  versus  $IC$  for a 30-nm device [12].

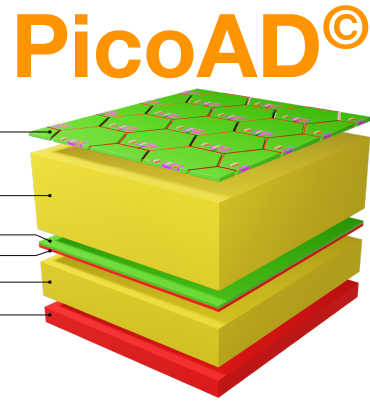
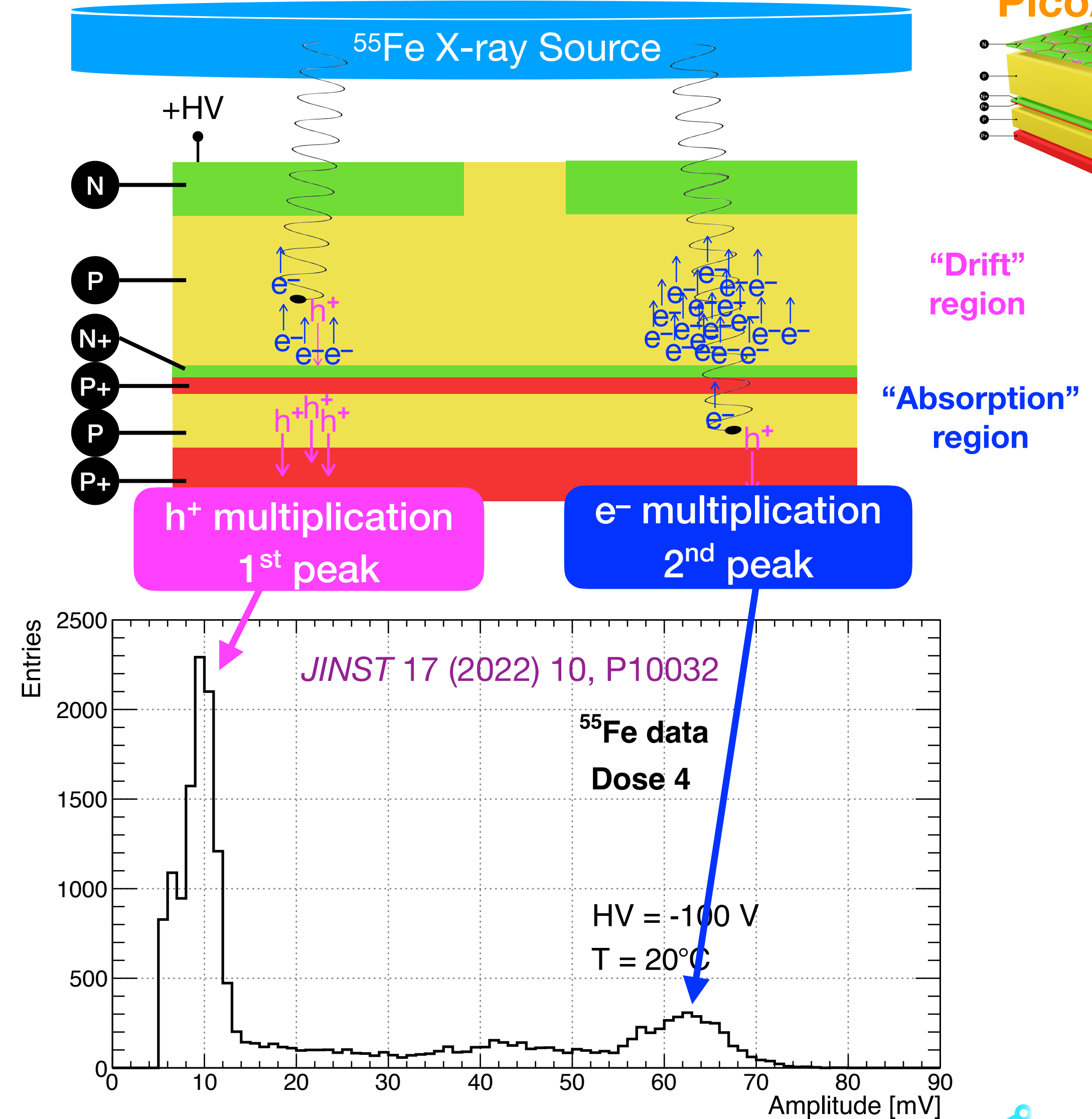
## X-rays from $^{55}\text{Fe}$ radioactive source:

- ▶ mainly  $\sim 5.9$  keV photons
- ▶ point-like charge deposition

## We found a **double-peak spectrum**

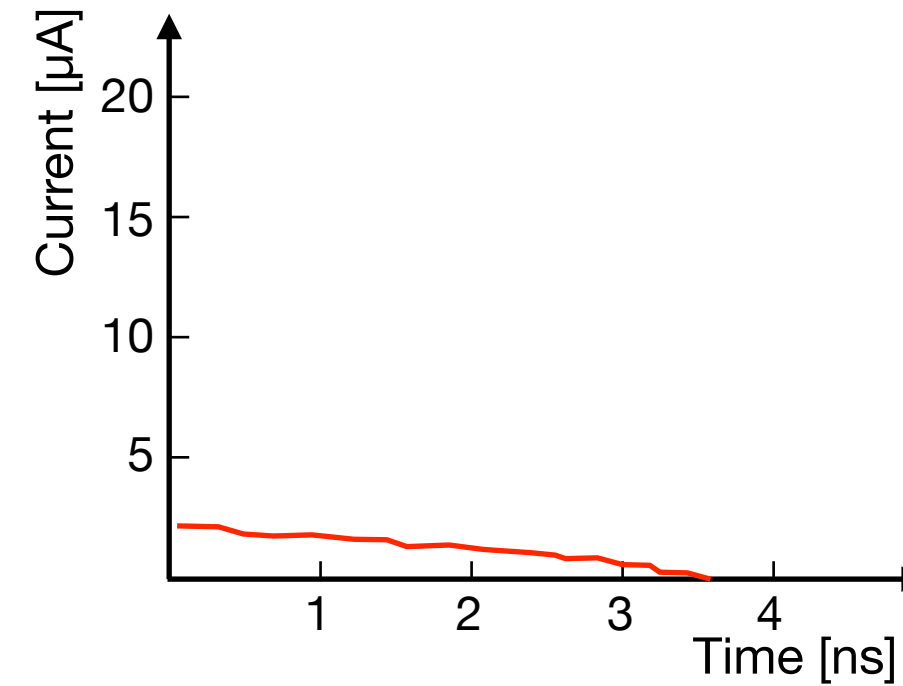
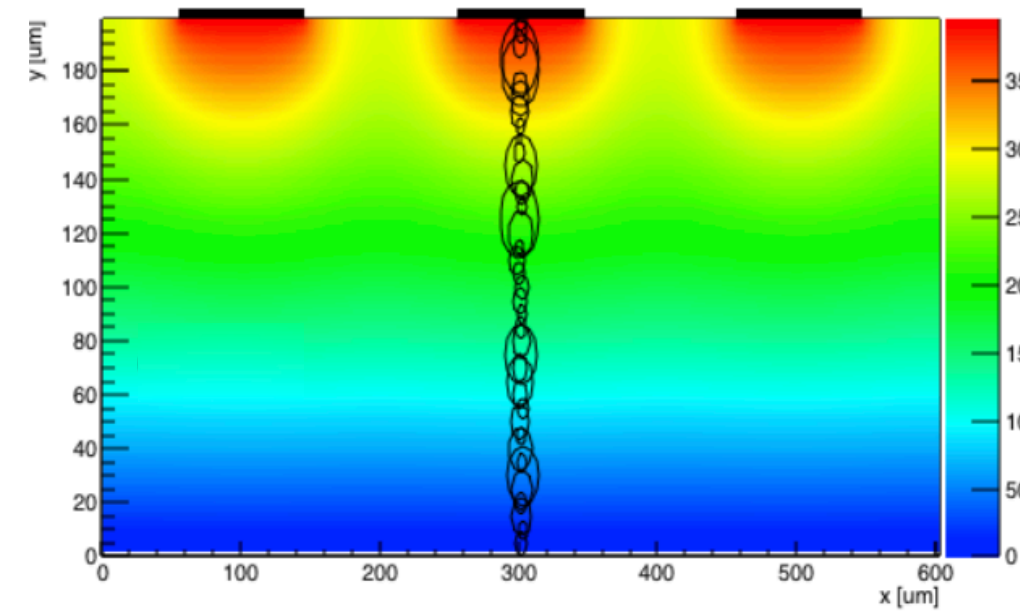
- ▶ photon absorbed in **drift region**
  - ➔ **holes** drift through gain layer & multiplied
  - ➔ **first peak** in the spectrum
- ▶ photon absorbed in **absorption region**
  - ➔ **electrons** through gain layer & multiplied
  - ➔ **second peak** in the spectrum

Gain measured:  $\sim 20$  for  $^{55}\text{Fe}$   
(corresponding to  $\sim 60$  for a m.i.p.)





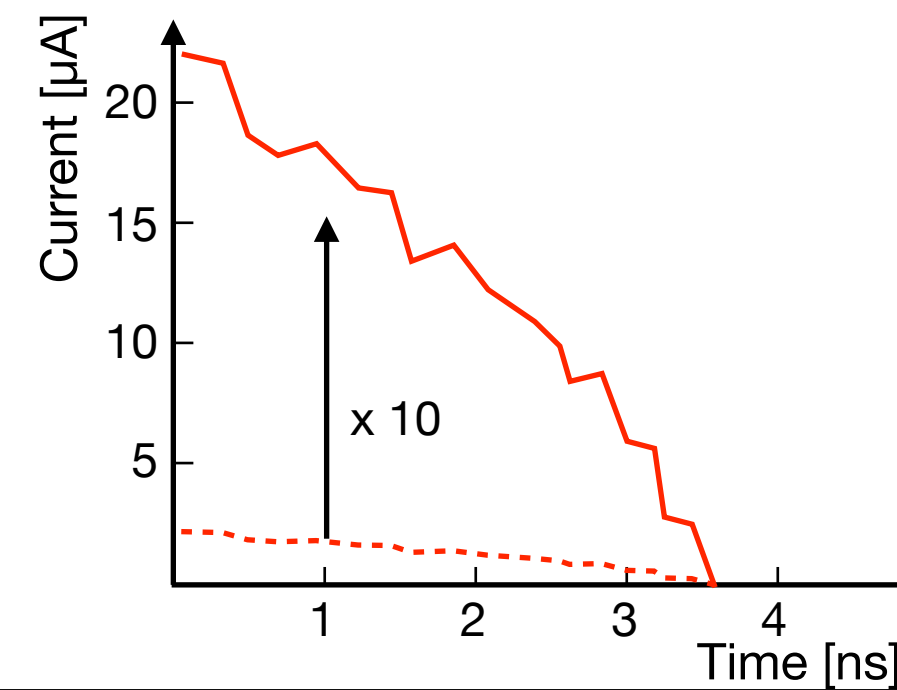
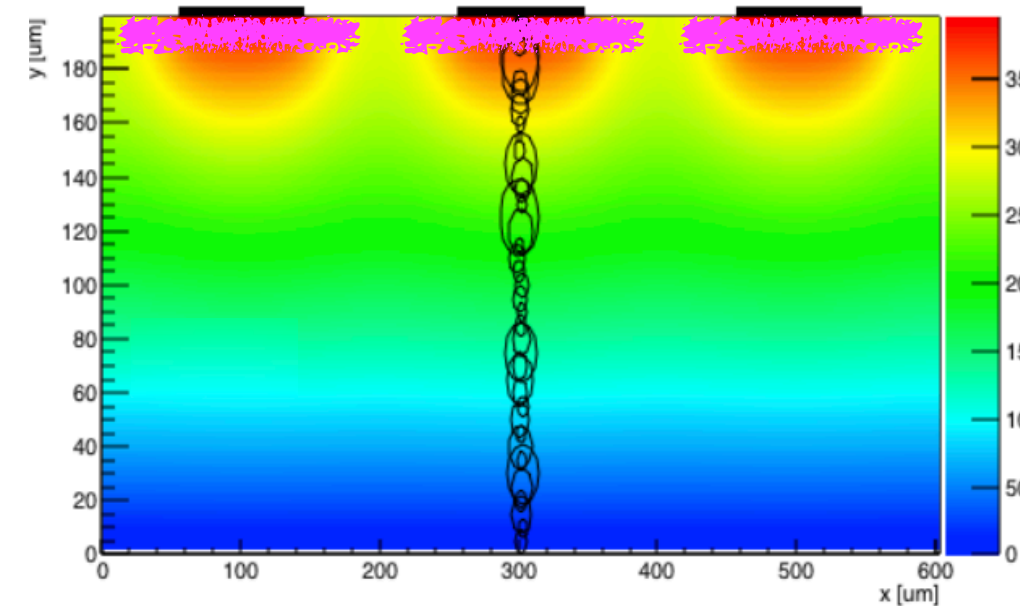
PN junction  
(no gain layer)



Landau noise is produced by the **charge collection** at the electrode: when a large cluster of charge is collected, the current drops suddenly producing a **jitter in the signal**

gain layer →

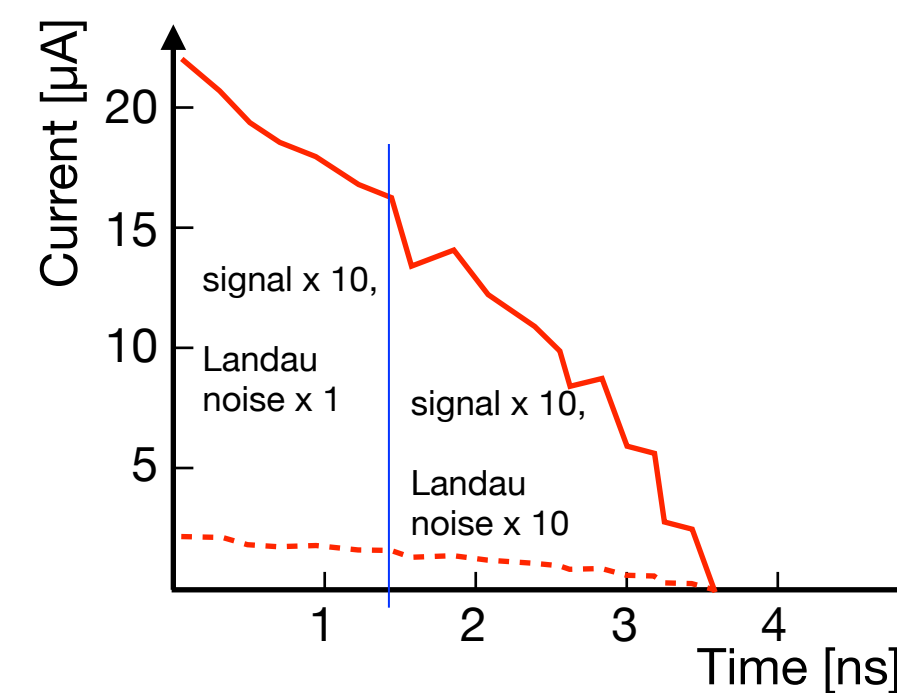
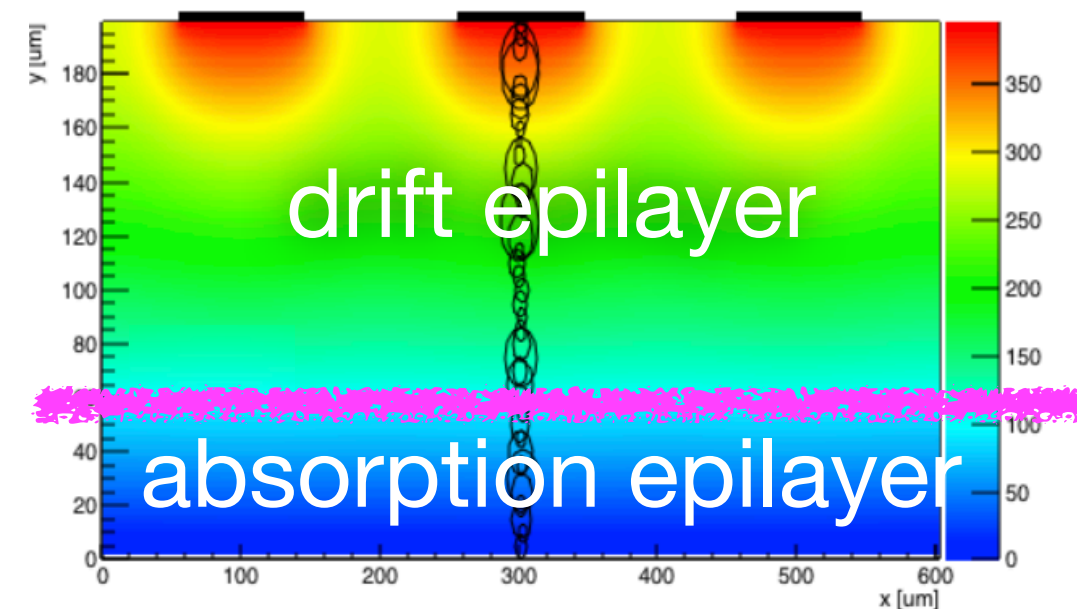
**LGAD**



In an LGAD, **all the Landau noise is multiplied by the gain factor** ( $G = 10$  in the figure) and becomes a limiting factor.

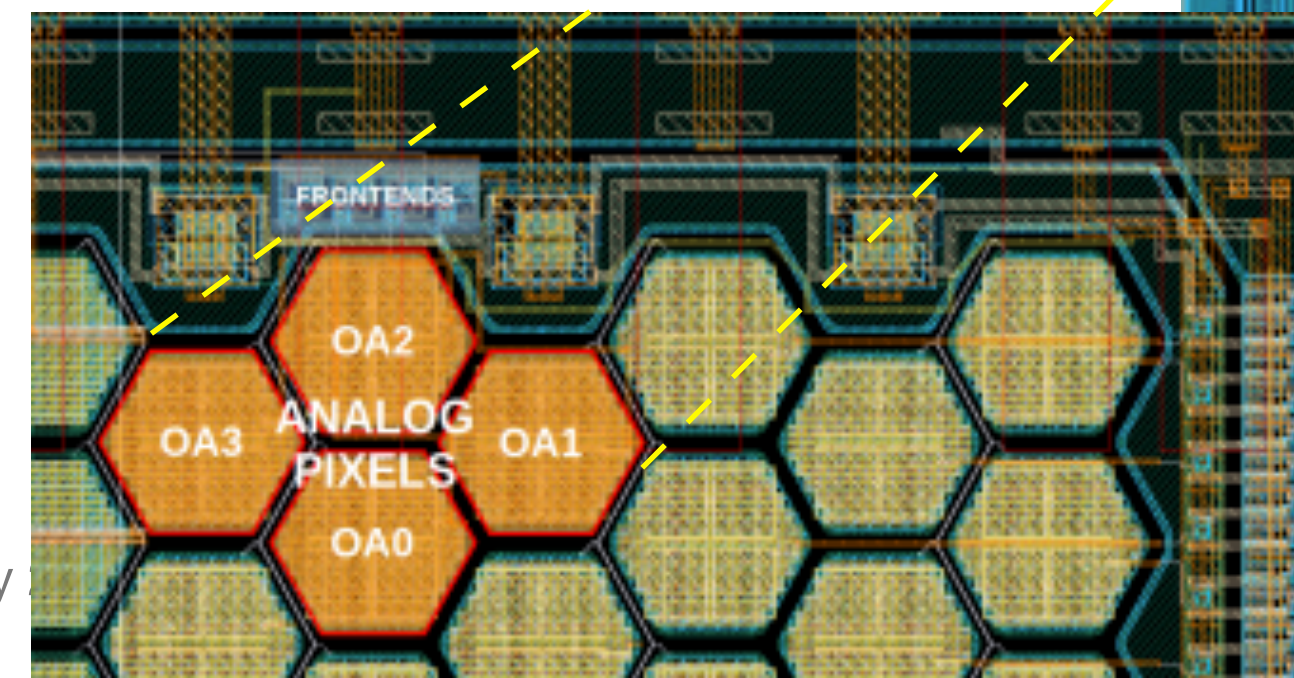
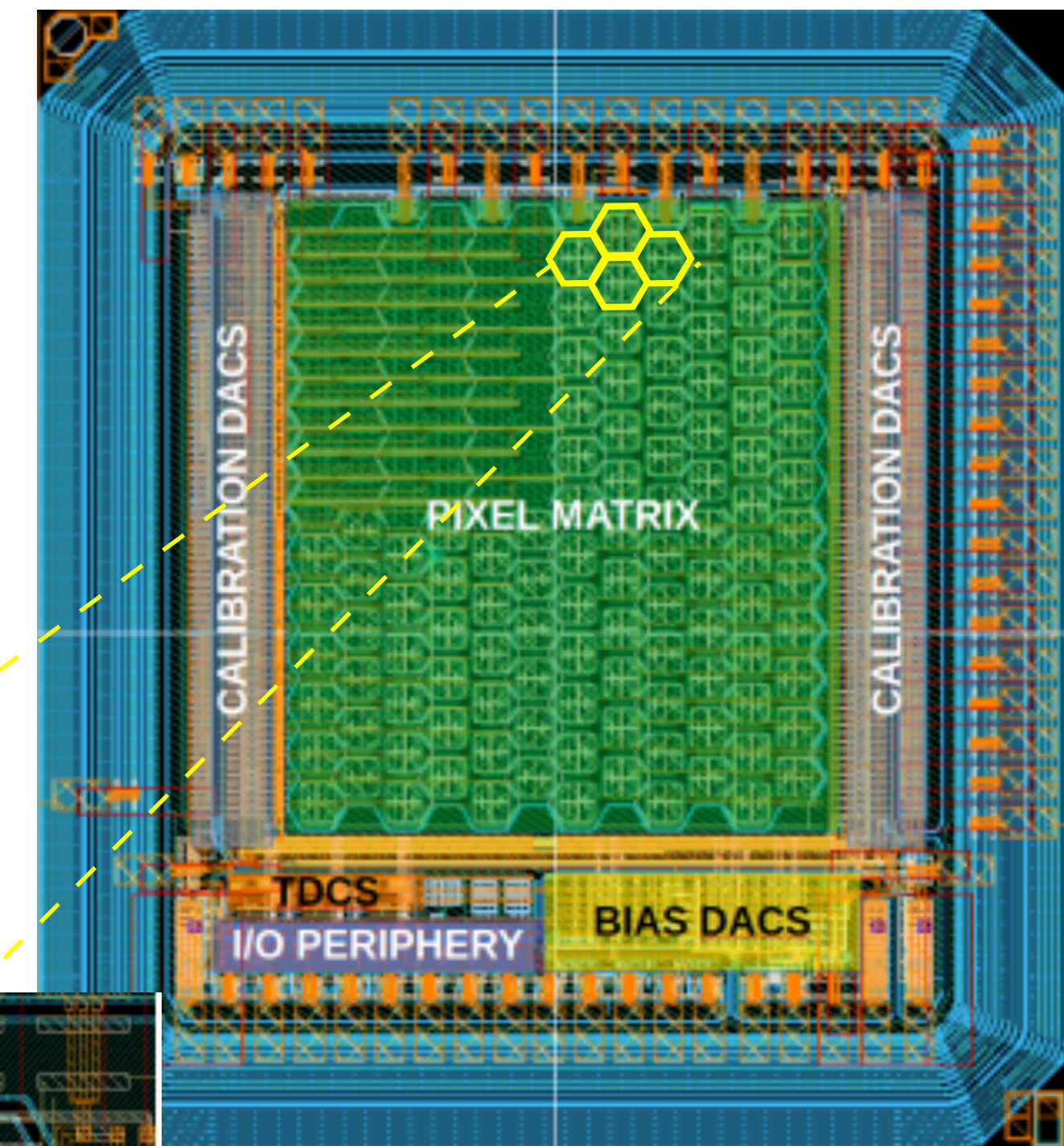
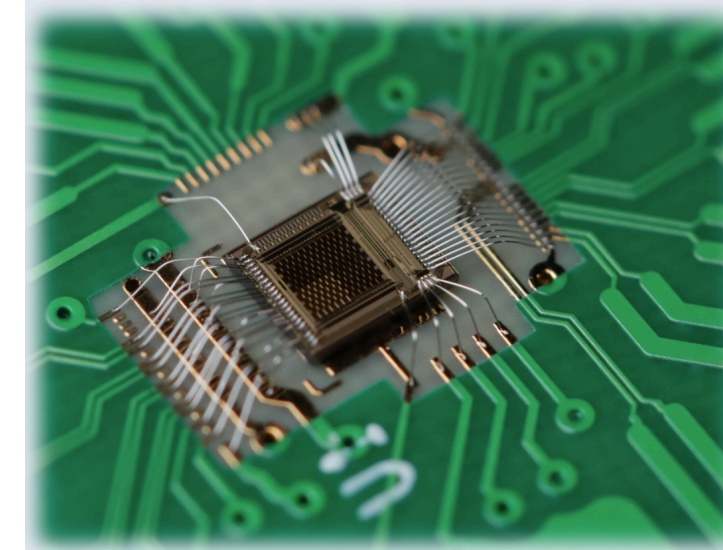
**PicoAD**

gain layer →

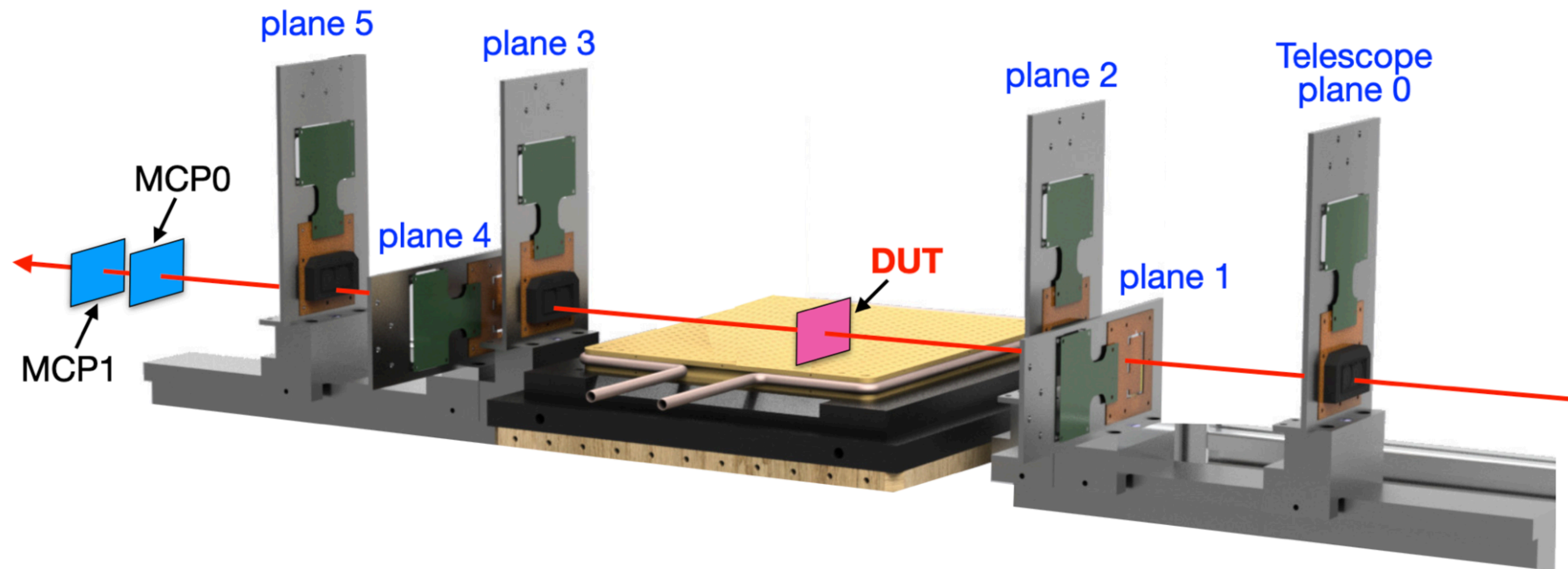


In a PicoAD, only the Landau noise produced by the absorption layer (that arrives at the electrode late) is multiplied by the gain factor. Thus the **Landau noise at the start of the signal is minimised.**

- Same matrix configuration as prototype1, but
  - ▶ **Substrate:**  $50\Omega\text{cm}$  →  $350\Omega\text{cm}$  epilayer,  $50\mu\text{m}$  thick on low-res ( $1\Omega\text{cm}$ )
    - ➔ smaller pixel capacitance
    - ➔ depletion  $23\mu\text{m}$  →  $50\mu\text{m}$
    - ➔ larger voltage plateau
    - ➔ that allows operating sensor with  $V_{\text{drift}}$  saturated everywhere
  - ▶ **Preamp and driver voltage decoupled**
    - ➔ was limiting optimal amplifier operation
    - ➔ was creating cross-talk; removed
  - ▶ **Optimised FE layout, differential output**, high-frequency cables
    - ➔ better rise time ( $600\text{ps}$  →  $300\text{ps}$ )



SPS testbeam in 2023 with 120 GeV/c pions to measure **efficiency** and **time resolution**



**UNIGE FE-I4 telescope** to provide spatial information ( $\sigma_{x,y} \approx 10 \mu\text{m}$ )

**Two MCPs** ( $\sigma_t \approx 5 \text{ ps}$ ) to provide the timing reference

