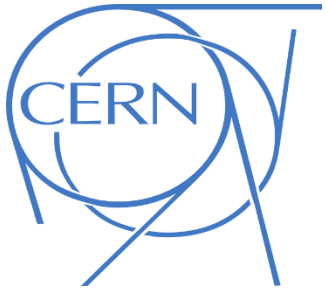
**PM2024 - 16th Pisa Meeting on Advanced Detectors**
Isola d'Elba, 26 - 1 June 2024

# On novel front-end electronics for the ATLAS BI RPC upgrade at HL-LHC developed in SiGe BiCMOS technology with a high-resolution rad-hard Time-To-Digital converter embedded

Luca Pizzimento on behalf of ATLAS muon community





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# ATLAS RPC Phase-II Upgrade Overview

HL-LHC increased luminosity and much harsher conditions:

- Luminosity up to $\mathbf{7,5 \times 10^{34}\ cm^{-2}s^{-1}}$
- *Pile-up* $\langle \boldsymbol{\mu} \rangle$ ***up to*** $\mathbf{200}$
- Target: integrate 3000-4000 $fb^{-1}$ (100 times Run-2)
- In these conditions the actual trigger can record only muons with pt > 50 GeV

2 main upgrades RPC related are in progress for the ATLAS Muons spectrometer Phase-II

- **The electronics of the ATLAS RPC currently installed will be replaced**

  The present electronics does not meet the Phase-2 specification,
  Readout buffer on the Front-End (FE) will not be used. Full information to be sent to backend
  and used in the trigger decision

- **Installation of a new RPC layer in the Inner Barrel (BI) of ATLAS muon system**

  New RPC detectors installation in the entire inner barrel to improve the RPC trigger coverage and
  new sMDT BIS chambers to gain space for new RPC layers

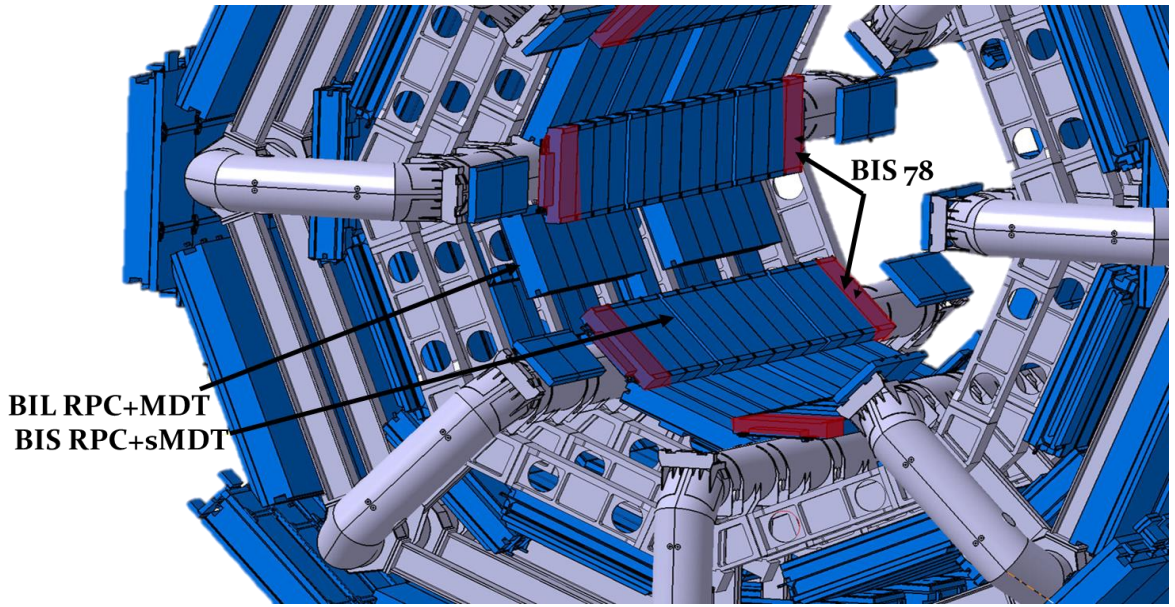
see posters:

- ”The ATLAS RPC Phase II upgrade for High Luminosity LHC era” by Gregorio Falsetti
- ”Production and test of BI-RPC detectors for ATLAS Phase II upgrade” by Mattia Francesco Perrone

# ATLAS RPC Phase-II – BI project

The BI project will consist in the coverage of the inner barrel of the ATLAS experiment with 306 triplets made of the new generation of RPC detectors

- More Redundancy (6→9layers)
- Longer lever arm (2.3 m→4.5 m)
- Increased acceptance (80%→96%)
- Improved tracking and trigger capability wrt current system
- Good time resolution enabling high-performance TOF




**The main challenges to be faced by the RPC BI project:**

1. **Physical encumbrance**

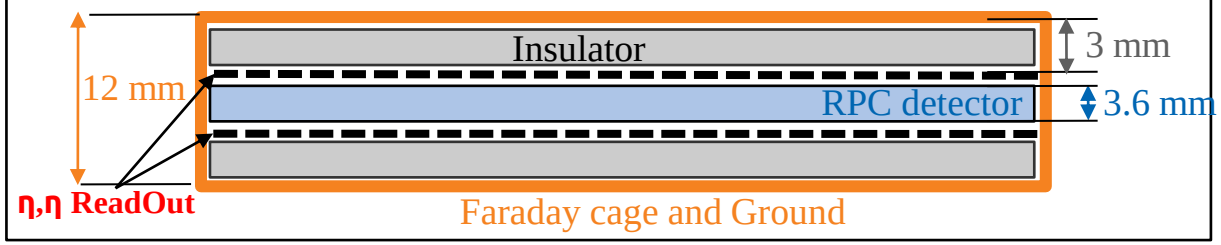
2. **Detector rate capability:** The ATLAS currently installed RPCs are certified to work at 100 Hz/$cm^2$ for 10 years. The measured rate capability of these detectors is around 1 kHz/$cm^2$. The actual RPC performance cannot be guaranteed in the harsher conditions of HL-LHC

**The new Front-End electronics represents one of the main upgrades for the ATLAS Phase-II RPC**

- Improved signal-to-noise ratio which allows the reduction of the average charge per count in the detector of one order of magnitude wrt the currently installed system, leading to an improvement of the rate capability from **1 KHz/$cm^2$ to 10 KHz/$cm^2$**

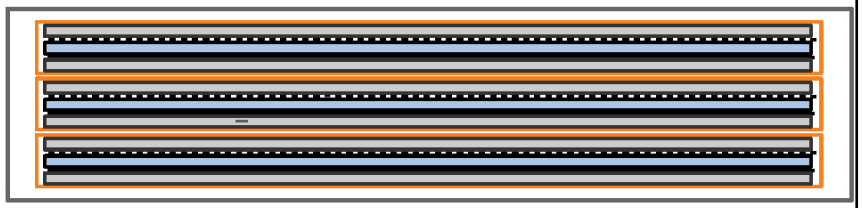
# BI RPC Challenges – Physical encumbrance & new detector structure

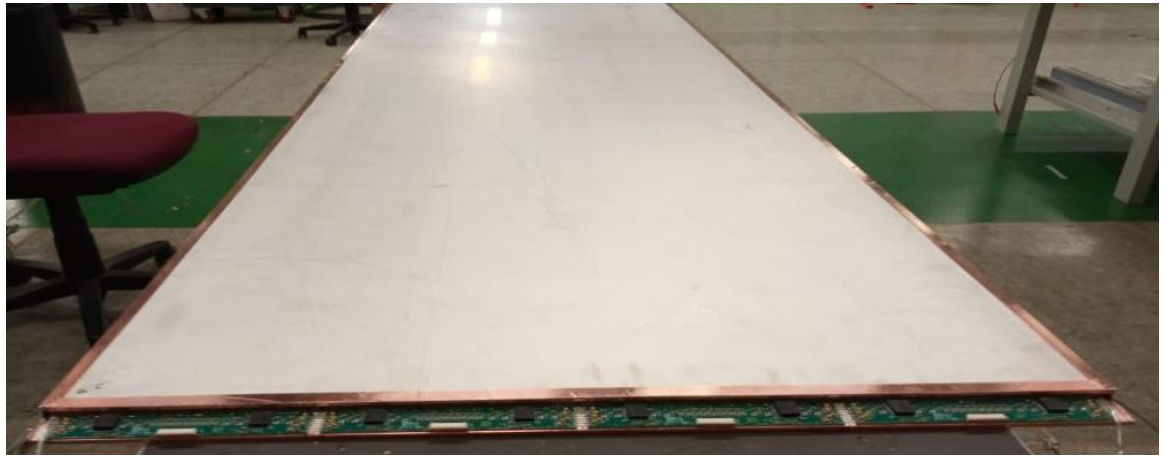
***BI RPC singlet layout***




***RPC triplet layout***

- 3 independent singlets
- Up to 36 x 8 η FE chs





| | ATLAS RPC currently installed | ATLAS New generation RPC |
|---|---|---|
| Detector | Mono gas gap | Mono gas gap |
| Gas Gap width | 2 mm | 1 mm |
| Electrode Thickness | 1.8 mm | 1.3 mm |
| Gas Mixture | 95% TFE, 4.7% i-C4H10, 0.3% SF6 | 95% TFE, 4.7% i-C4H10, 0.3% SF6 |
| Time Resolution | 1 ns | 0.4 ns |

**The available space in the ATLAS muon-spectrometer inner barrel implies mainly:**

- Few centimeters space (in the orthogonal direction wrt the beam) for the full detector placement along with most of its services
- Some fully inaccessible zones

**Detector and services structures re-design**

- No room for the electronics on the detector phi side due to geometrical factors and impossibility to overlap the detectors

**Parallel strips readout** (second coordinate measured with the time arrival difference at the detector edges)

**The time resolution < 100 ps of the TDC embedded** in the FE allows the reconstruction of the second coordinate with 1 cm space resolution.

# RPC detector and high-radiation environment

The **RPC rate capability** is mainly limited by the current that can be driven by the high resistivity electrodes.

$$V_{el} = V_a - V_{gas} = IR \Rightarrow V_{el} = \rho d \langle Q \rangle \Phi$$

$$V_{gas} = V_a - \rho \cdot \frac{d}{S} \cdot \langle Q \rangle \cdot S \cdot \Phi_{particles} = V_a - \rho \cdot d \cdot \langle Q \rangle \cdot \Phi_{particles}$$

$$RateCapability = \frac{\Phi}{V_{el}} = \frac{1}{\rho d \langle Q \rangle}$$

ρ: Resistivity of the electrodes
d: Electrodes thickness
Q: Average charge per count

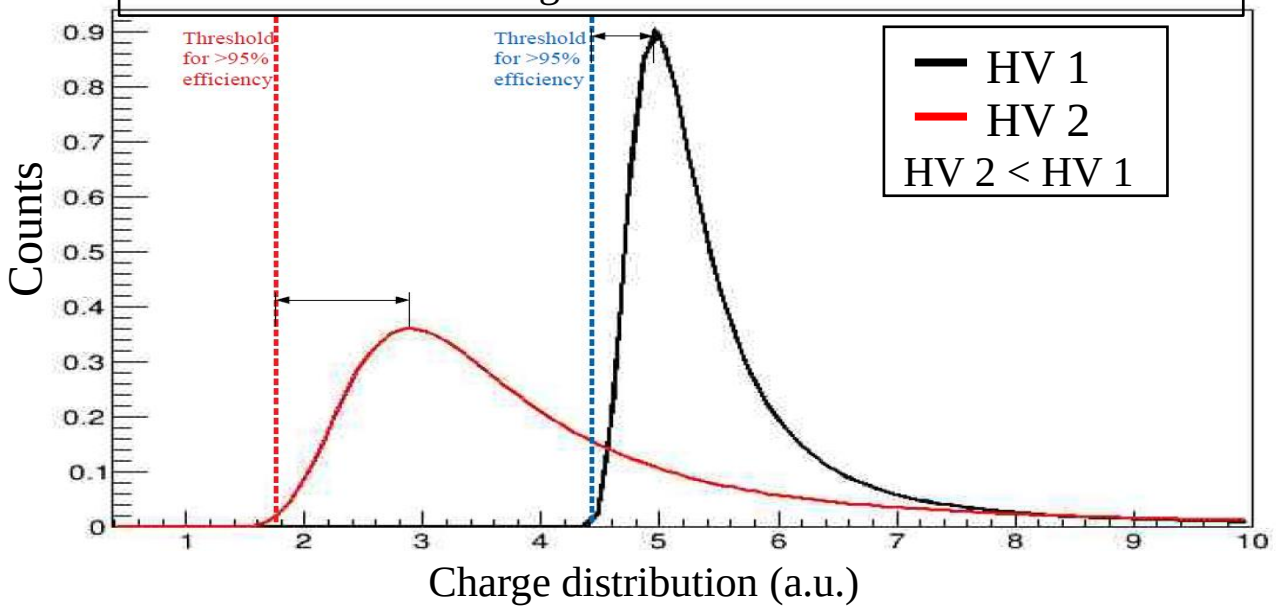
**Reduce the average charge per count Q:**
This only method that permits to increase the rate capability while operating the detector at fixed current.
**No further ageing test required**

Obtained through a reduction in the electric field

- Reduction of the average charge per count (peak value of the charge distribution)
- Charge distribution changes, spreading over a wider range
- Much smaller signals induced on the readout panel
- **Very low threshold required to be fully efficient**

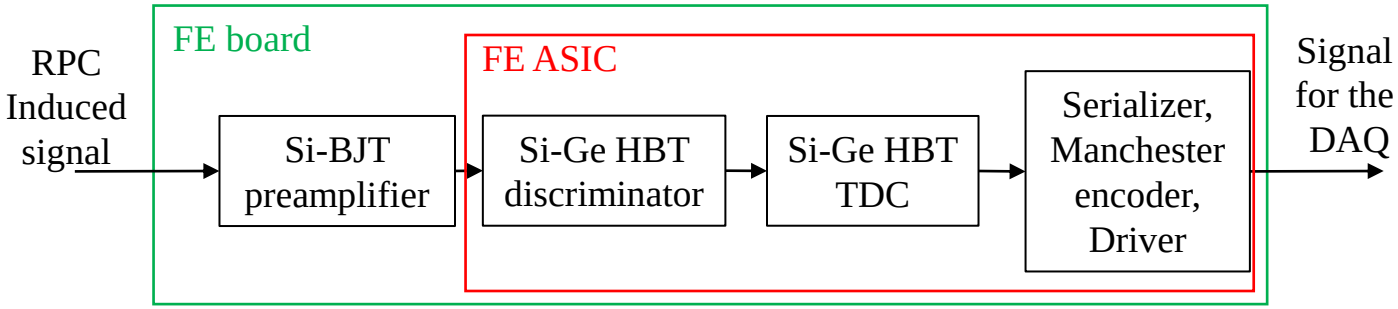
Requirements:
- Very sensitive FE electronics with an excellent signal-to-noise ratio
- High suppression of the noise induced inside the detector by the electronics and by external sources
- Very careful optimization of the chamber structure as Faraday cage

Sketch of the RPC charge distribution as function of HV



# BI Front-End electronics

The FE electronics is realized in a mixed technology of Silicon BJT for the discrete component preamplifier and a full custom ASIC in IHP Silicon-Germanium BiCMOS technology.




**Strategy behind the mixed technology in the FE electronics:**

- Si BJT seems to be more robust to ESD coming from the RPC detector
- Possibility to repair broken discrete components
- ESD protection still included at the input connection with the readout panel

1. Minimum Threshold of 0.3 mV
2. Detectable signal of *1-2 fC*

Reduction of **factor 10** in the charge produced inside the gas gap wrt the ATLAS RPCs currently installed

**Rate capability up to 10 kHz/cm²**

Pubblished on JINST **15** (2020) no.11, C11010

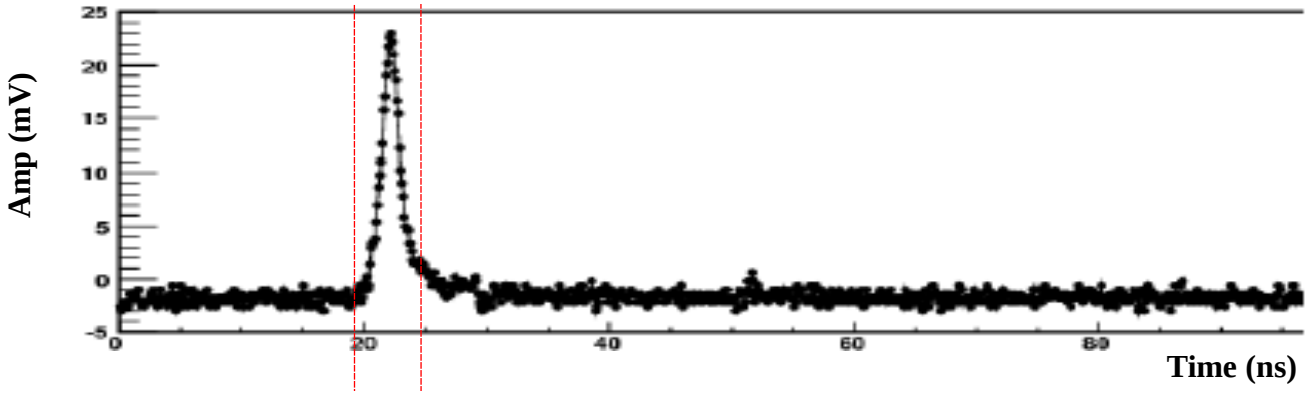
**Overall advantages of low-threshold operation:**

- Rate capability improvement
- Possibility to work at a reduced detector working current → better detector ageing
- **Possibility to use environment-friendly gas mixtures not usable otherwise** (see poster by G.Proto "Study of environment-friendly gas mixture for the Resistive Plate Chambers of the ATLAS Phase-2 upgrade")

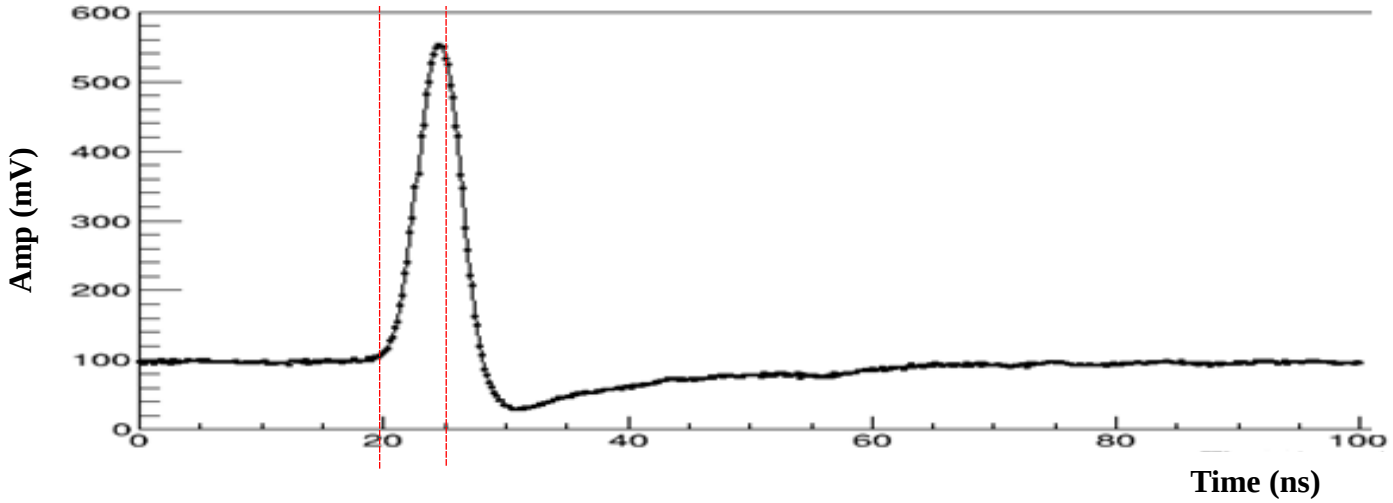
# BI Front-End electronics – Preamplifier

**The new preamplifier** developed for the RPCs is made in **Silicon Bipolar Junction Transistor** technology. It is based on the concept of transimpedance amplifier in a configuration which allows to achieve a fast charge integration

**Typical Pulse of a 1mm RPC gas gap**




**Output Pulse from the preamplifier for a 1mm RPC gas gap signal**

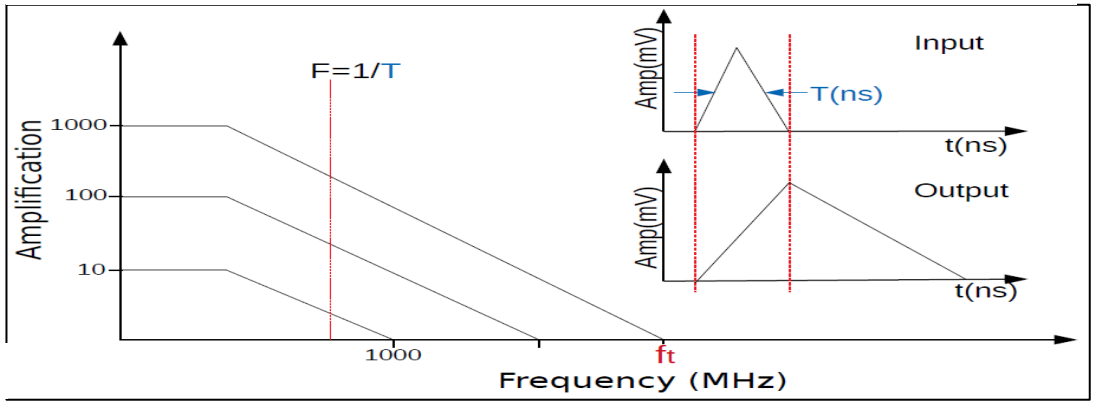



- Amplification factor: 3-4 mV/fC
- max equivalent input noise → min= 1000; max=2000 (electrons RMS )
- Bandwidth: 100 MHz
- Power consumption: 2 mW/ch

Advantages of this architecture:

- Achieves the integration exploiting the working point outside of the bandwidth and the internal capacitor of the BJT
- Improved radiation hardness due to the chosen architecture

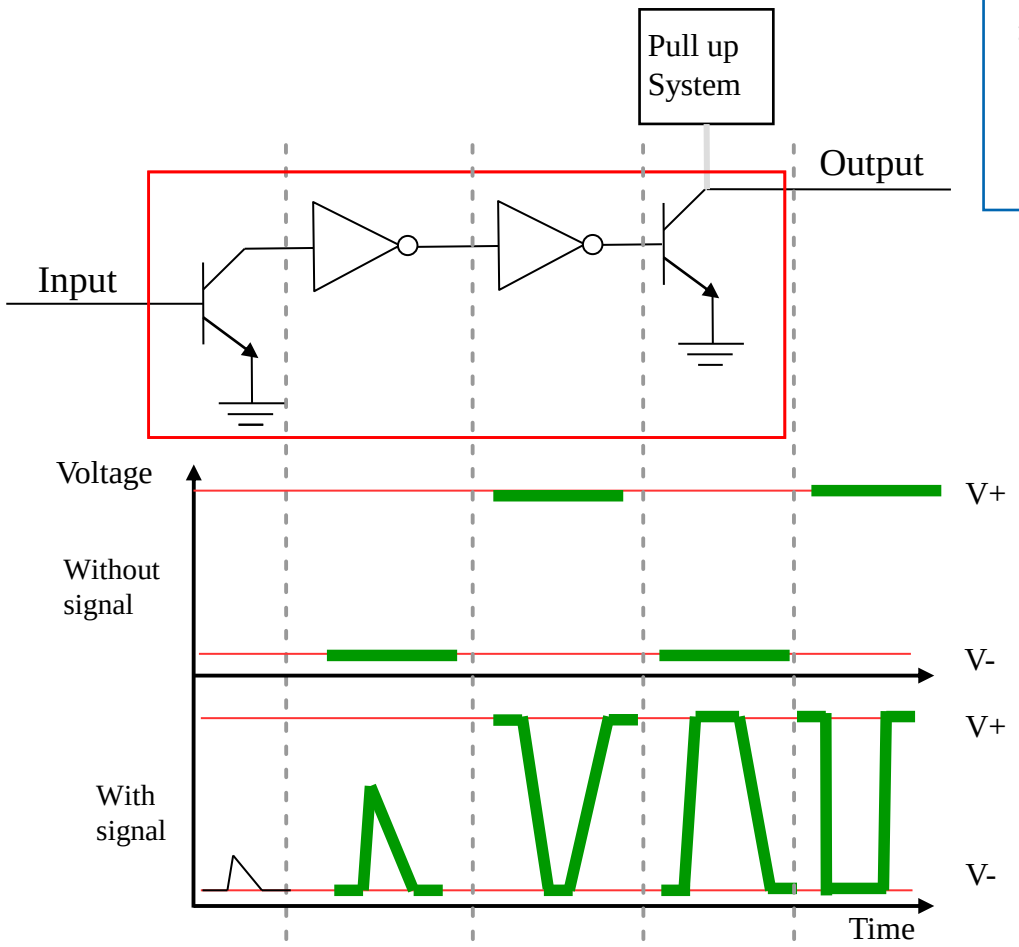
**Transimpedance charge amplifier conceptual scheme**

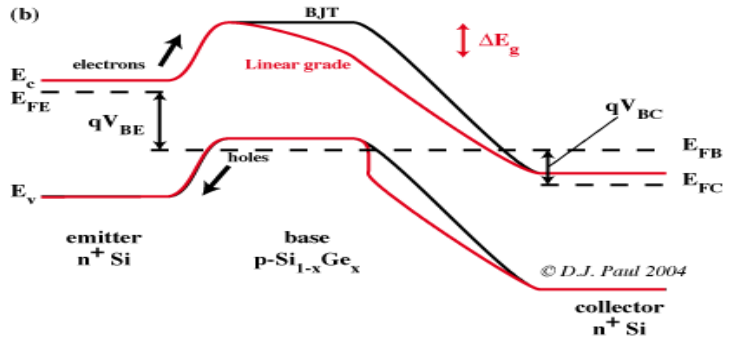


# Front-End electronics – Discriminator

**The new full-custom discriminator** for high-rate environment is developed by using **the Silicon-Germanium HJT technology.**

- Limit amplifier concept
- Time-Over-Threshold measurement
- Limit amplifier is chosen considering the charge distribution of the RPC




**The principle of SiGe heterojunction bipolar transistor (HJT)** is to introduce a Silicon-Germanium impurity in the base of the transistor. The band structure introduces a drift field for electrons into the base of the transistor, producing a ballistic effect that reduces the base transit time of the carriers injected in the collector

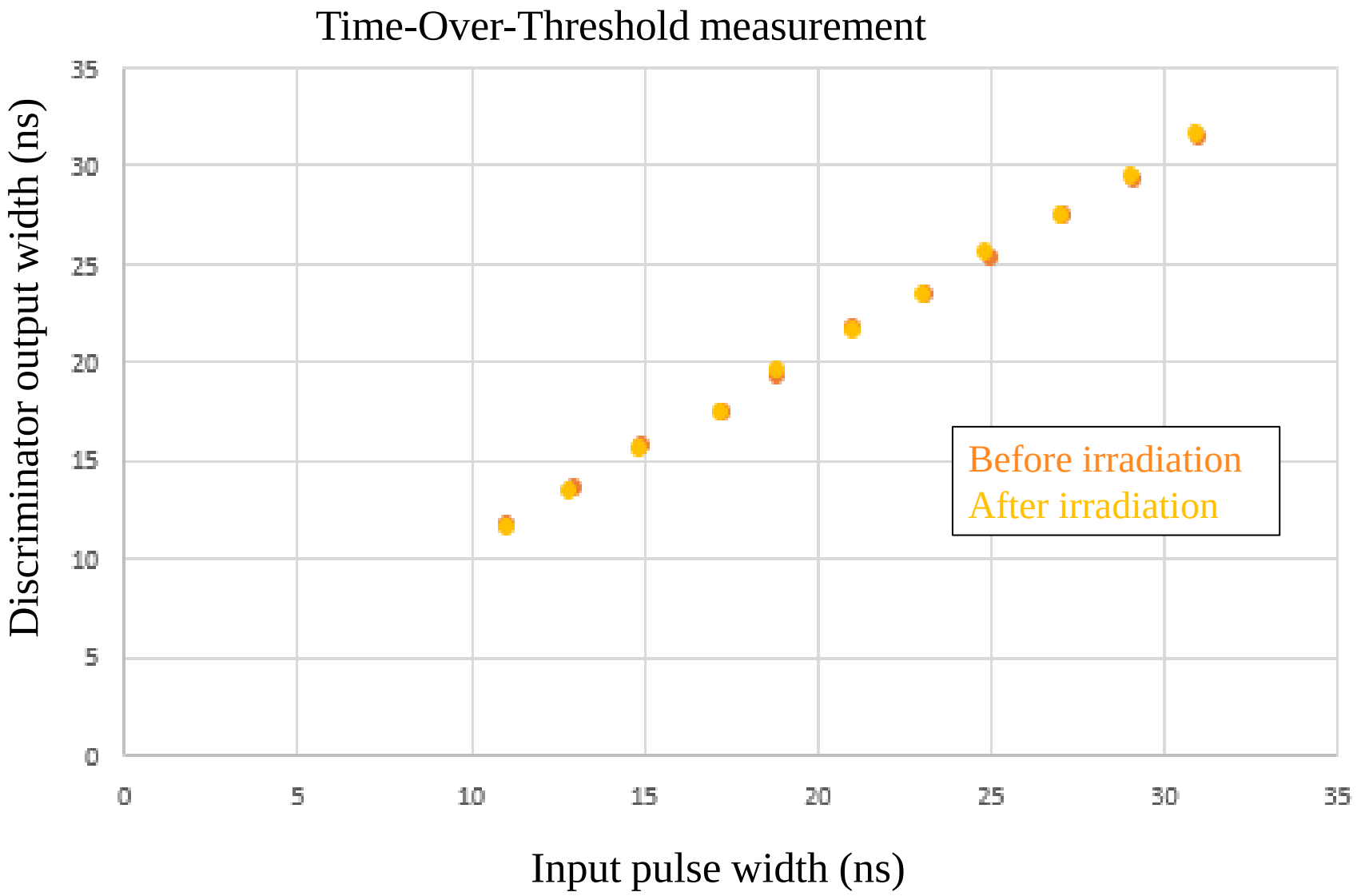
Improvement in the transition frequency and a much higher amplification

| Technology | SiGe BiCMOS 130 nm |
|---|---|
| Minimum threshold | 3 mV |
| Minimum pulse width for linear response | 0.5 ns |
| Bandwidth | 100 MHz |
| Double pulse separation | 1 ns |
| Radiation hardness | $10^{13}\ \frac{n}{cm^2}$ |

Advantages of this architecture:

- No positive feedback → improved stability in terms of self-oscillation
- Minimized dead-time → high repeatibility
- Improved radiation hardness due to the architecture designed

# Front-End electronics – Discriminator TOT measurement




Irradiation measurement performed at the China Spallation Neutron Source (Dongguan) with 10 ASIC samples

TOT measurement to verify proper behaviour after irradiation

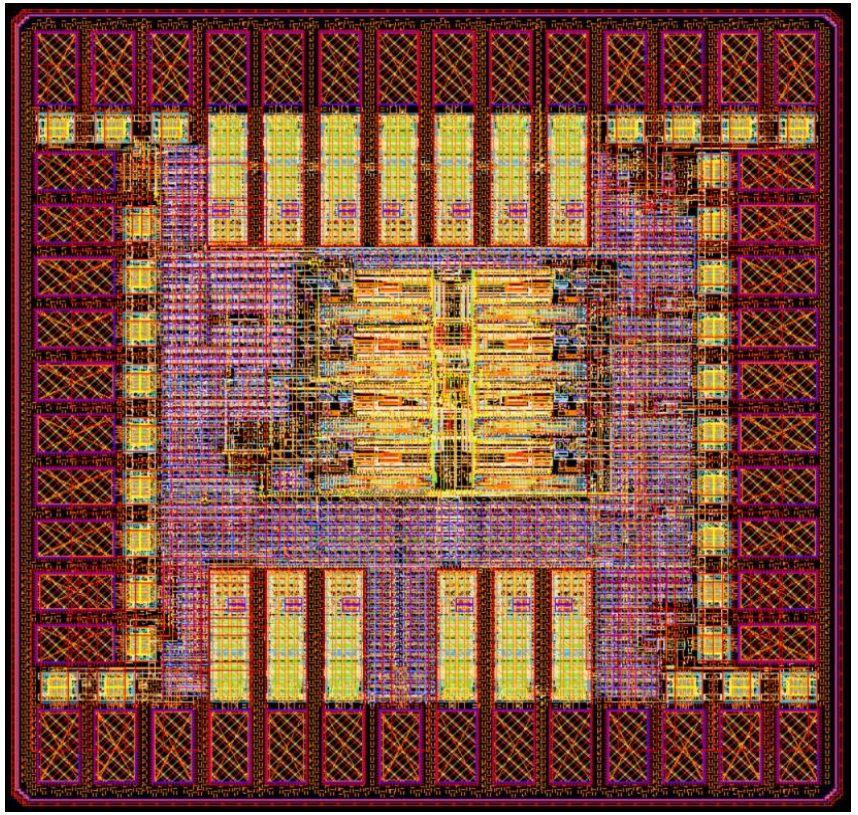
Irradiation flux: $10^{13}\ \frac{n}{cm^2}$

**After the irradiation no change in the discriminator response**

# BI Front-End electronics - ASIC Overview

- **Discriminator**
  - Limit amplifier
- **TDC**
  - Voltage Controlled Oscillator (VCO); free running oscillator which defines the TDC time resolution driving the scaler
  - Scaler; 8-bits synchronous counter
  - FlipFlop & Registers; memories which save the status of the TDC scaler when the RPC(latch) signal is provided
- **Transmission logic, serializer and transmission protocol**

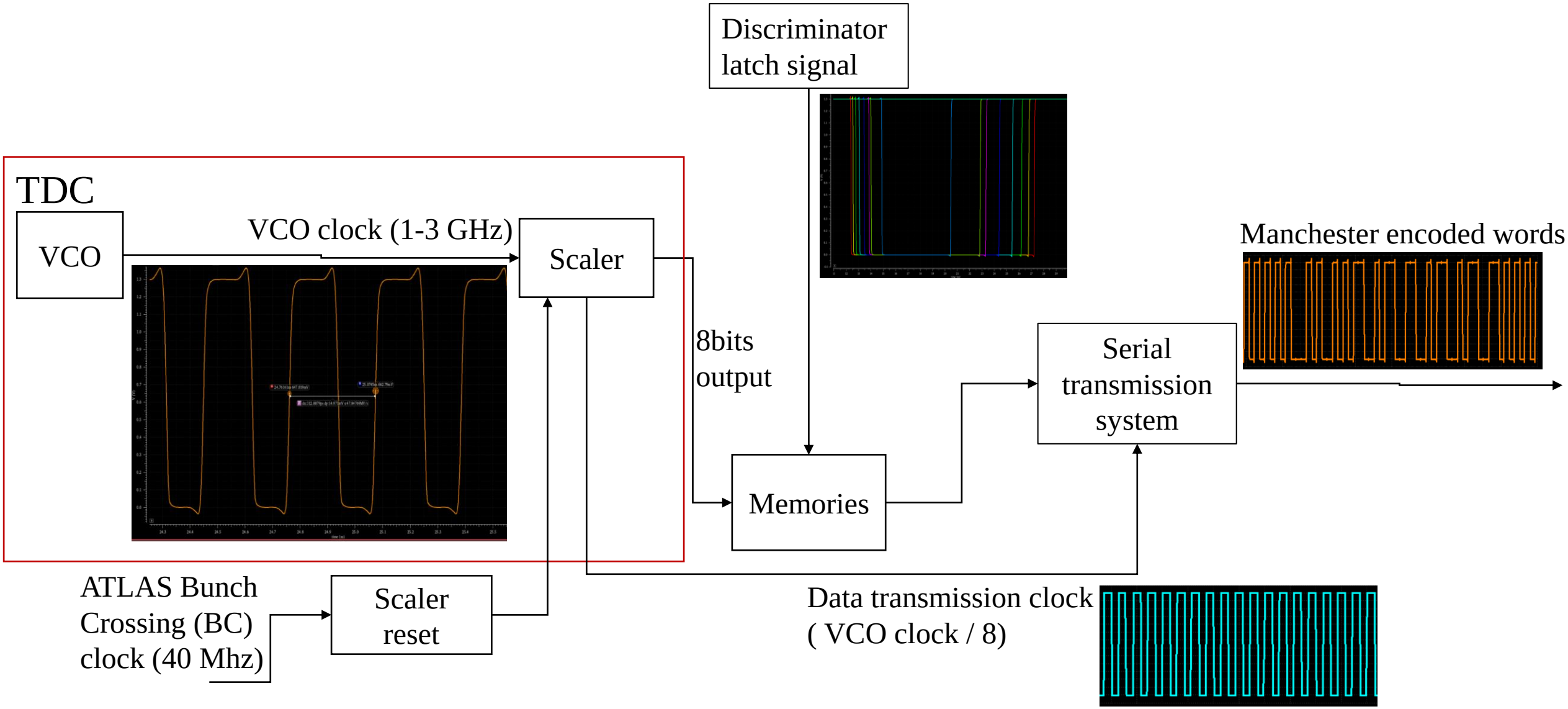
  The data communication to the external DAQ is performed with a serial line for each channel which transmits all the informations Manchester encoded to allow for the reconstruction of trigger candidates



## ASIC foundry runs:

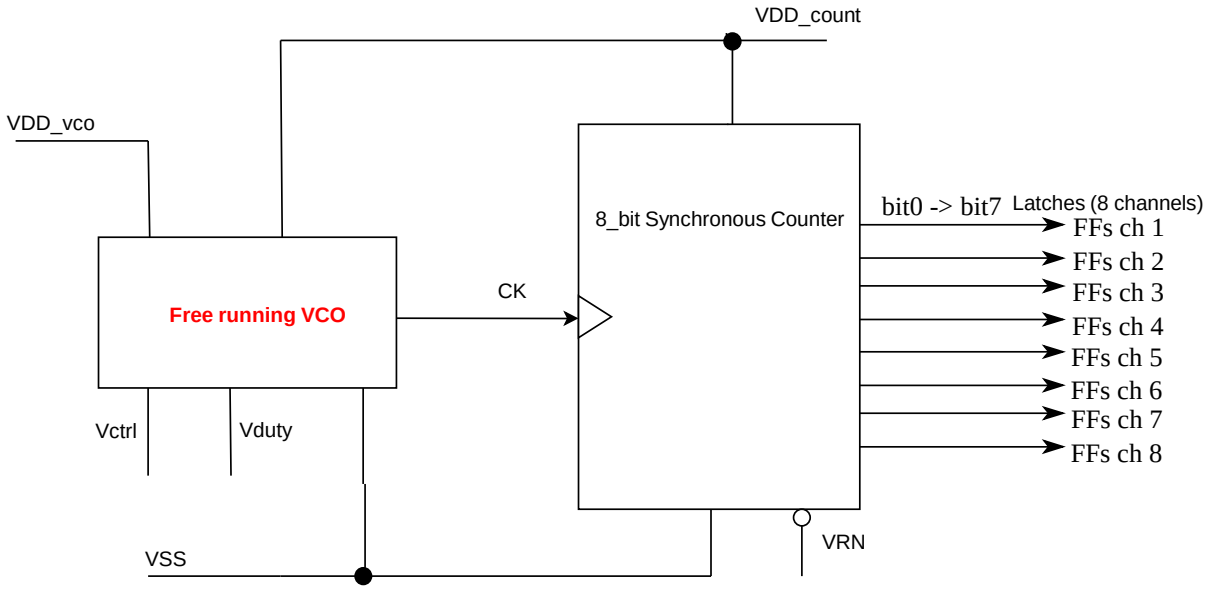
- September 2020; pre-prototype containing the individual components and several single chain configurations
- March 2021; First prototype with the 8-channels configuration along with the final architecture and the transmission system
- July 2021; Same architecture of the previous foundry run with improved technology (250 nm to 130 nm)
- **September 2022; Second prototype with the full configuration, problems fixed**
- **May 2023; First engineering run. Certification test ongoing**

# BI Front-End electronics - ASIC Overview

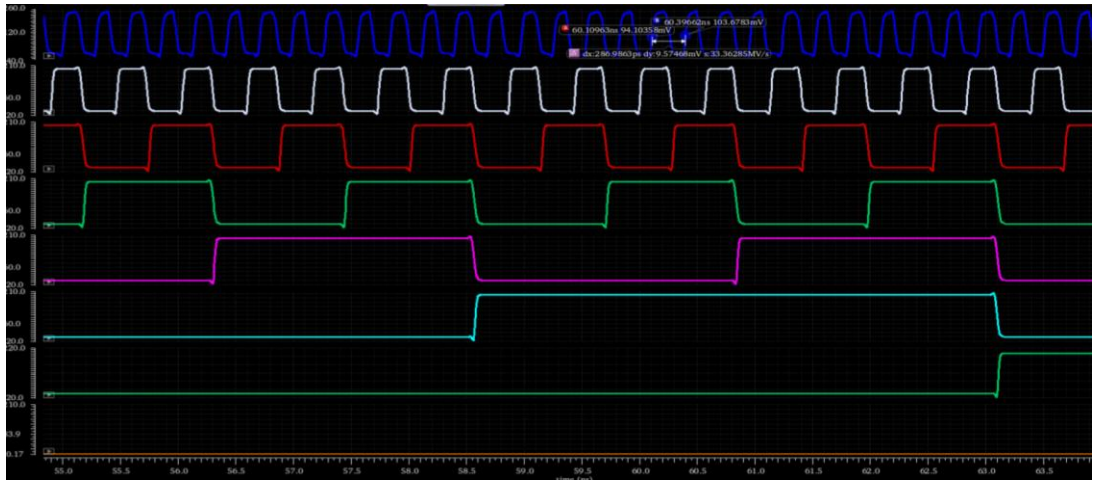


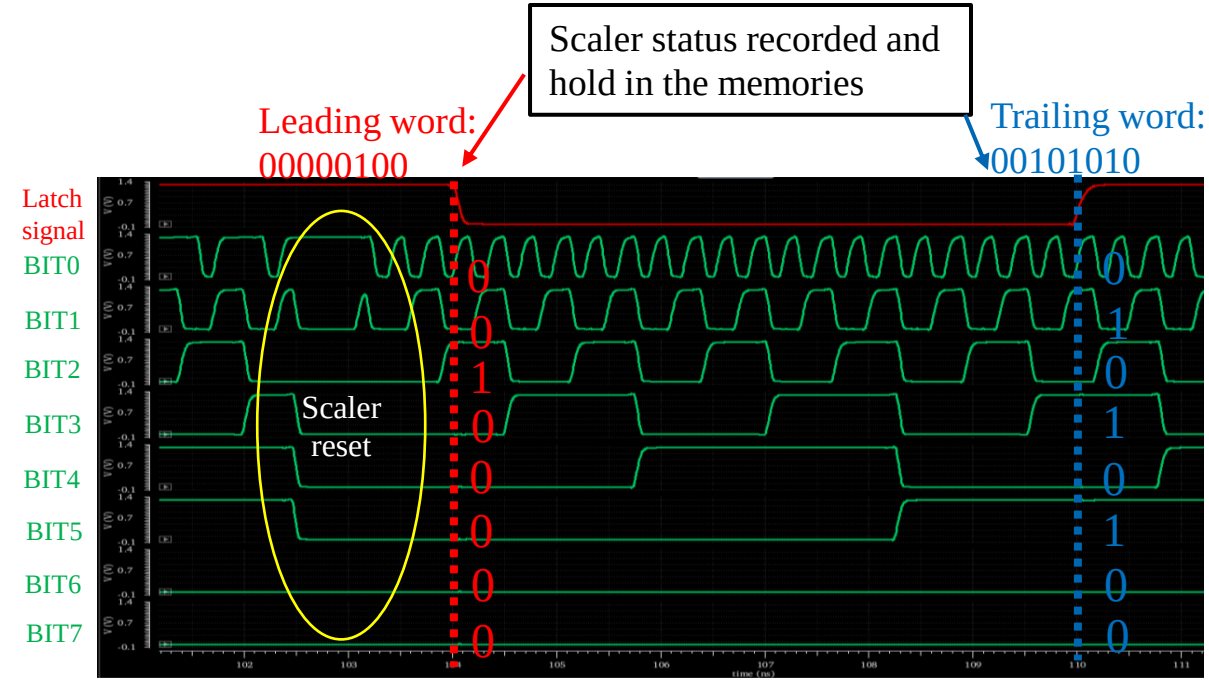
# BI Front-End electronics - TDC

- **Time resolution tunable: 150 - 50 ps rms**
- **TDC power consumption 5 mW**
- **VCO frequency range: 1 – 3 GHz**




Scaler output: Bit 0 … Bit7



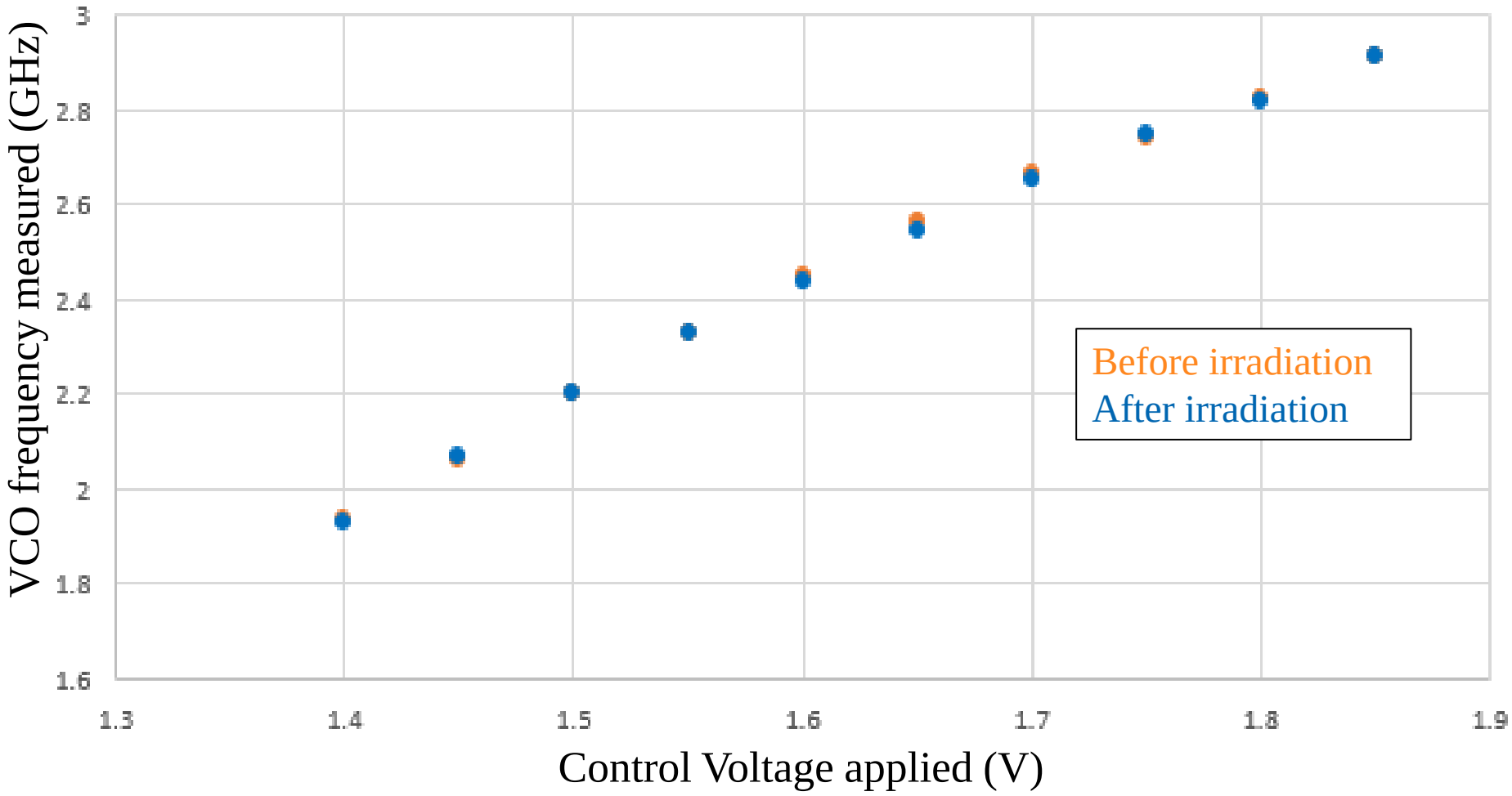



Advantages of this architecture:

- No PLL, nor any sinchronization needed → reduction in the complexity of the FE
- Easier to reach the desired time resolution of the TDC with reduced power consumption and complexity

# BI Front-End electronics – Voltage Controlled Oscillator

Study of the performance of the VCO as function of the voltage that defines its oscillation frequency (Vctrl) **(experimental results)**

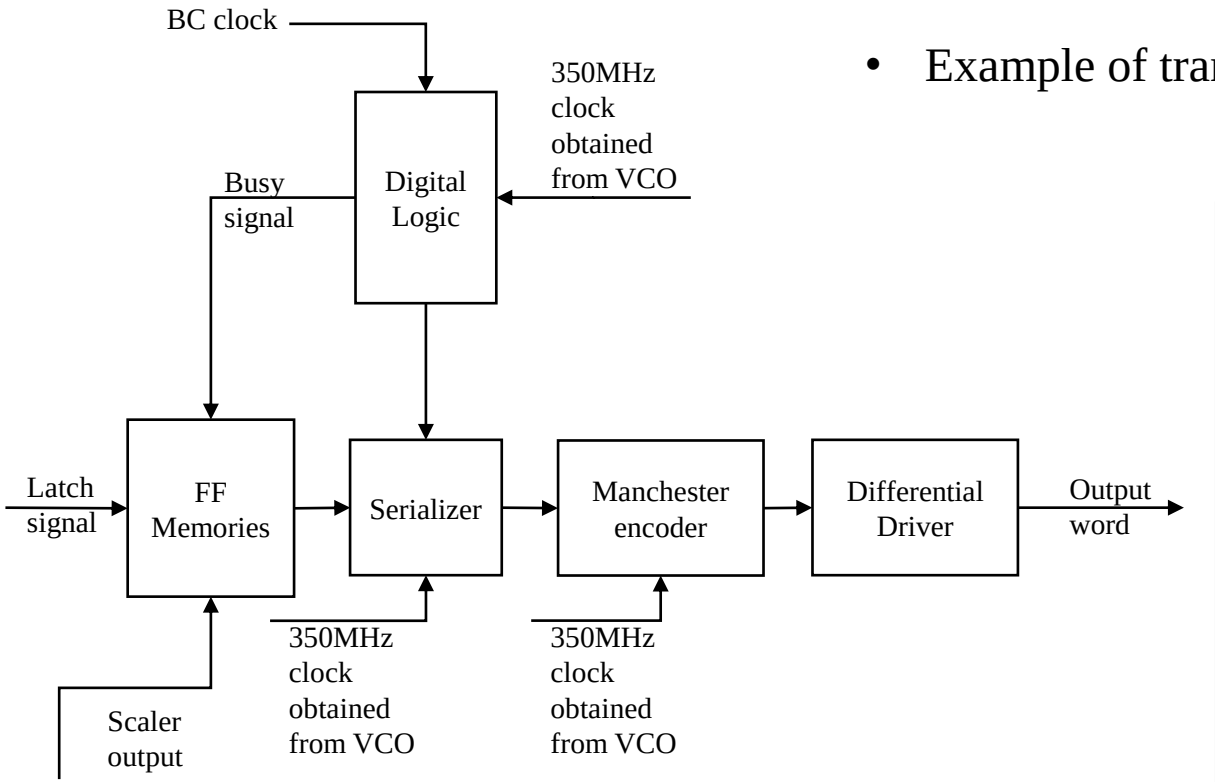



Irradiation measurement performed at the China Spallation Neutron Source (Dongguan, China) with 10 ASIC samples

Irradiation flux: $10^{13}\ \frac{n}{cm^2}$

**After the irradiation no change in the VCO response**

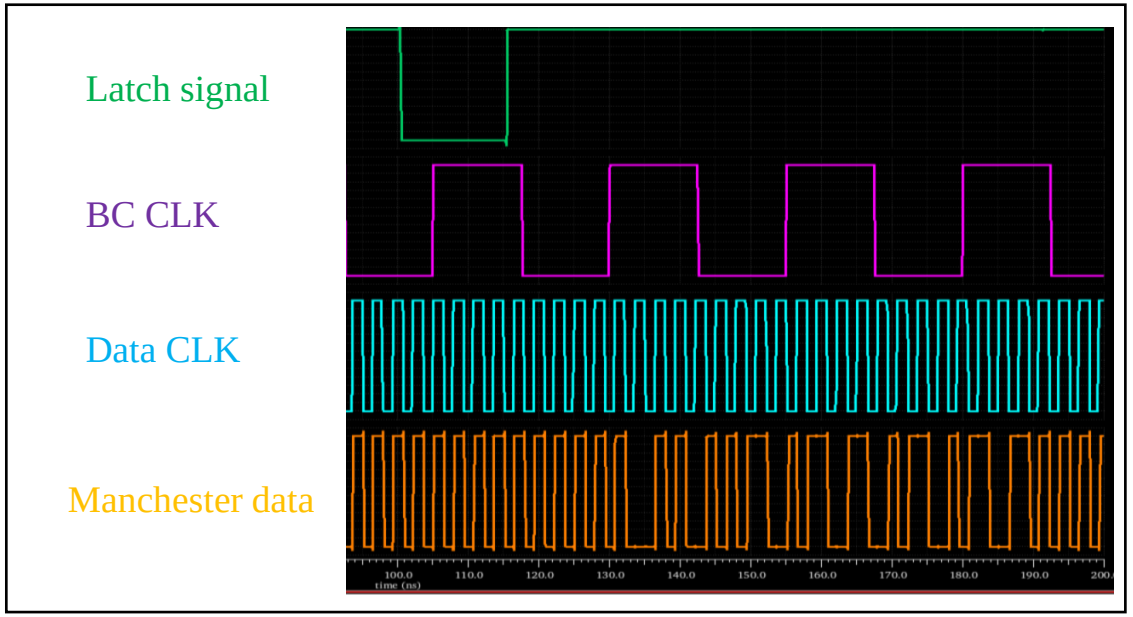
# BI Front-End electronics - Serial transmission




Clock transmission in idle state | Header | Clock transmission in idle state

- Example of transmission: 101010-0010-Manchester encoded data-101010

Manchester error

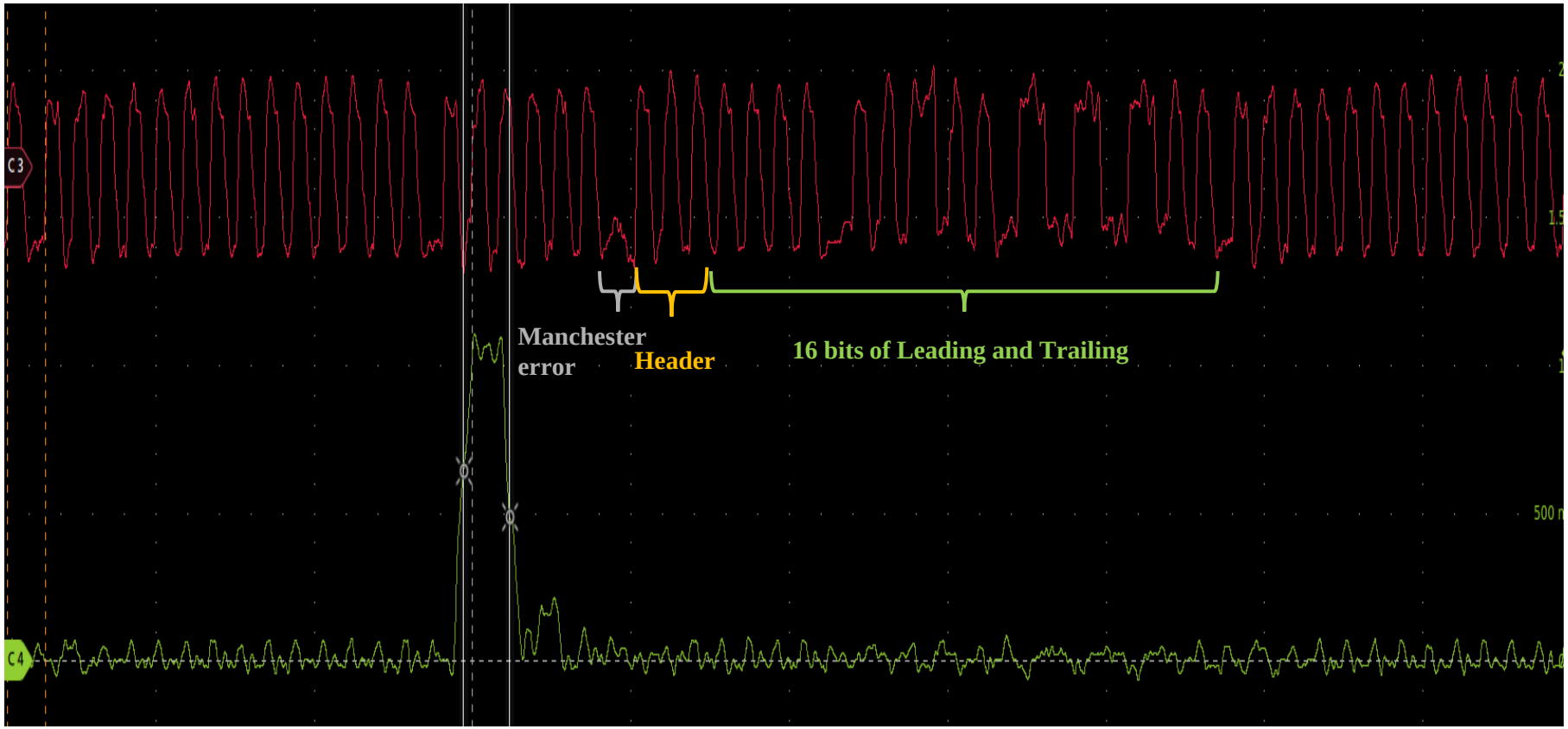



- The data is encoded using the Manchester coding. The transmission consists of 16 bits of leading and trailing + 2 bits of BC counter and 2 bits of header (Manchester error; 3 semiperiod at 0 and 1 semiperiod at 1) to recognize the beginning of a data word in the receiver and to start the decoding.
- Each channel has its own independent serial transmission line

The Manchester encoding is a RZ (return to zero) type encoding, which allows a simple clock recovery. The RZ encoding has been chosen, avoiding to recover the clock with a PLL. This was also done considering the 10^5 transmission lines.

# TDC performance

- Fixed T0 is provided from the 40 MHz BC clock
- Input signal synchronous with the BC clock with variable delay
- Manchester output has been checked and compared with the discriminator signal taking into account the system timing **(fixed T0)**

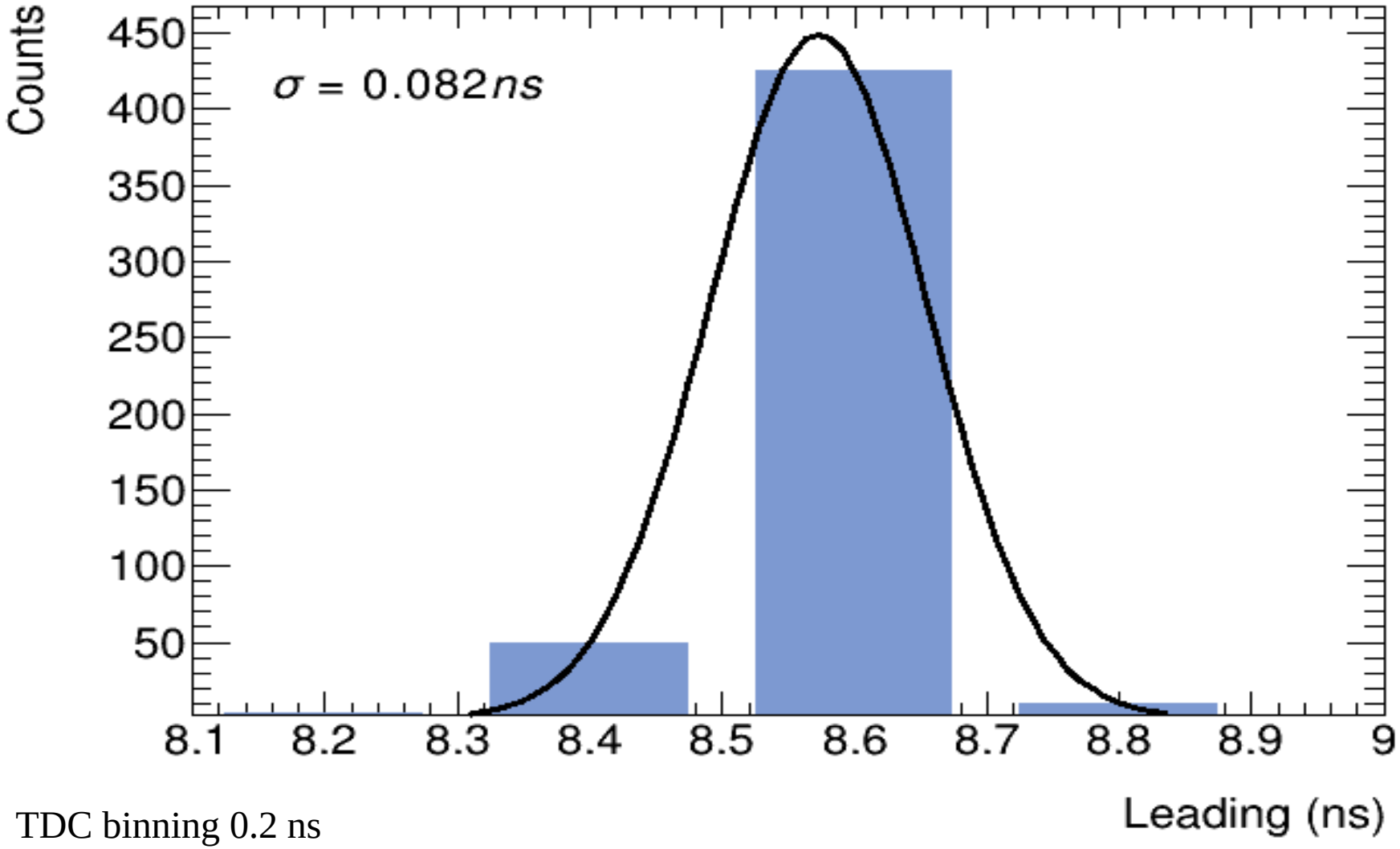



The number of TDC counts is **in every single cases** comparable with the expected one, given by the TDC LSB and the VCO oscillation frequency

The following measurements have been performed:

- TDC resolution with different input signal delays
- Calibration curve

# TDC time resolution



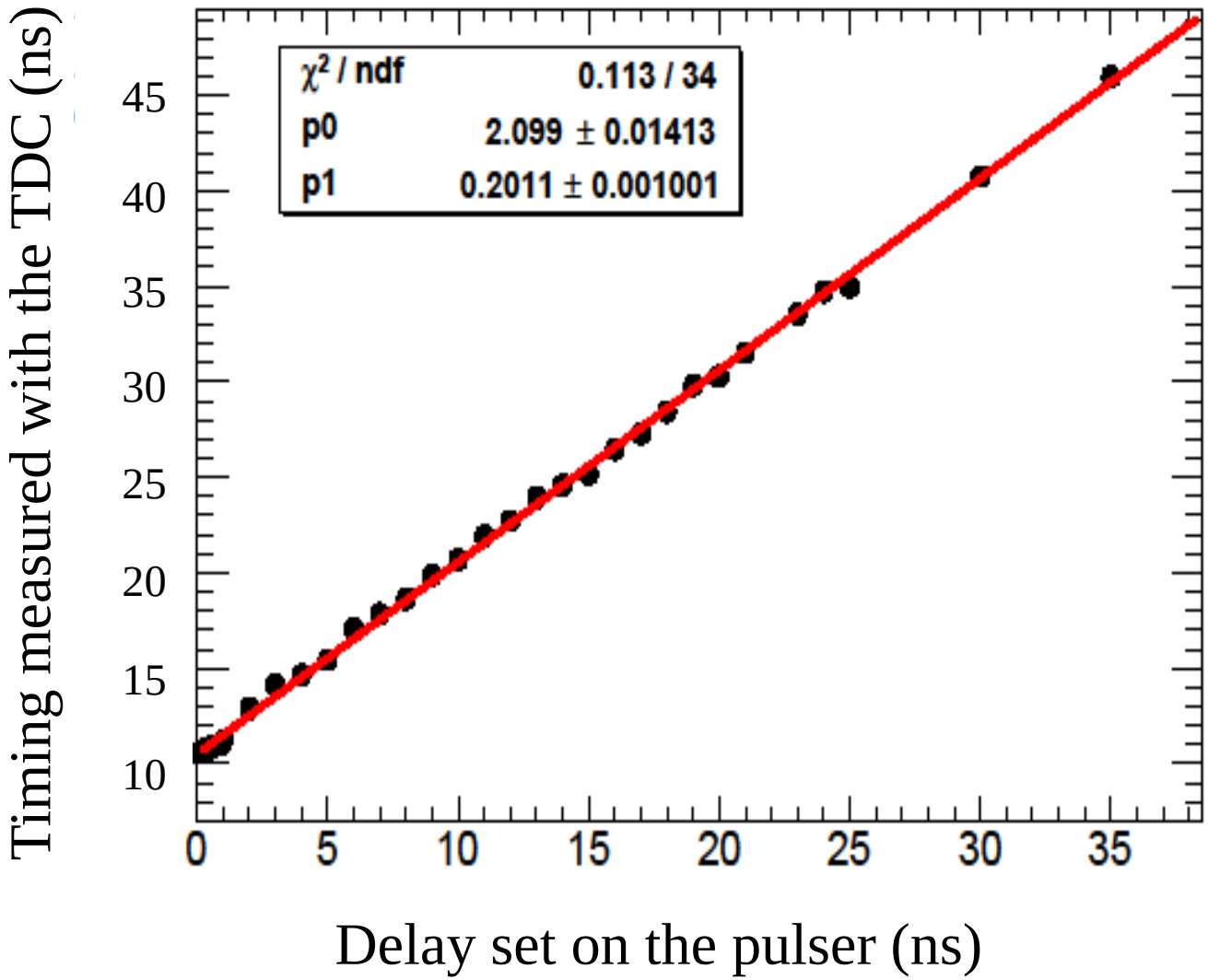

The TDC resolution has been evaluated by sending a signal synchronous with the BC clock which provides the **fixed T0**

This measurements is still affected by:

- the jitter of the injected signal
- noise super-imposed on injected signal

- TDC binning 0.2 ns
- **No cut or correction applied**

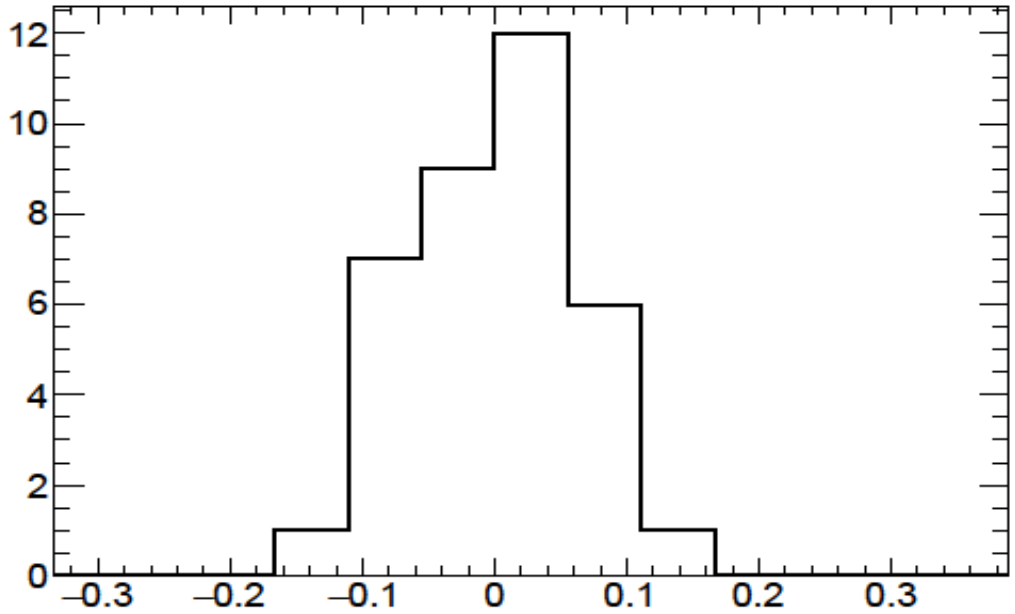
# TDC calibration curve




The delay is measured by multiplying the number of TDC counts times the LSB (0.2 ns).

- The TDC counts are the expected ones for the desired resolution
- This measurement is affected by the noise present in the signal injection system
- Due to the cable lenght there is an offset of around 10 ns

- **The results show that the system is working as designed**



# Conclusion

- The novel Front-End electronics for the RPC detector has been developed successfully
- The amplifier and the discriminator have been developed and a minimum threshold of 1fC of injected charge in the FE has been achieved, leading to the desired improvement in the rate capability of the detector (10 kHz/cm2)
- The TDC developed is working as designed reaching a time resolution of < 100 ps

# Thank you!!!