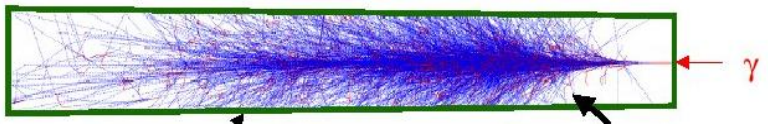
ASICs for 5D calorimetry at OMEGA

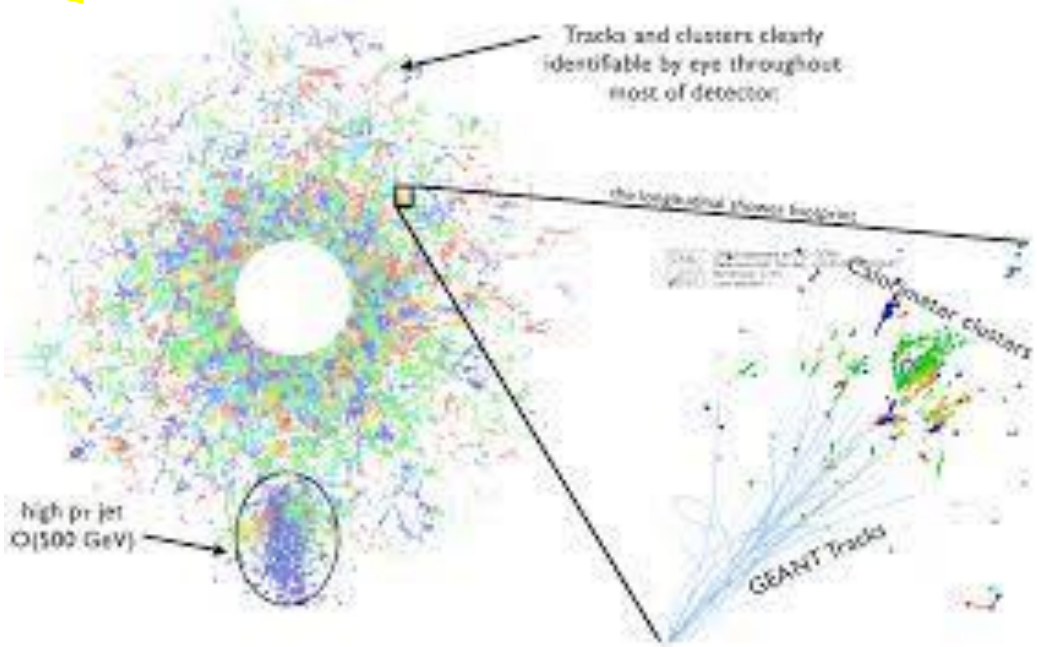
Ch. de LA TAILLE et al. 16th Pisa meeting 2024

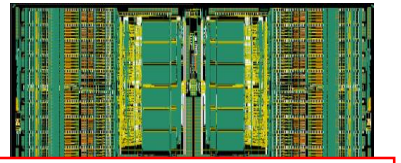
Evolution of calorimetry : « imaging calorimetry »

- 3D calorimetry : eta, phi, Energy
- 4D calorimetry : x,y,z,E
- 5D calorimetry : x,y,z,E,t
  - High granularity=> Millions of channels = > Low power !
    - Power pulsing ~1% for ILC
    - Low power + C02 cooling for CC
  - Energy measurement : Large dynamic range
    - MIP sensitivity => low noise (~0.1 fC)
    - Up to thousands of MIPs (~10 pC)
  - Timing information
    - Nice addition for LC for PID : few ns is enough
    - Crucial for HL-LHC : pileup mitigation, need few tens of ps
  - Embedded electronics vs data out
    - Daisy chain and low power busses for e+e-
    - High speed e/optical links for HL-LHC
  - Radiation levels
    - Negligible at an e+e-
    - Daunting at HL-LHC : >200 Mrad $1^{E}16N$

See talk by Y. Liu





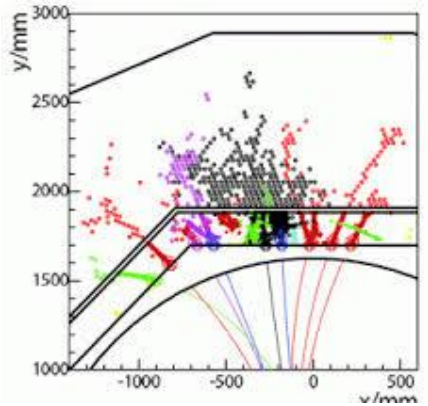


CMS HGCAL ~20mW/ch

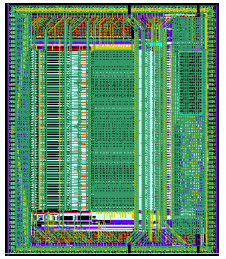
ATLAS LAr FEB ~1W/ch

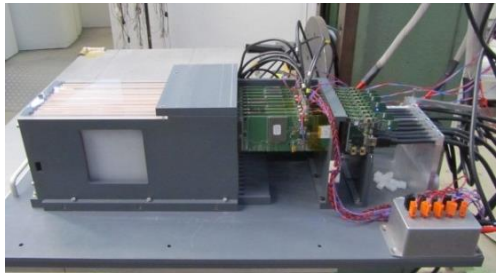
CALICE technological prototypes

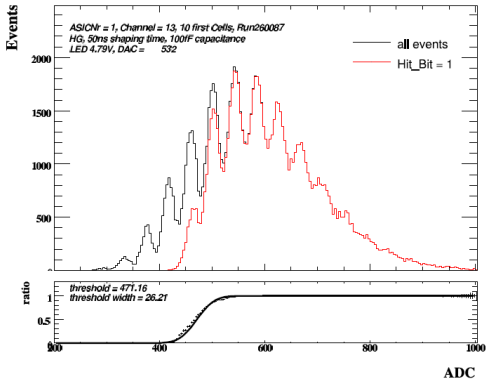
- R&D on imaging calorimetry (2004-2024)
  - Particle Flow Algorithms *[Brient, Videau et al.]*
  - Electronics crucial (low noise, low power, fully integrated)
  - Several innovative features (power pulsing, SiPM…)
  - Validation of technological prototypes
  - Common R/O features
  - Applied to CMS HGCAL



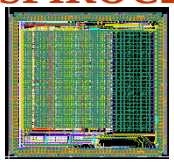
SKIROC2



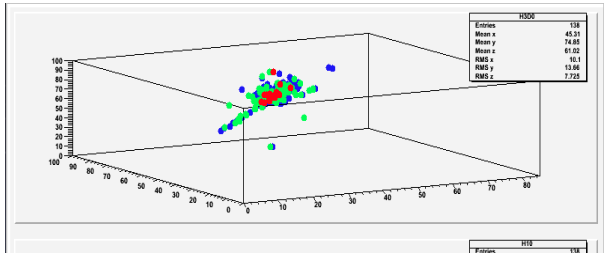




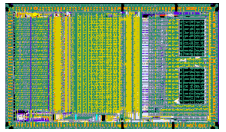
SPIROC2



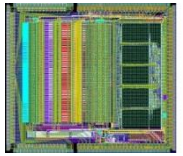
AIDA



HARDROC2



MICROROC



HGCROC (CMS HGCAL)

Overall chip divided in two symmetrical parts

- Each half is made of:
  - 39 channels: 36 channels, 2 common-mode, 1 calibration
  - Bandgap, voltage reference close to the edge
  - Bias, ADC reference, Master TDC in the middle
  - Main digital block and 3 differential outputs (2x Trigger, 1x Data)

Measurements

- Charge
  - ADC (AGH): peak measurement, 10 bits @ 40 MHz, dynamic range defined by preamplifier gain
  - TDC (IRFU): TOT (Time over Threshold), 12 bits (LSB = 50ps)
  - ADC: 0.16 fC binning. TOT: 2.5 fC binning
- Time
  - TDC (IRFU): TOA (Time of Arrival), 10 bits (LSB = 25ps)

Two data flows

- DAQ path
  - 512 depth DRAM (CERN), circular buffer
  - Store the ADC, TOT and TOA data
  - 2 DAQ 1.28 Gbps links (CLPS)
- Trigger path
  - Sum of 4 (9) channels, linearization, compression over 7 bits
  - 4 Trigger 1.28 Gbps links (CLPS)

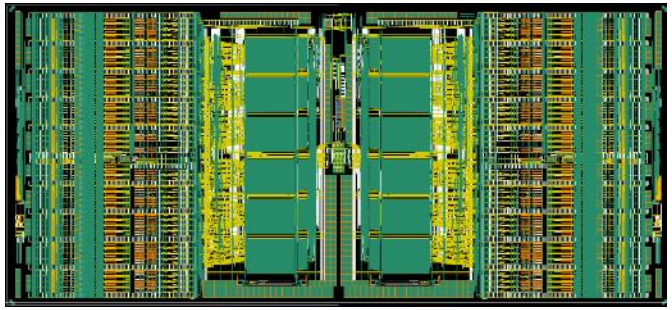
Control

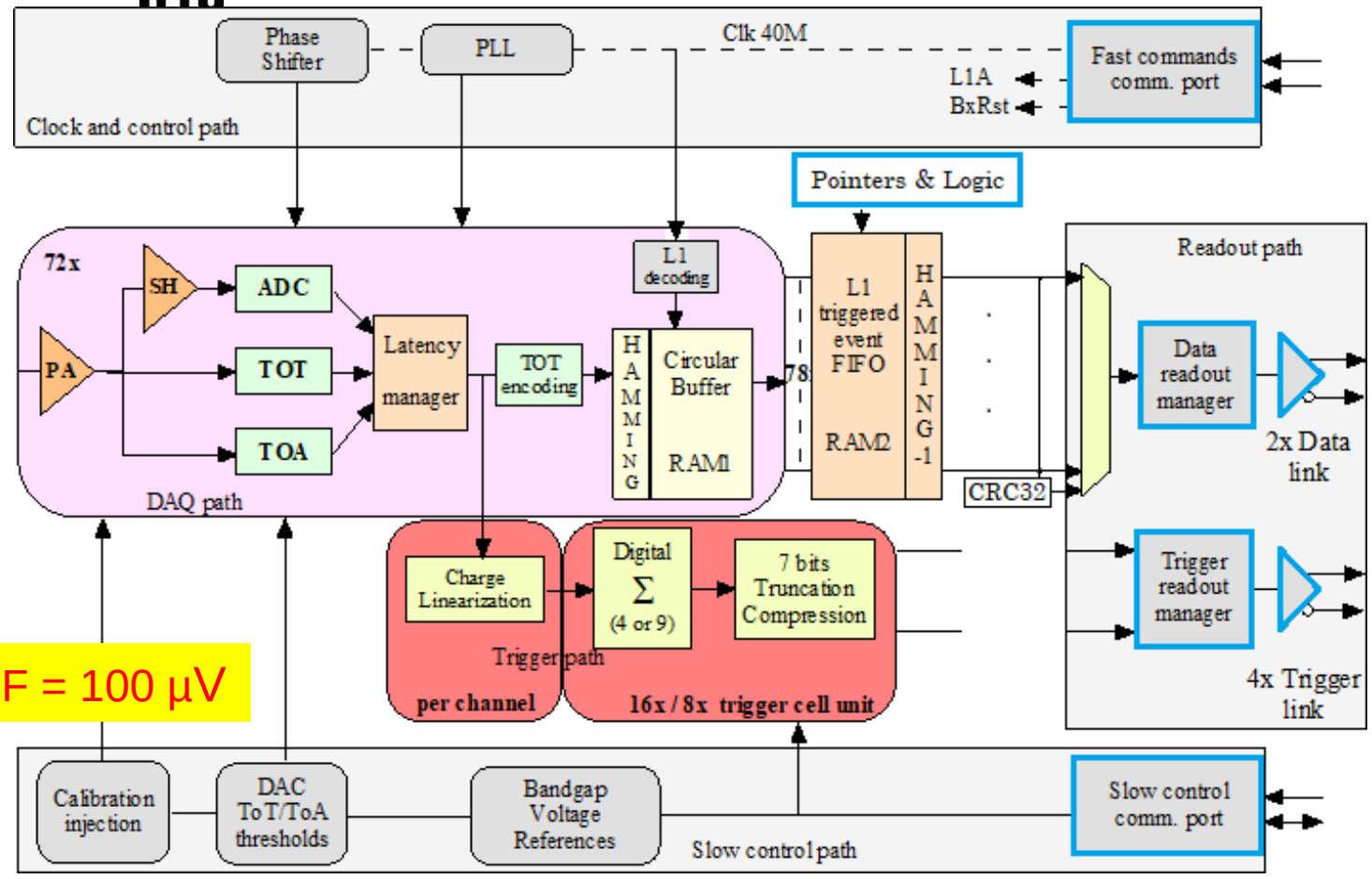
- Fast commands
  - 320 MHz clock and 320 MHz commands
  - A 40 MHz extracted, 5 implemented fast commands
- I2C protocol for slow control

Ancillary blocks

- Bandgap (CERN)
- 10-bits DAC for reference setting
- 11-bits Calibration DAC for characterization and calibration
- PLL (IRFU)
- Adjustable phase for mixed domain

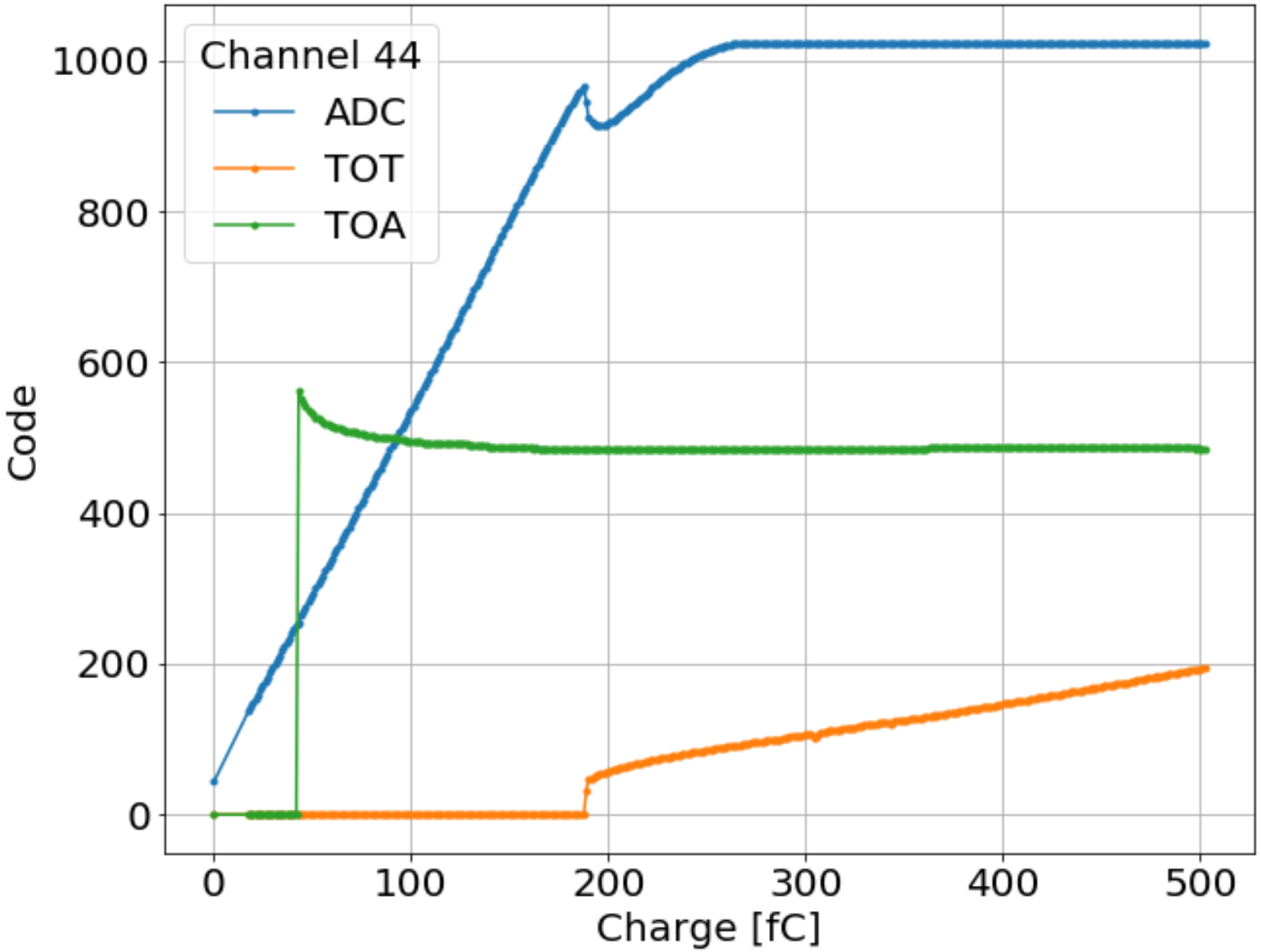
$Q_{MIP}/Cd \sim 3\ fC/30\ pF = 100\ \mu V$



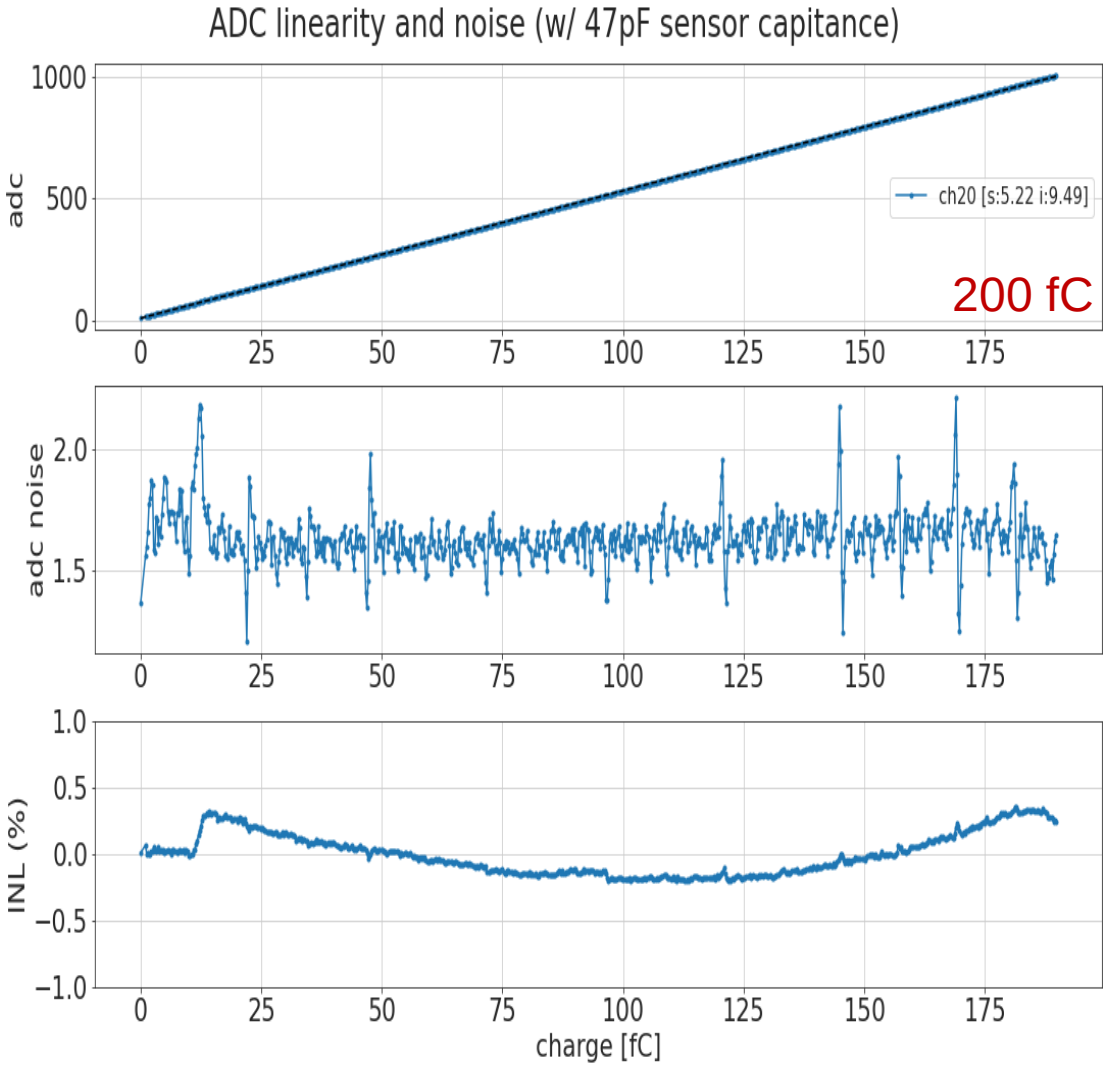


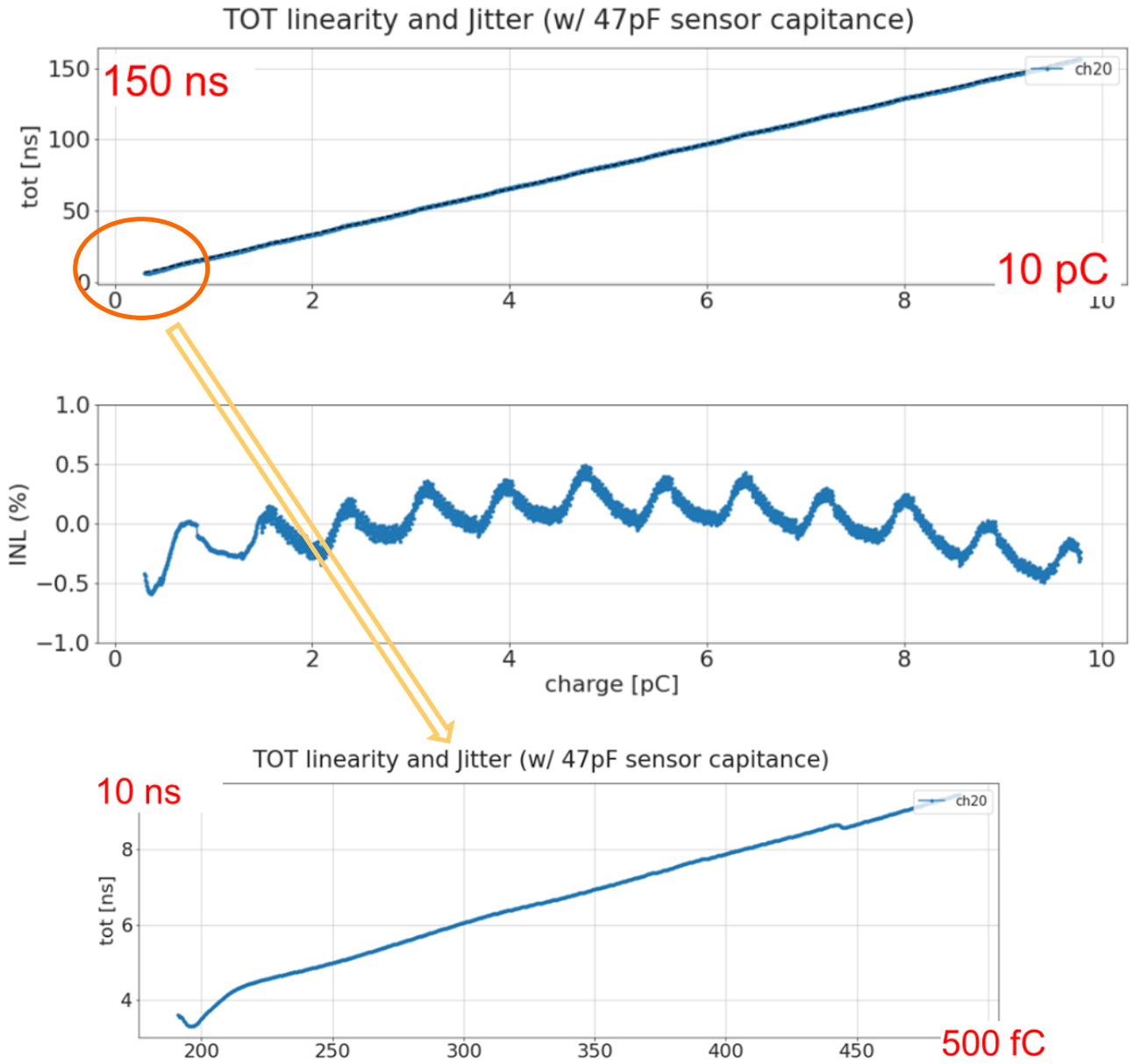
Handling the dynamic range : ADC and TOT

- ADC range 0 - 200 fC
- TOT range 200 fC - 10 pC
- Non-linear inter-region
- But 200 ns dead time



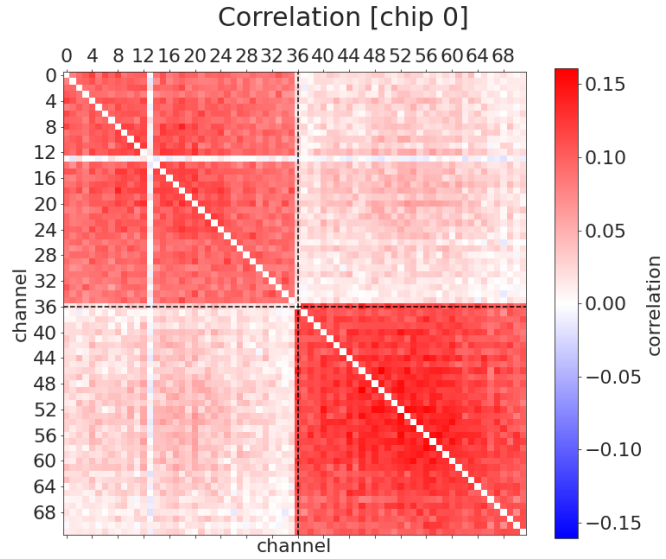
Performance : charge measurement



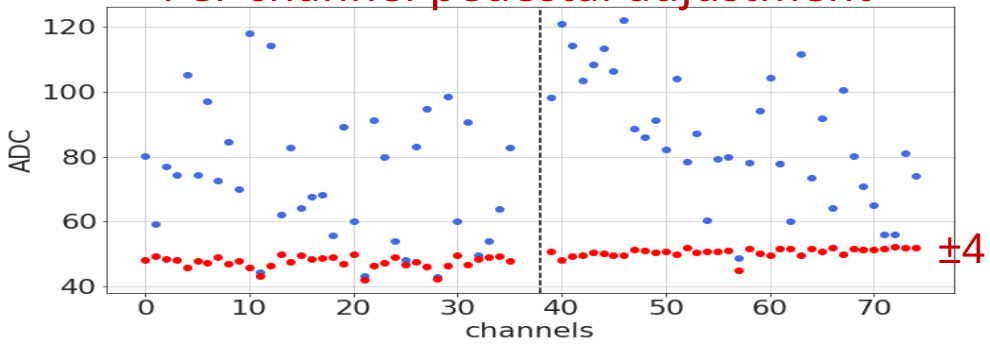


HGCROC3: Noise and pedestal measurements

- Measured noise with 47 pF input cap = 0.3 fC (~ 2000 e-) (0.7 nV / √Hz)
- Very low correlated noise contribution: max 15%
  - Comparable with HGCROC2 even if the digital activity was doubled
- ADC pedestal adjustment done manually with local 6b DAC

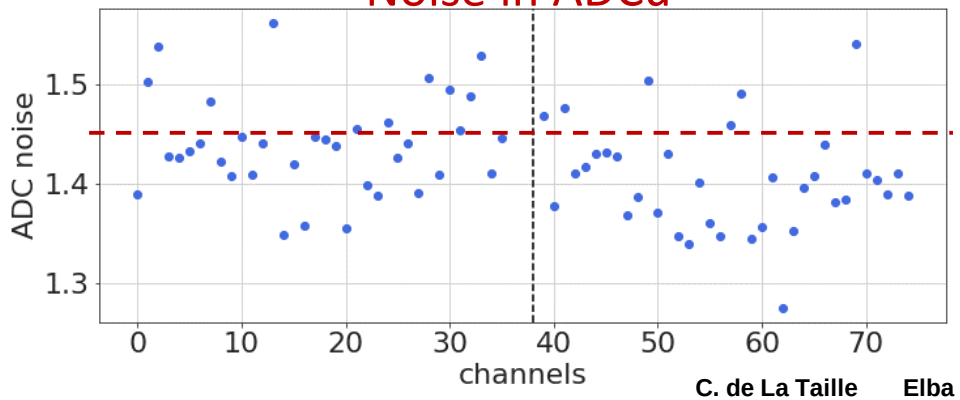


Per channel pedestal adjustment



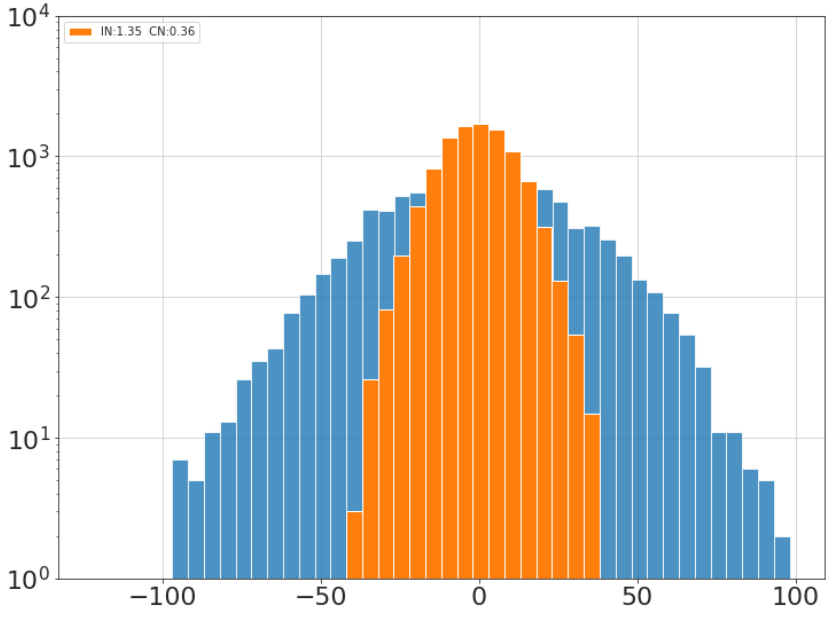
±4 ADCu

Noise in ADCu



~0.3 fC

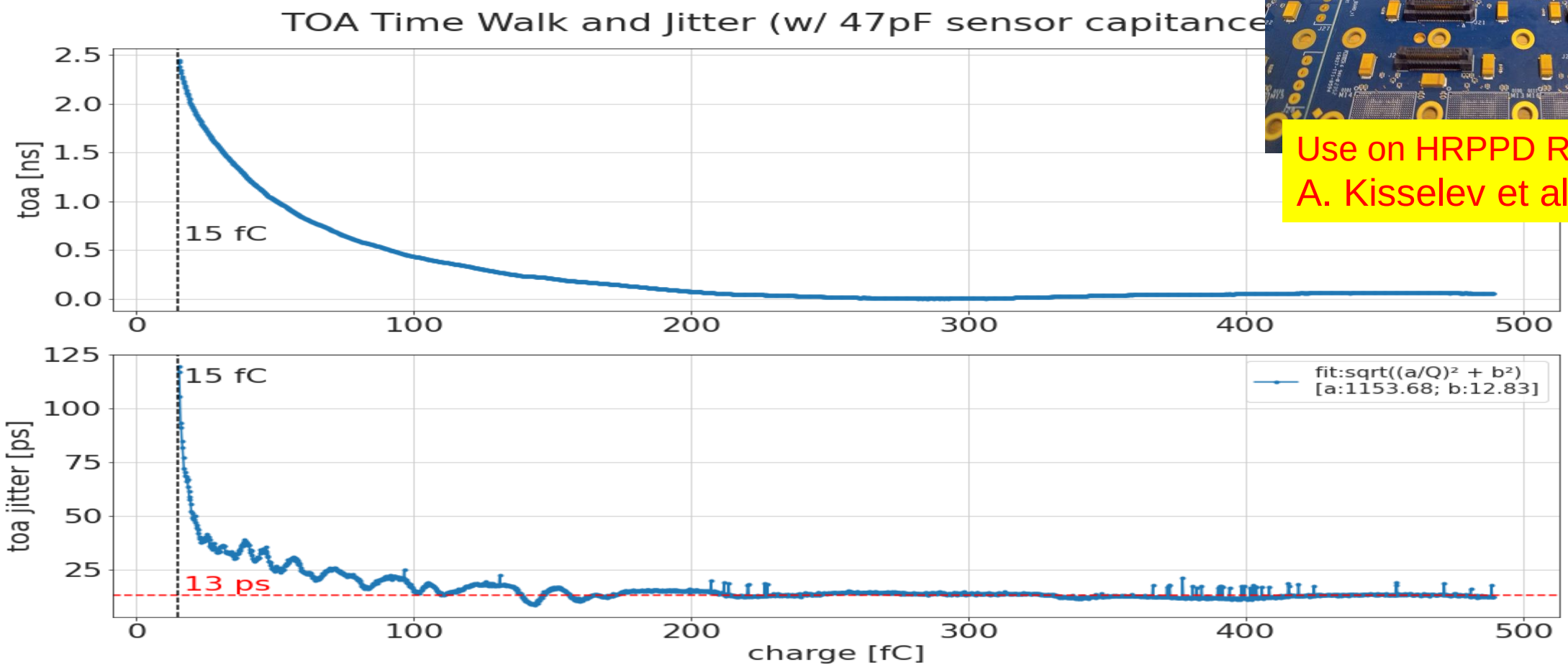
Full chip (72 channels)



Zoom on timing

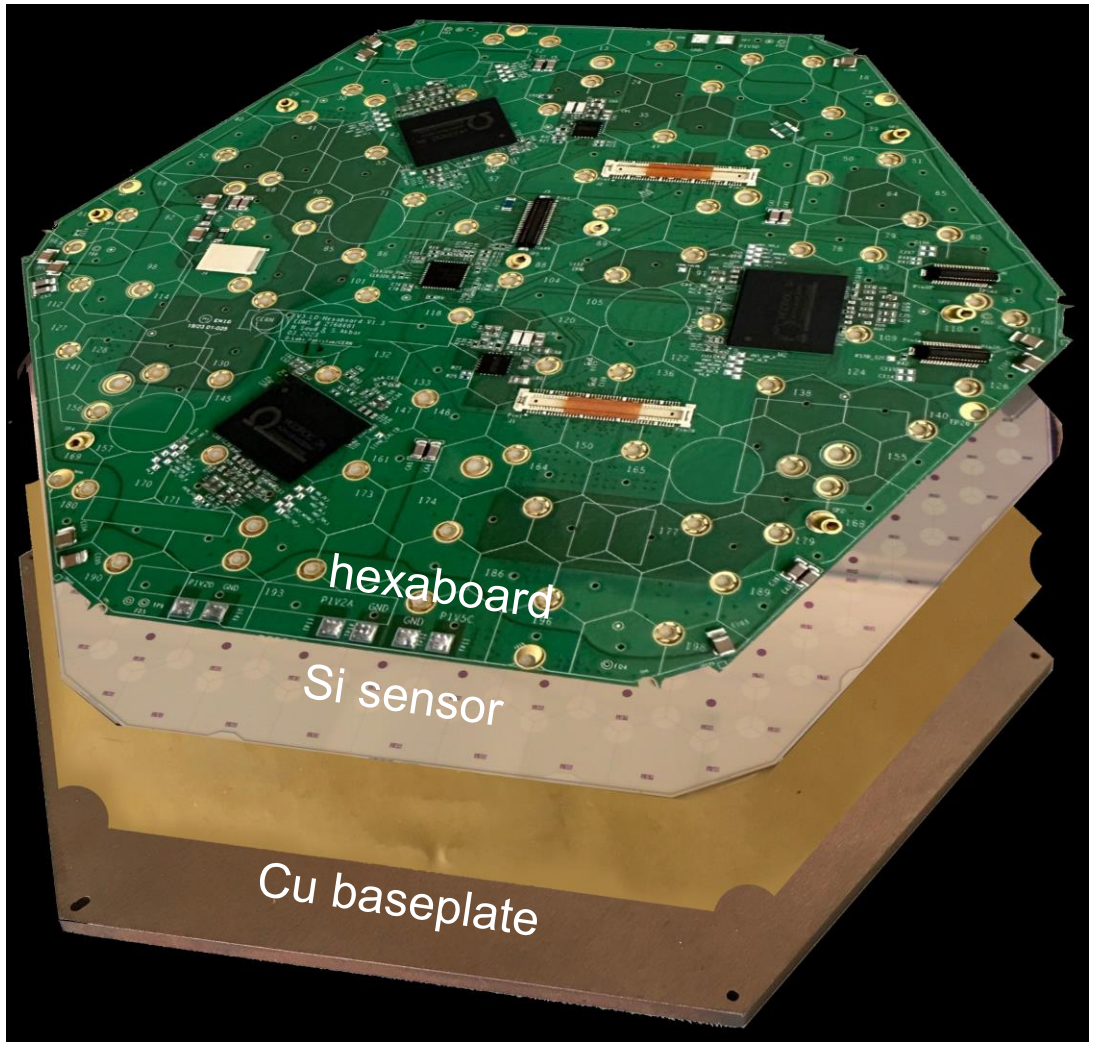
- ~2.5 ns time walk, 13 ps jitter for Q>100fC at Cd = 47 pF
- Fits also well MCPs for PID @EIC (HRPPD)

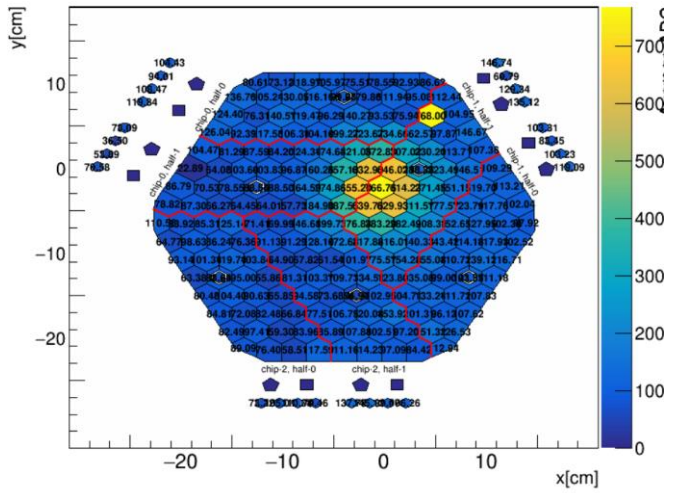
Use on HRPPD RICH @EIC
A. Kisselev et al (BNL)

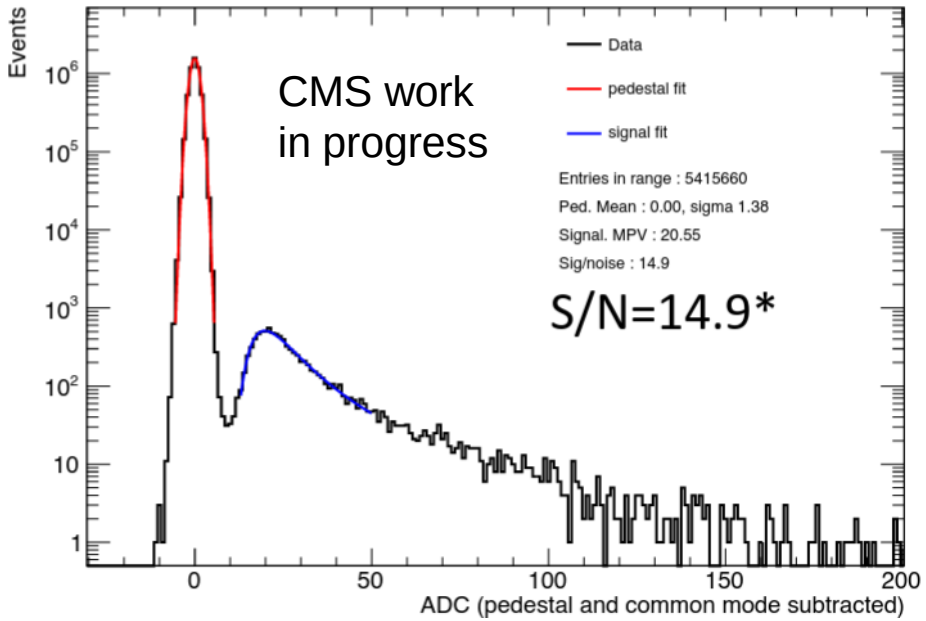


HGCAL modules

- Good performance in test beam

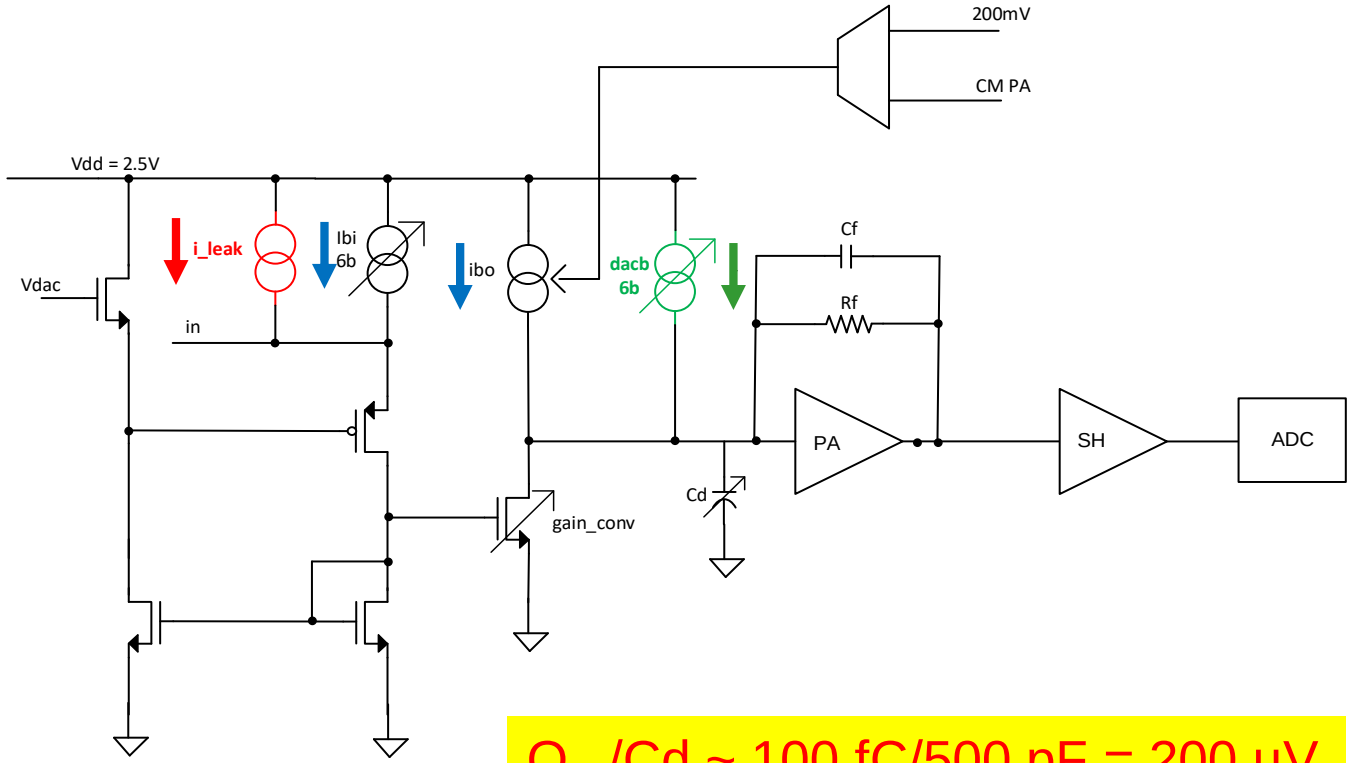




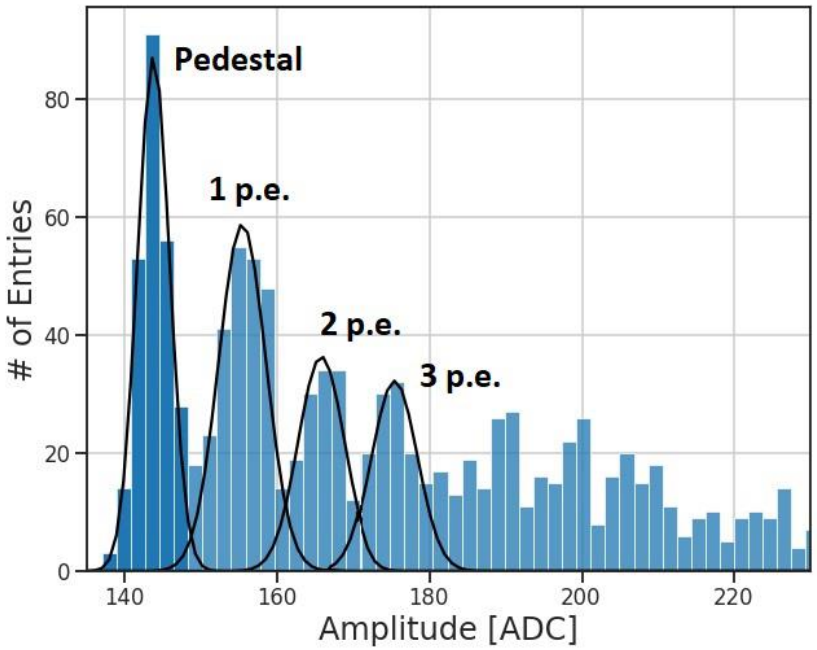


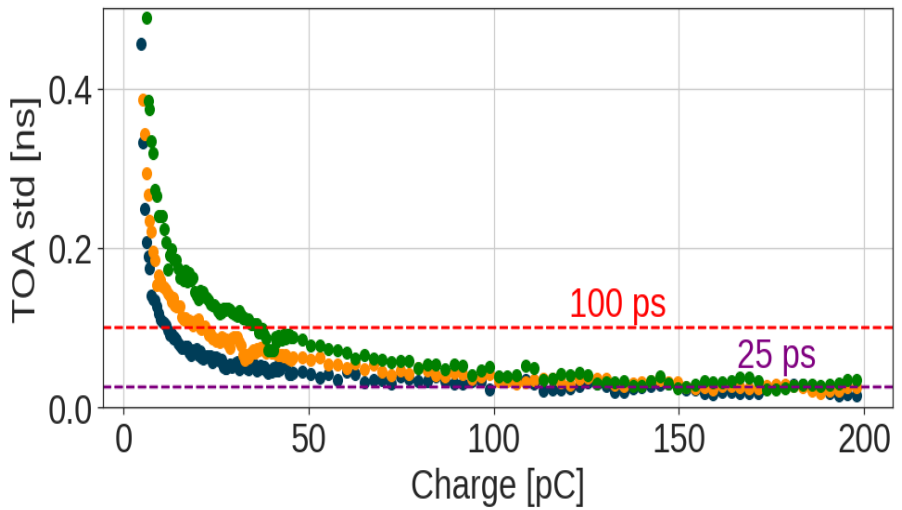
H2GCROC: SiPM version current conveyor

- **Current conveyor (Heidelberg design) to adapt to Si version**
- **Dynamic range : 50 fC – 300 pC**
- **2 typical gains**
  - Low gain (Physics mode): **44 fC/ADC gain, 50 fC noise (1.25 ADCu)**
  - High gain (Calibration mode): **10 fC/ADC gain, 20 fC noise (2 ADCu)**
- **Measurements in backup slides**



Q_{pe}/Cd ~ 100 fC/500 pF = 200 µV





R&D for calorimetry at future experiments (DRD6)

Name	Track	Active media	readout
LAr	2	LAr	cold/warm elx"HGCROC/CALICElike ASICs"
ScintCal	3	several	SiPM
Cryogenic DBD	3	several	TES/KID/NTL
HGCC	3	Crystal	SiPM
MaxInfo	3	Crystals	SIPM
Crilin	3	PbF2	UV-SiPM
DSC	3	PBbGlass+PbW04	SiPM
ADRIANO3	3	Heavy Glass, Plastic Scint, RPC	SIPM
FiberDR	3	Scint+Cher Fibres	PMT/SiPM,timing via CAENFERS, AARDVARC-v3,DRS
SpaCal	3	scint fibres	PMT/SiPMSPIDER ASIC for timing
Radical	3	Lyso:CE, WLS	SiPM
Grainita	3	BGO, ZnWO4	SiPM
TileHCal	3	organic scnt. tiles	SiPM
GlassScintTile	1	SciGlass	SiPM
Scint-Strip	1	Scint.Strips	SiPM
T-SDHCAL	1	GRPC	pad boards
MPGD-Calo	1	muRWELL,MMegas	pad boards(FATIC ASIC/MOSAIC)
Si-W ECAL	1	Silicon sensors	direct withdedicated ASICS (SKIROCN)
Si/GaAS-W ECAL	1	Silicon/GaAS	direct withdedicated ASICS (FLAME, FLAXE)
DECAL	1	CMOS/MAPS	Sensor=ASIC
AHCAL	1	Scint. Tiles	SiPM
MODE	4	-	-
Common RO ASIC	4	-	common R/O ASIC Si/SiPM/Lar

See talk by T. Bergauer

Trends for calorimeter readout

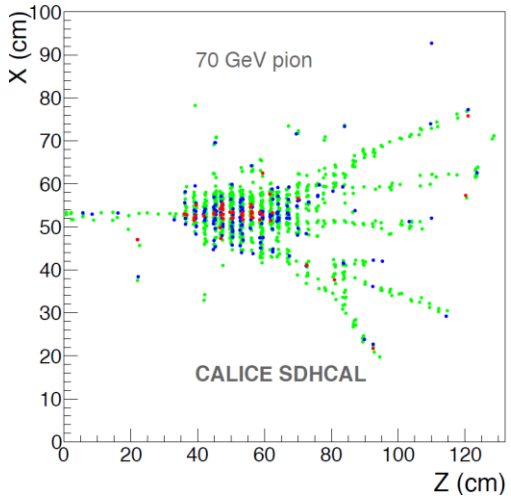
- On-detector embedded electronics, low-power multi-channel ASICs
  - CALICE SKI/SPI/HARDROC, FLAME, CMS HGCROC, FCC LAr, FATIC…
  - Challenges : #channels, low power, digital noise, data reduction
- Off-detector electronics : fiber/crystal readout
  - Wavefrom samplers : DRS, Nalu AARD, LHCb spider…
  - Challenges : low power, data reduction
- Digital calorimetry : MAPs, RPCs…
  - DECAL, ALICE FOCAL, CALICE SDHCAL
  - MAPS for em CAL : eg ALPIDE ASIC for FOCAL, DECAL…
  - Challenges : #channels, low power, data reduction

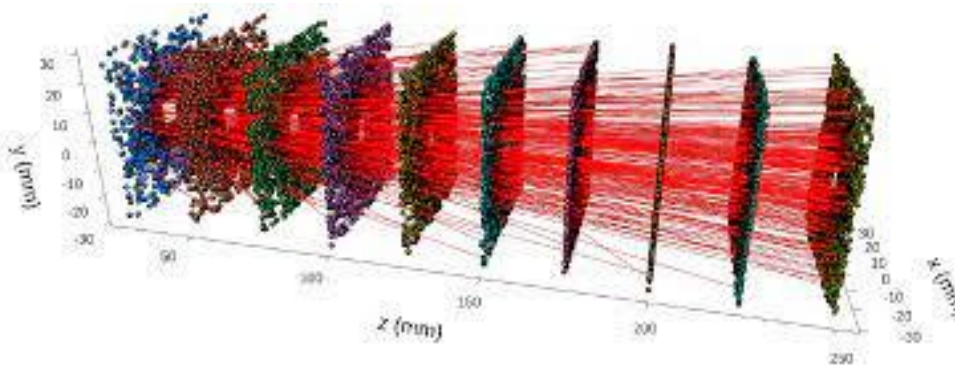
Digital calorimetry

- Hadronic : e.g. CALICE RPCs or µmegas
  - ~1 cm² pixels, low occupancy, ~1 mW/cm² (unpulsed)
  - Performance improvement with semi-digital architecture
  - Timing capability can be added

- Electromagnetic : e.g. DECAL, ALICE FOCAL…
  - Based on ALPIDE : (30µm)² pixels, high occupancy, ~ 100 mW/cm², slow
  - To be compared with embedded electronics ~10 mW/cm²
  - Most power in digital processing => would benefit a lot from ≤ 28 nm node
  - Semi-digital and/or larger pixels couldl be an interesting study

- Upcoming R&D
  - Power reduction, dead area minimization
  - Coping with high occupancy, managing data bandwidth



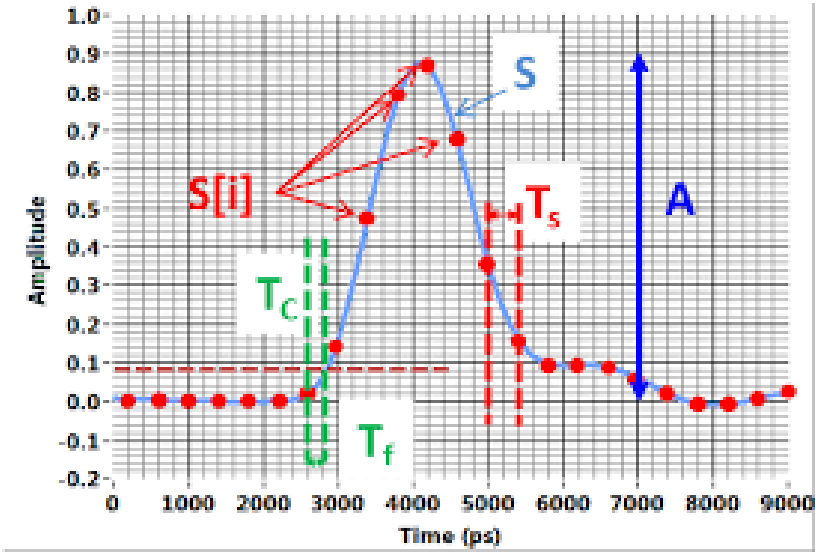


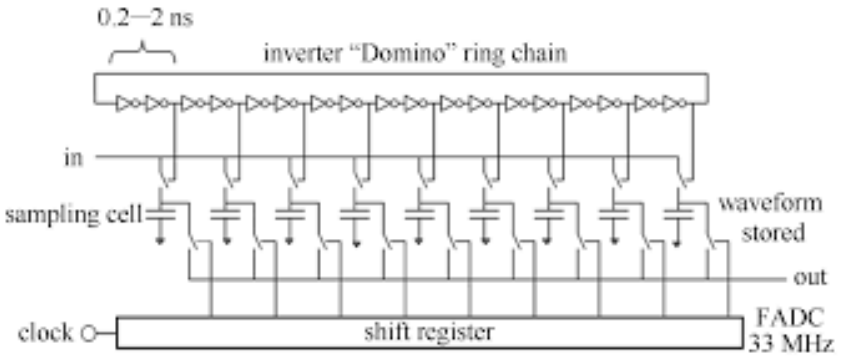
Waveform sampling

- Switched capacitor arrays (DRS4, Nalu, SPIDER…)
  - Pulse shape analysis
  - High accurcay timing, digital CFD
  - Sizeable power to provide GHz BW on large capacitance
  - large data volume

- Often used in off-detector electronics
  - Space and cooling available
  - Small/medium size detector readout and/or characterization
  - See LHCb calorimeter upgrade

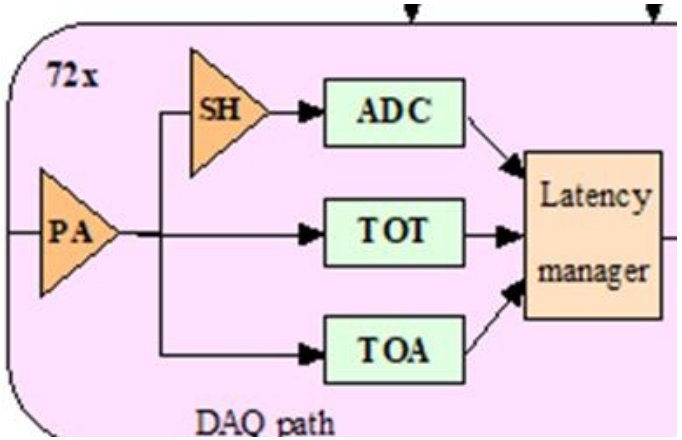
- Upcoming R&D
  - Power reduction, Front-end integration
  - Data bandwitdth
  - Time walk correction, potentially best for ps accuracy



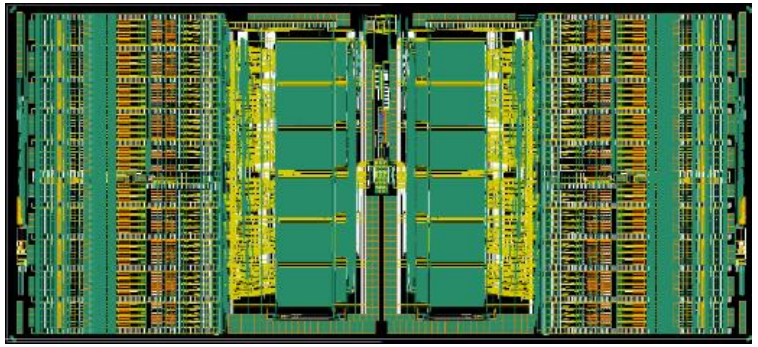


Embedded ASICs

- Pioneered with CALICE R&D (SKIROC, SPIROC..)



- Multi-channel charge/time readout
  - Fast preamp
    - Full dynamic range. Possible extension with ToT
  - Fast path for time measurement (ToA)
    - High speed discriminator and TDC
    - Time walk correction with ADC (or ToT)
  - Slow path for charge measurement
    - ~10 bit ADC ~40 MHz
  - Low power for on-detector implementation (~10 mW/ch) e.g. CMS HGCAL



- Upcoming R&D
  - Power reduction,
  - Auto-trigger, Data-driven readout

Evolution of embedded calorimeter readout chips

- Further reduction in power dissipation
- Auto-trigger and data-driven readout
- More SiPM readout
- Addressed in DRD6 proposal

DRD6 Common readout ASICs proposal [AGH, Omega, Saclay]

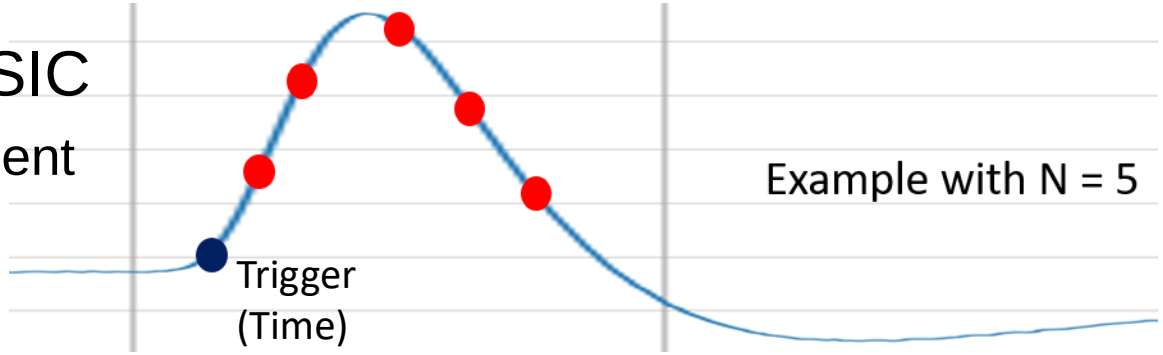
- Develop readout ASIC family for DRD6 prototype characterization
  - Inspired from CALICE SKIROC/SPIROC/HARDROC/MICROROC family
  - Targeting future experiments as mentionned in ICFA document (EIC, FCC, ILC, CEPC…)
  - Addressing embedded electronics and detector/electronics coexistence + joint optimization
  - Detector specific front-end but common backend

  ⇒ allows common DAQ and facilitates combined testbeam

- Start from HGCROC / HKROC : Si and SiPM
  - Reduce power from 15 mW/ch to few mW/ch. Lower occupancy, slower speed
  - Allows better granularity or LAr operation
  - Remove HL-LHC-specific digital part and provide flexible auto-triggered data payload
  - Extend to MCPs (PID) or HRPPD. First tests with EIC calo/PID

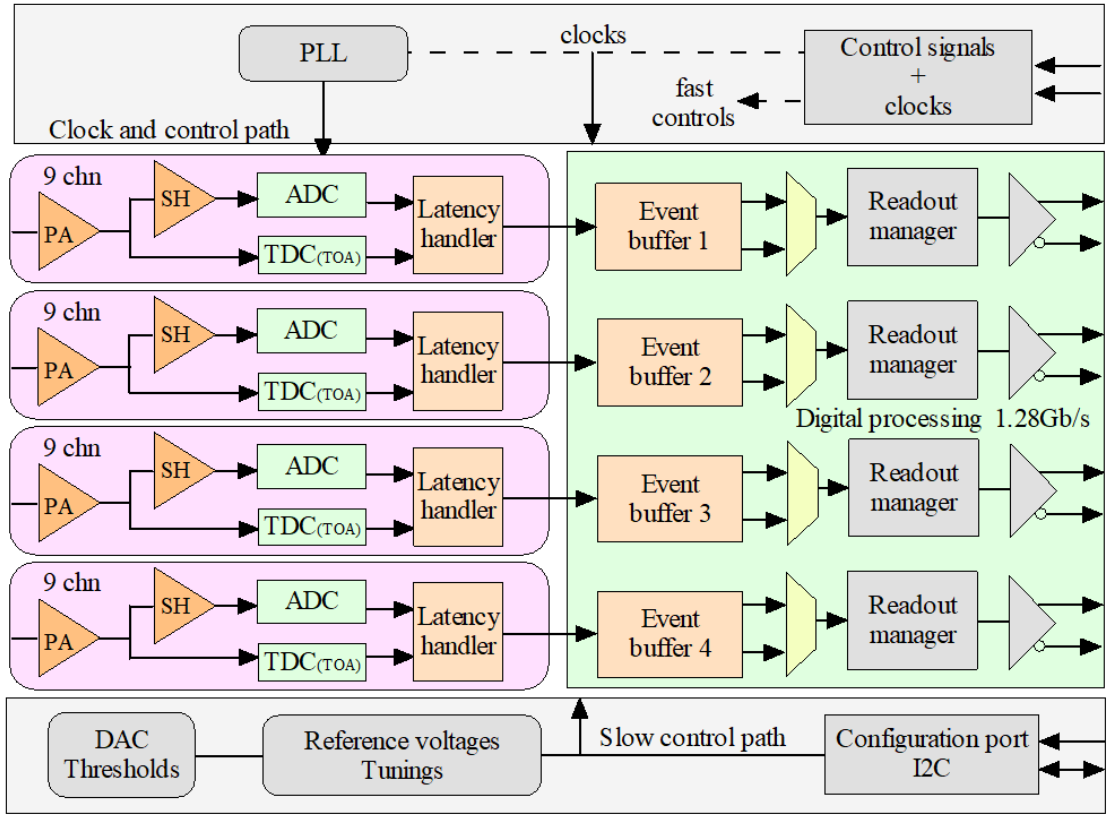
HKROC: (slow) waveform digitizer with TDC and auto-trigger

- HKROC is a charge/time measurement ASIC
  - Intended for PMTs readout at neutrino experiment
  - Slow channel (30 ns) for charge measurement
    - waveform digitizer working @ 40 MHz
    - Number of charge sampling points from 1 to 7
  - Fast channel for precise timing (25 ps binning)



- Auto-trigger on single photoelectron
  - 4 outputs at 1.28 Gb/s
  - Data-driven readout (ch#,ADC,TDC)
  - Hit rate capability up to 0.4MHz/PMT

- Measurement results in backup

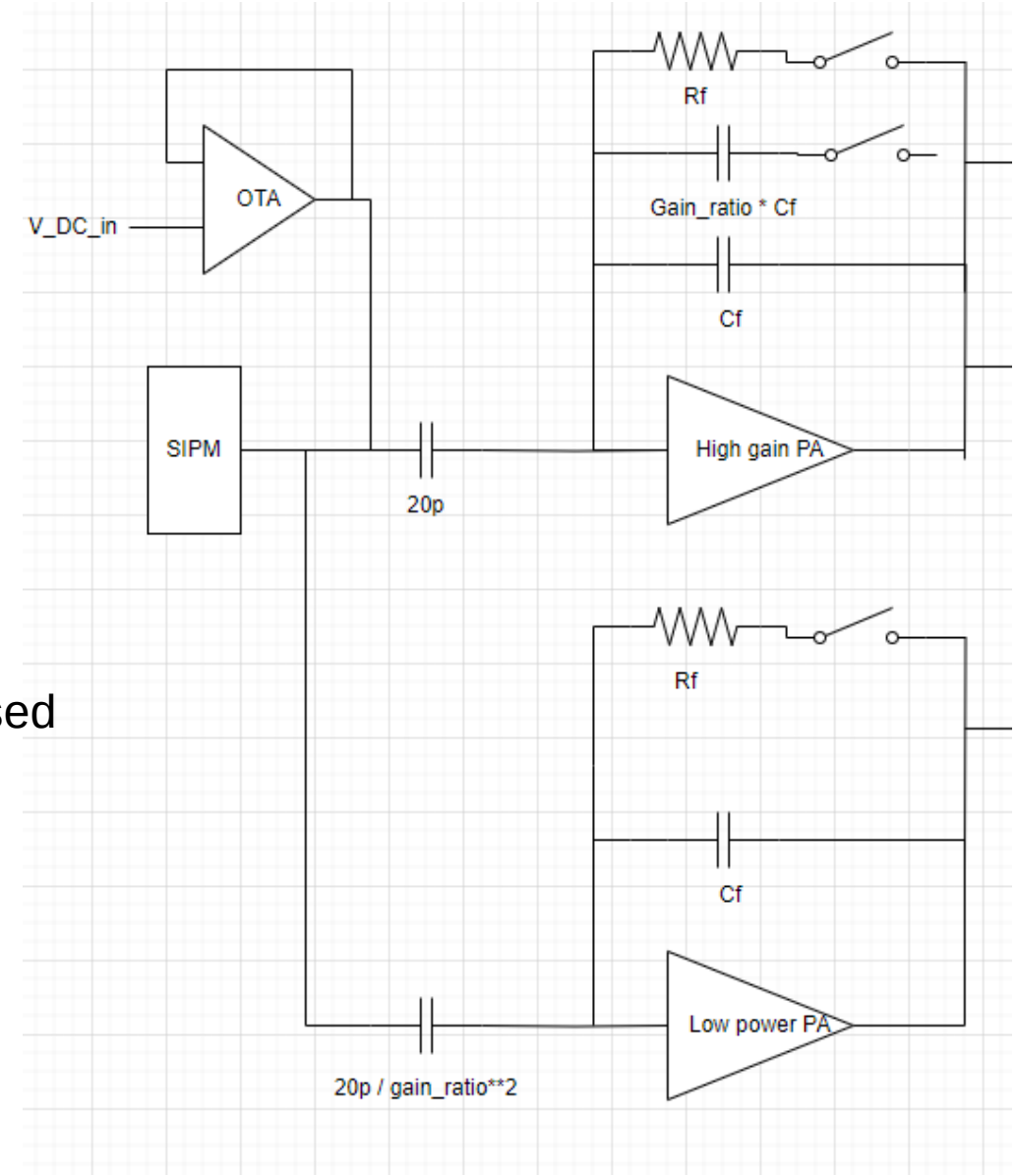


Further steps : CALOROC

- SiPM readout calorimetry : CMS H2GCROC with EIC readout (200 MHz clock and fast commands)
  - SiPM from 500 pF to 2.5 nF (or 10 nF)
  - ~5-10 mW/channel

- 2 versions : conservative and exploratory
  - Conservative : uses H2GCROC (ADC, TOT) as it is and replaces the backend
  - Exploratory : new analog part (dynamic gain switching).
  - Pin to pin compatible
  - Backend « à la HKROC » : auto-triggered, zero-suppressed
  - 40 MHz internal clocking (ADC, TDCs)

- Could fit FCC SiPM calorimeters
- A Si version would fit FCC Si calorimeter

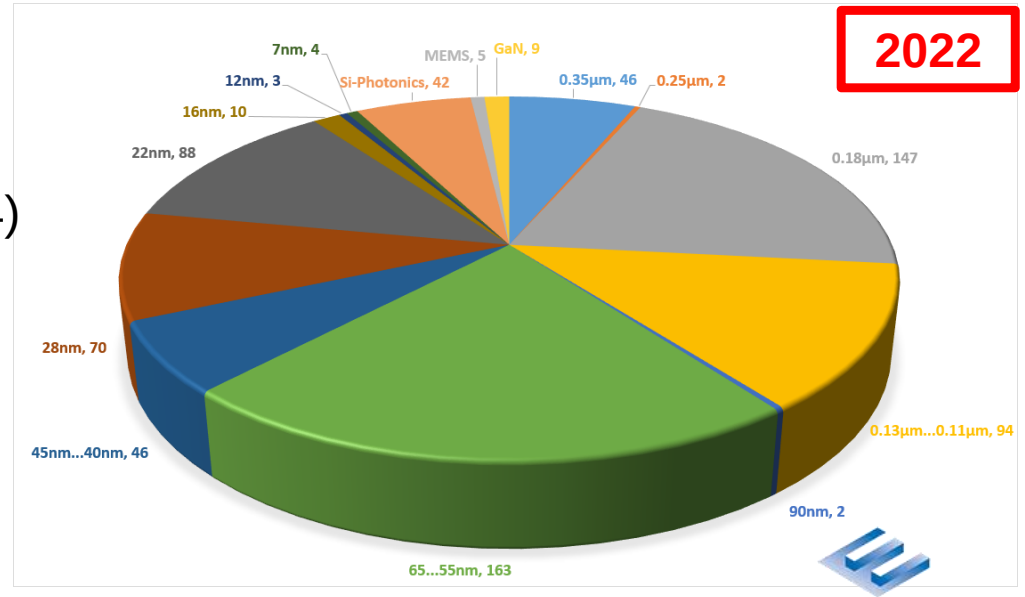


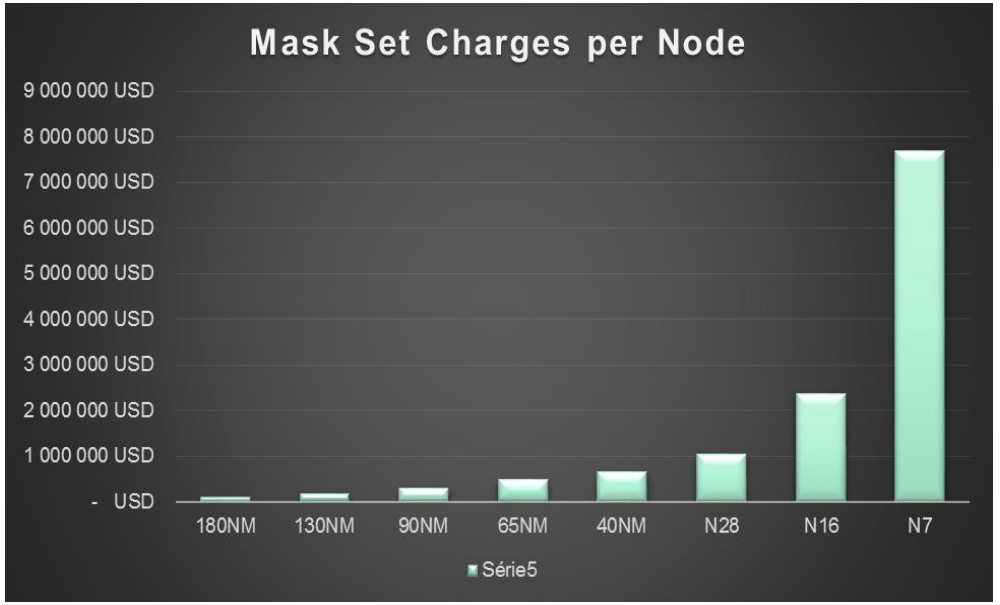
Technology choice for mixed signal ASICs

- TSMC 130nm : mixed signal, cheap
  - Very mature technology with good analog performance
  - 2.5 k€/mm² MPW, 300-350 k€/engineering run (20 wafers C4)
  - Perenity ?

- TSMC 65 nm : mixed signal, main stream
  - ~2-3 times lower power in digital, similar in the analog (compared to 130n)
  - 5 k€/mm², 700-800 k€/ engineering run

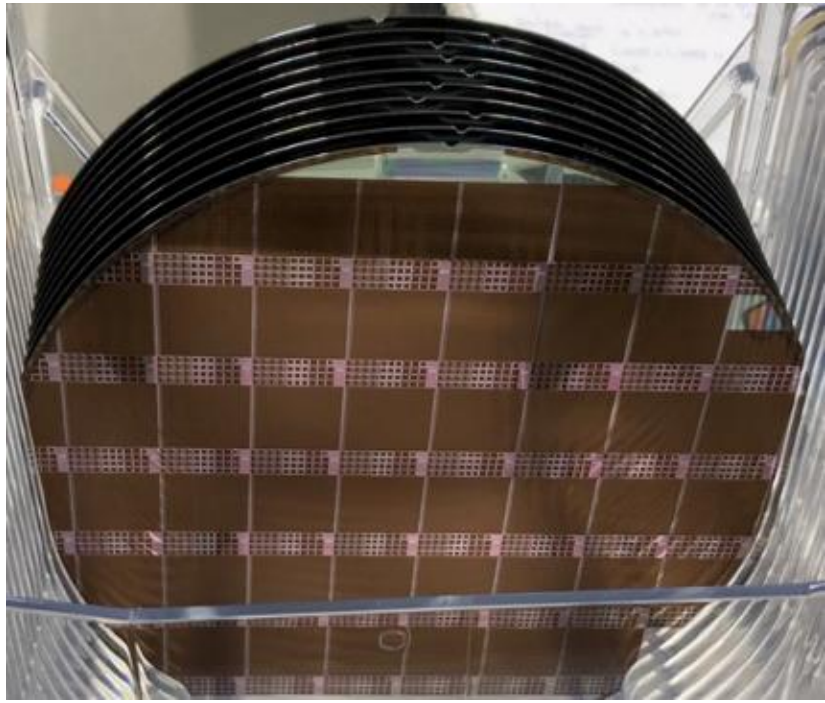
- TSMC 28 nm : digital oriented
  - High density integration (pixels)
  - High performance, lower power digital, similar in the analog
  - 10 k€/mm², 1-1.5 M€/ eng run





conclusion

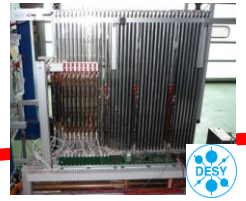
- Importance of joint optimization detector/readout electronics



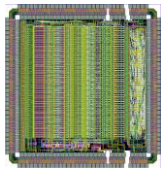
- Trend to reduce power and data volume
  - Pileup will be less of an issue, better granularity will be appreciated !
  - Low occupancy, auto-trigger, data-driven readout
  - Low power ADCs and TDCs (DRD7 with AGH&CEA)
- Picosecond Timing important R&D area
  - PID and/or calorimetry, several new detectors appearing : need R/O
- Next chips at OMEGA will target EIC, DRD1-4-6-7
  - Calorimetry and timing : CALOROC1 and 1A
  - Further R&D needed to bring power down to ~1 mW/ch (Lar)
- Technology choice to be addressed in coordination with other design groups
  - Cost sharing for engineering runs

backup

OMEGA ASICs : overview

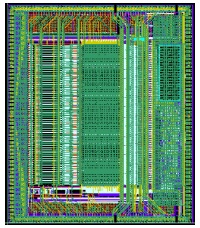


MAROC3

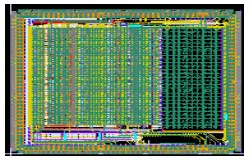


2006

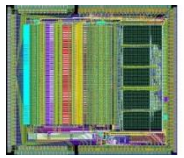
SKIROC



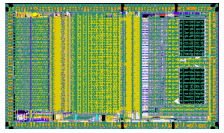
SPIROC



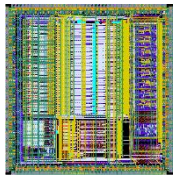
MICROROC



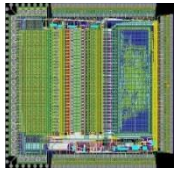
HARDROC



SPACIROC



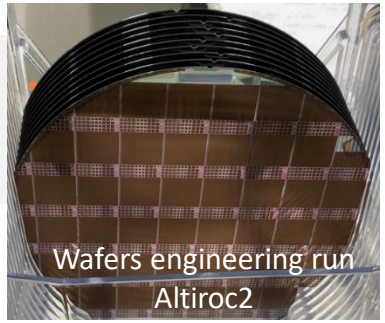
PETIROC



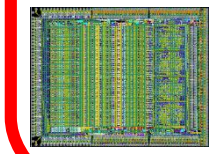
9 engineering runs in 9 years :

AMS SiGe 0,35um 2014, 2016, 2018

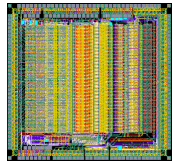
TSMC 130nm: 2019, 2020, 2021, 2022 and 2023 (x2)



TRIROC

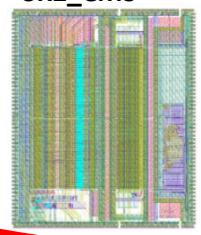


CITIROC

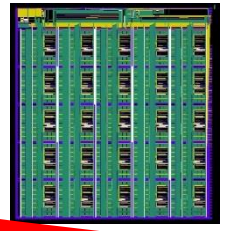


CATIROC

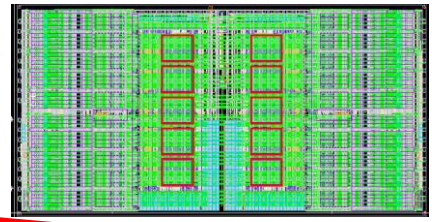
SK2_CMS



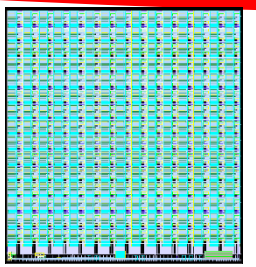
ALTIROC1



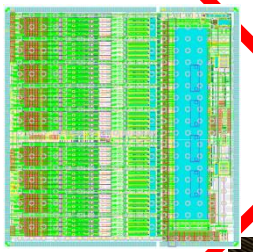
HGCROC



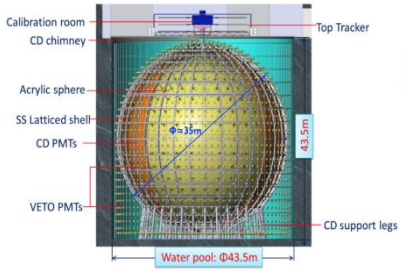
ALTIROC2



HKROC



2023



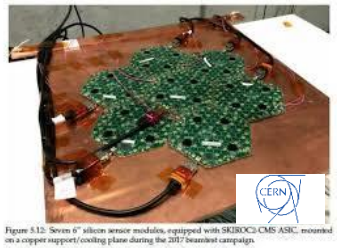
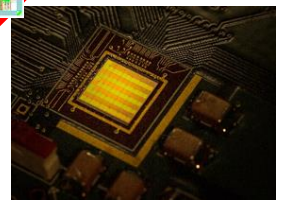


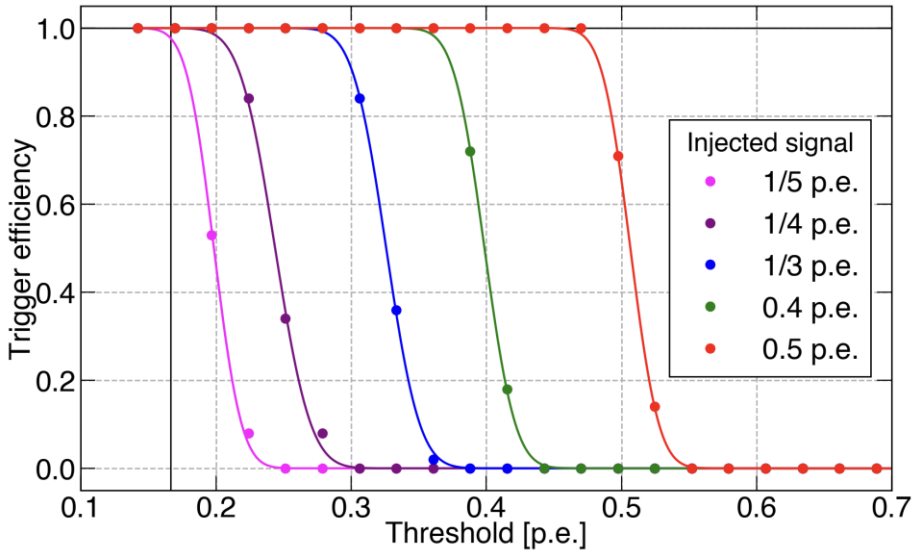
Figure 5.12: Seven 6" silicon sensor modules, equipped with SKIROC2-CMS ASIC, mounted on a copper support/cooling plane during the 2017 beamtest campaign.

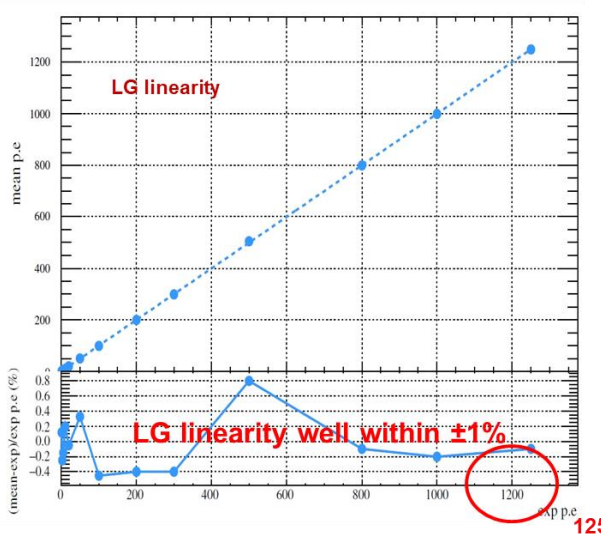
Taille

Elba

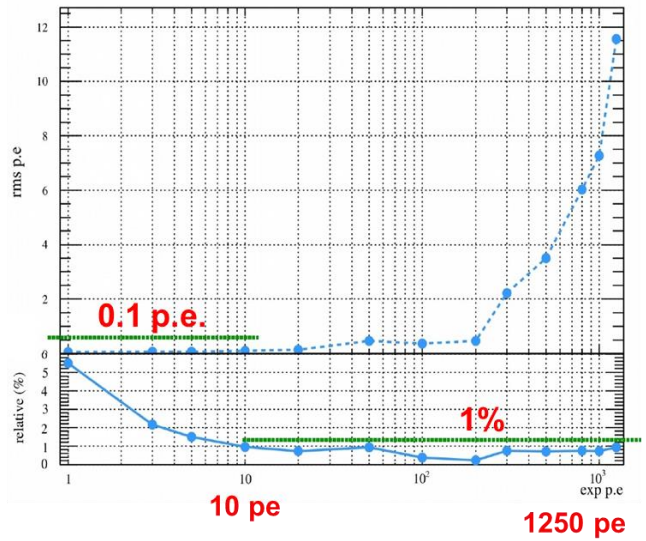


HKROC performance





1250 p.e. = 2500 pC



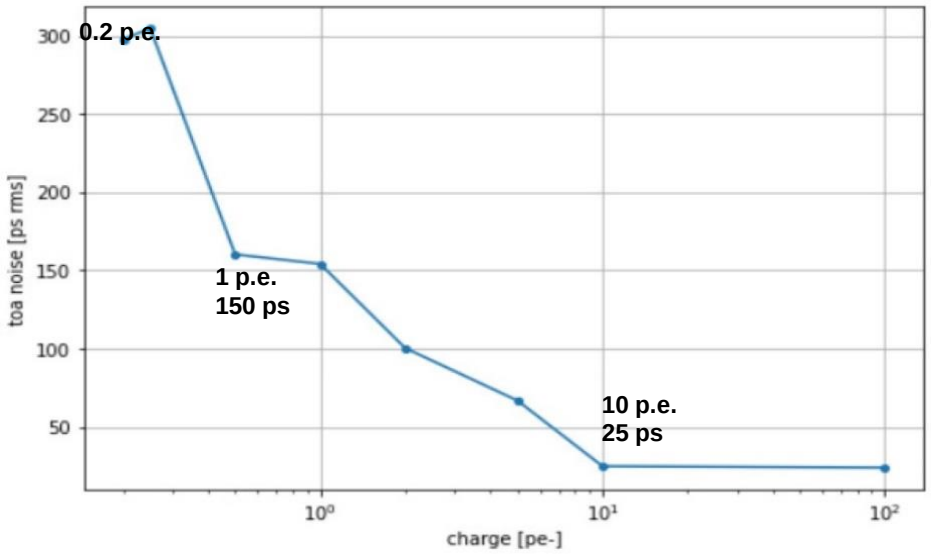
HG, MG and LG tested!!

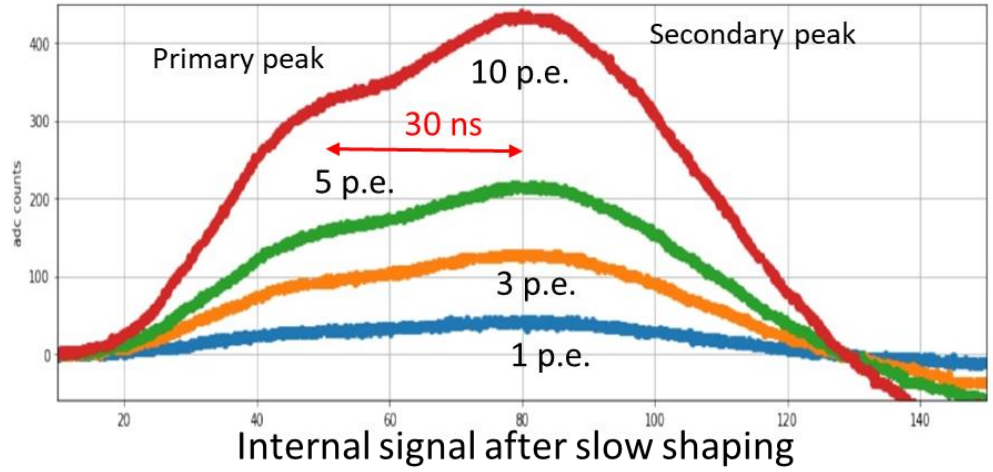
Charge linearity < **±1%** from 1 to **1250 p.e. (2500 pC)**

Charge resolution :

< **0.1 p.e (200 fC)** at ≤ 10 p.e

< 1 % otherwise

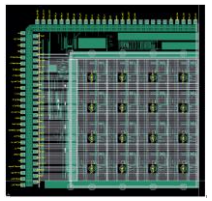


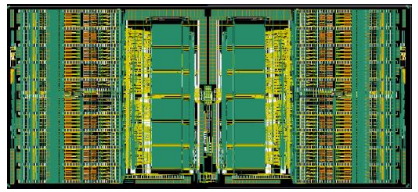


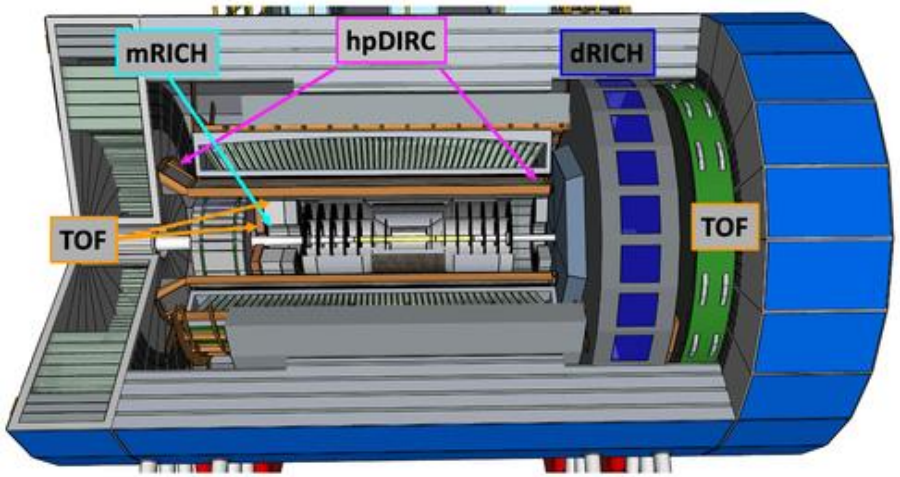
Chips for EIC : electron-ion collider at BNL

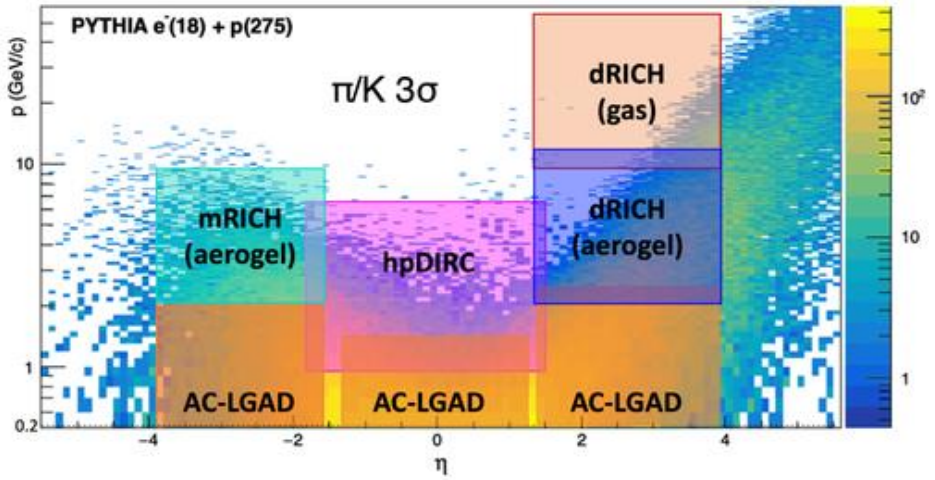
- PID and calorimeters
  - EICROC for AC-LGAD roman pots
  - H(2)GCROC for calorimeters
  - « Event driven » DAQ

Detector Group	Channels			
	MAPS	AC/DC-LGAD	SiPM/PMT	MPGD
Tracking	32 B			100k
Calorimeters	50M		67k	
Far Forward	300M	2.3M	500	
Far Backward		1.8M	700	
PID		3M-50M	600k	
TOTAL	32 B	7.1M-54M	670k	100k
ASIC	ITS-3	EICROC FCFD HPsOC ASROC FAST	Discrete/COTS HGCROC3 ALCOR-EIC	SALSA



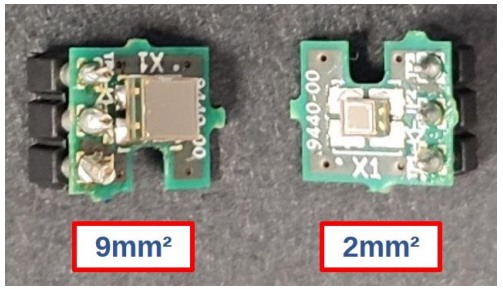


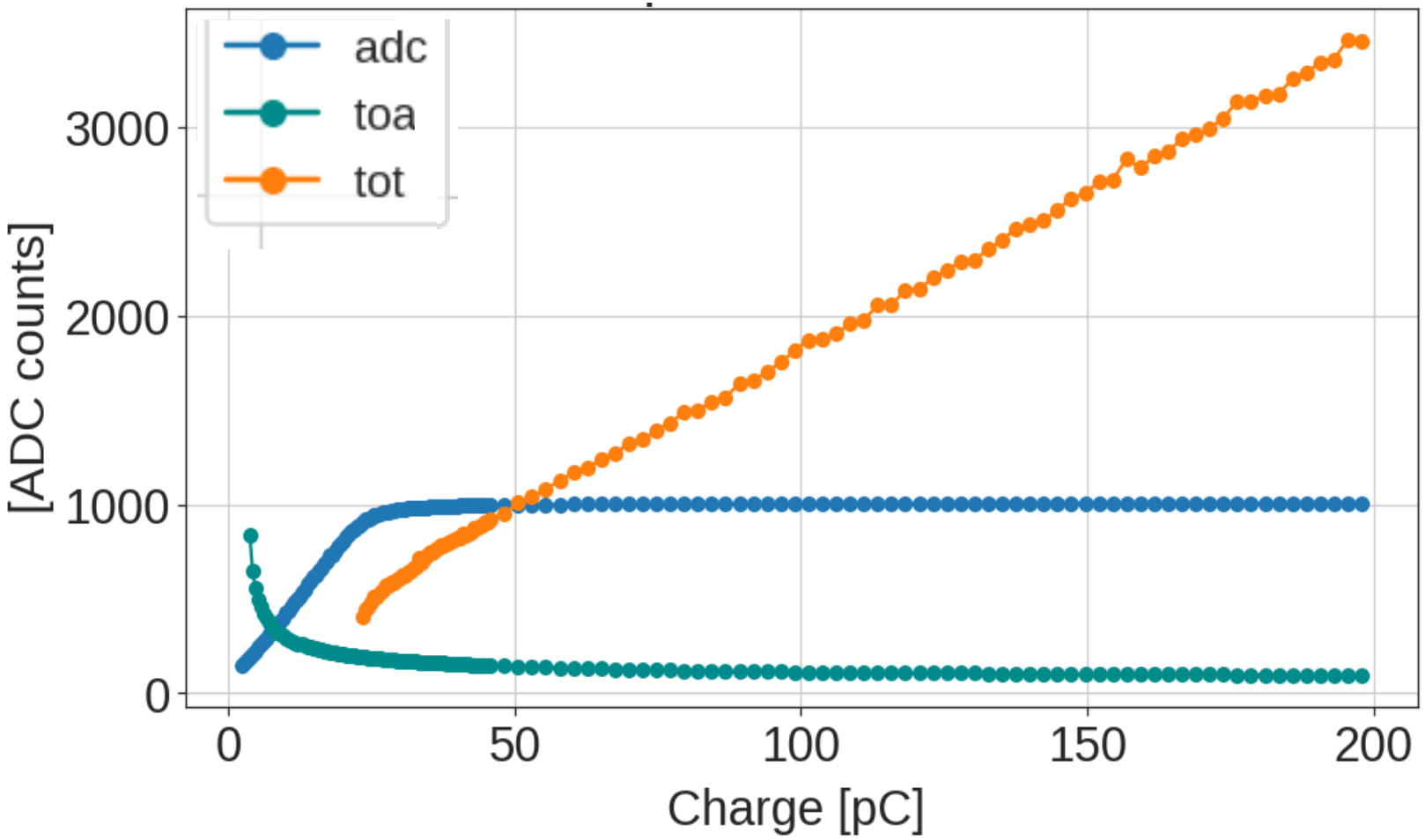




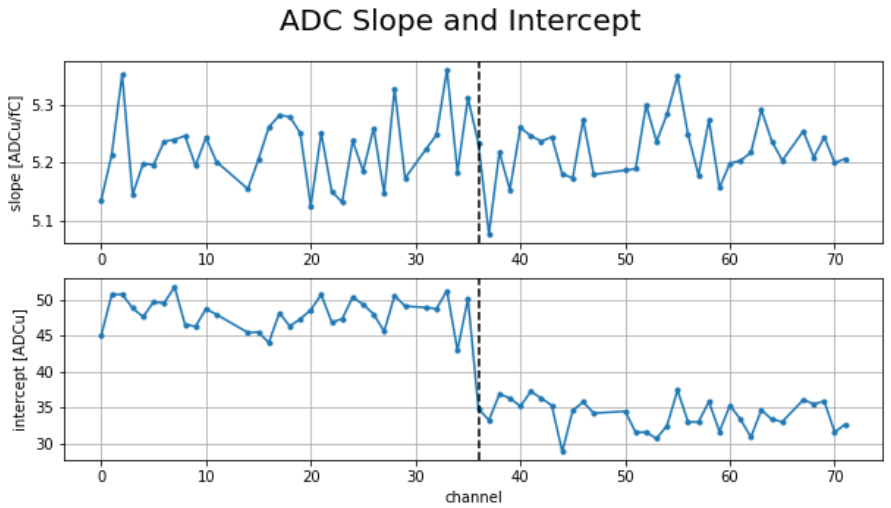
SiPM : ADC and TOT readout

- 16bit dynamic range split in 10 bit ADC and 12 bit ToT
- Tests with 2 sizes of SiPM : 2mm² (120 pF) and 9 mm² (560 pF)

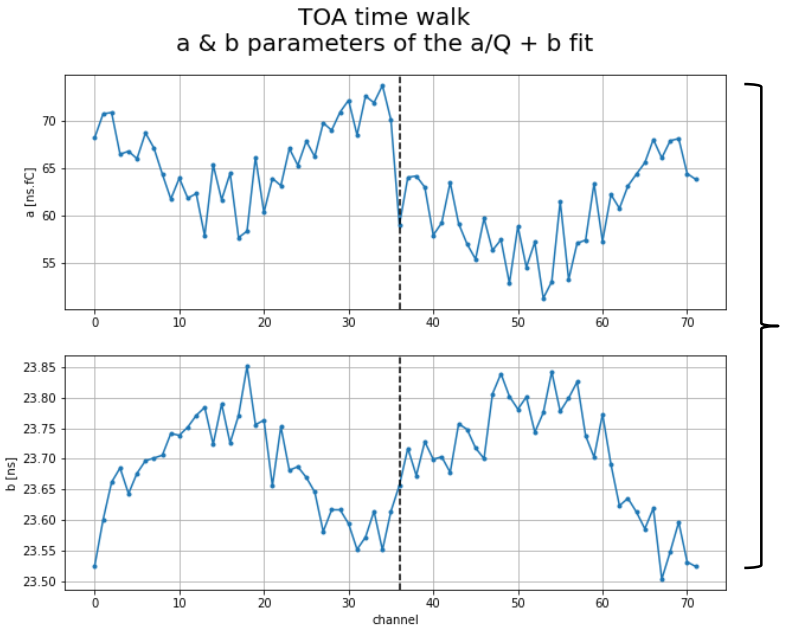




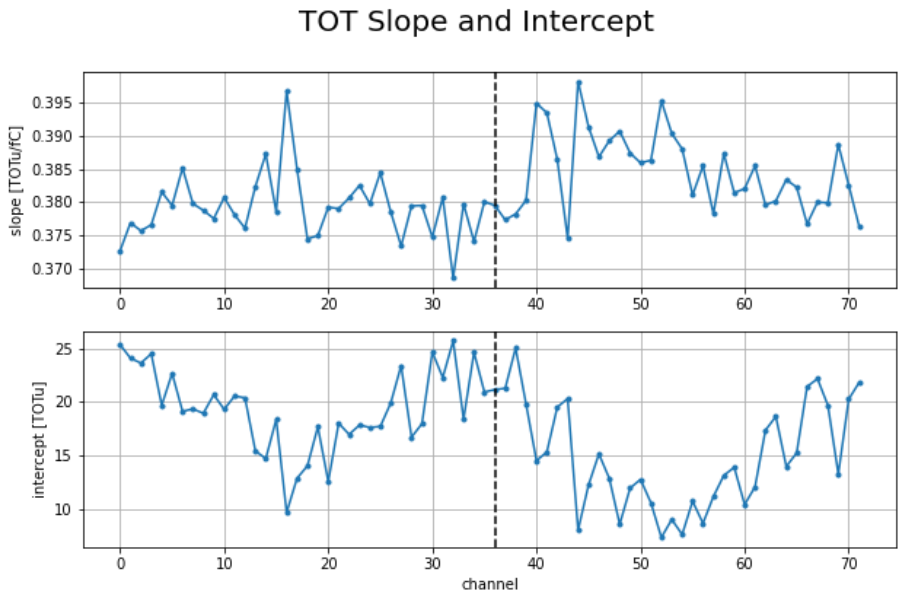
Uniformity



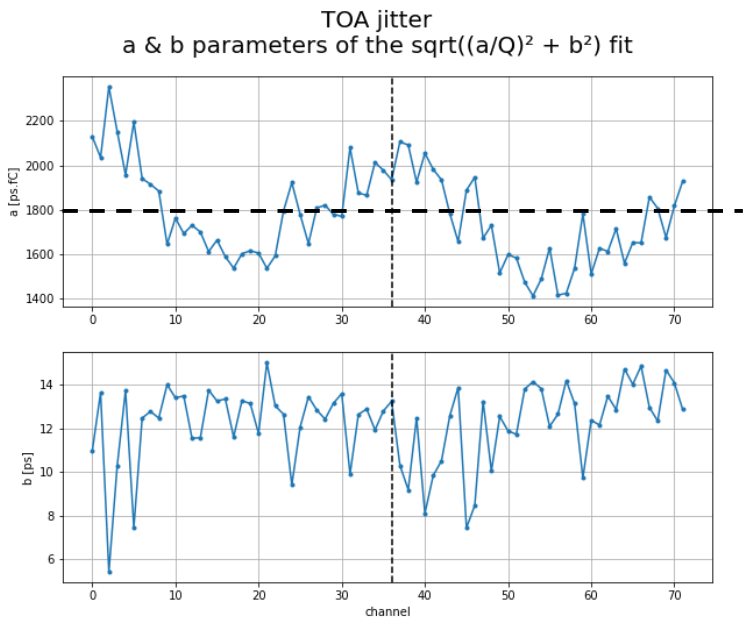
5.2 ADCu / ch
(+/- 2%)



Clock distribution from the middle of each half visible on the time walk distribution



0.38 TOTu / ch
(+/- 3 %)

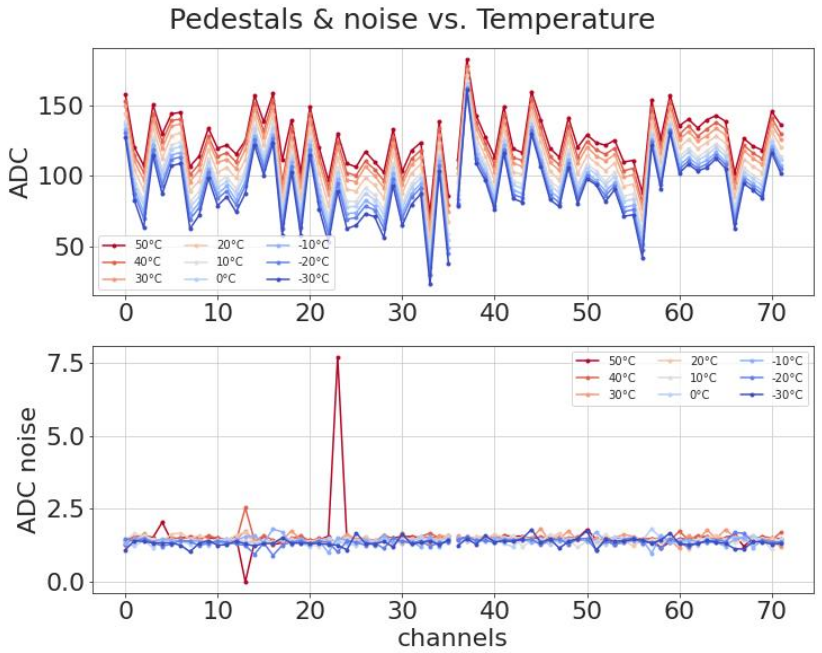


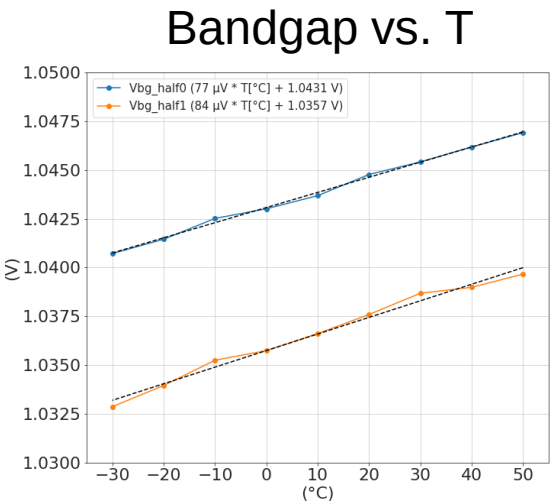
1.8 ns / Q(fC)

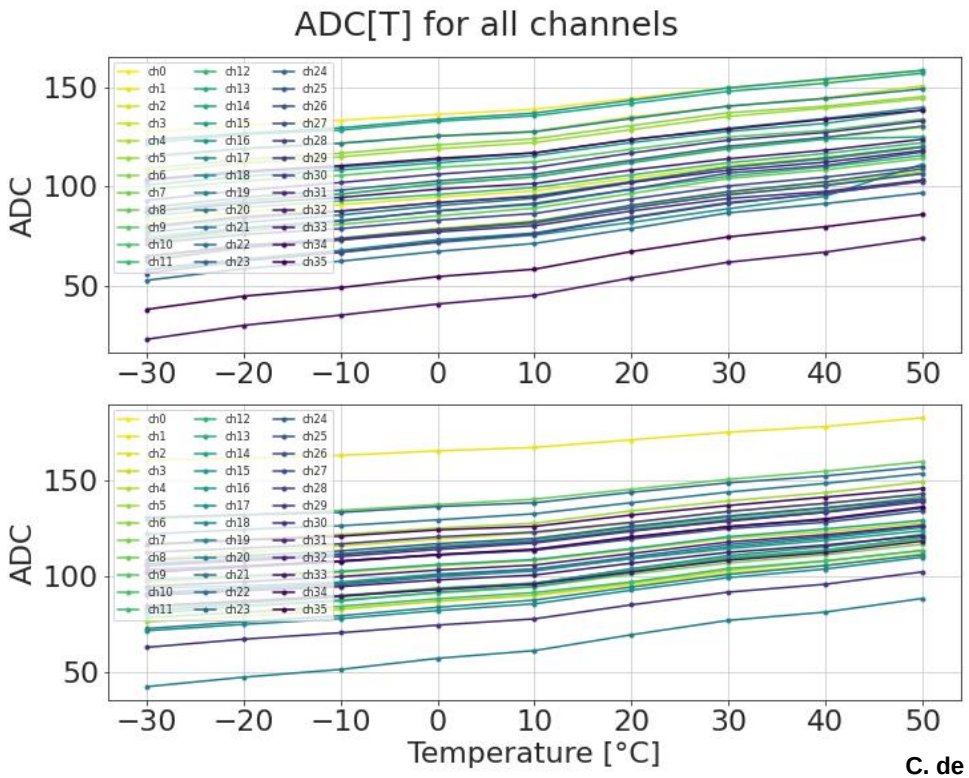
13 ps rms

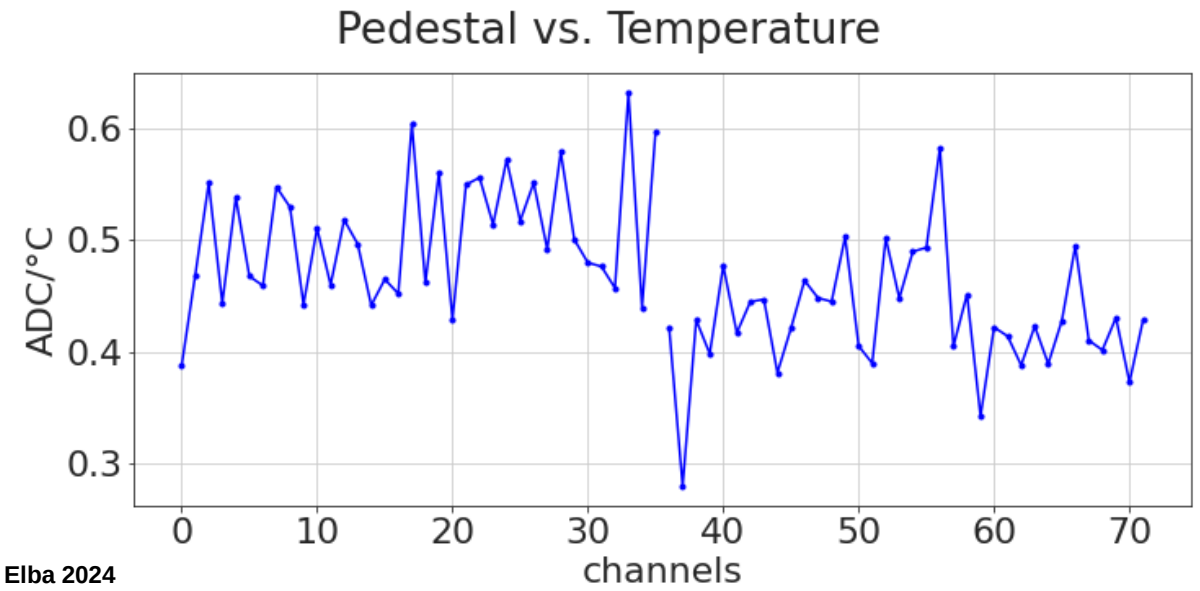
Temperature sensitivity

- Bandgap
  - 80 µV / °C
- Pedestals
  - + 0.5 ADCu/°C



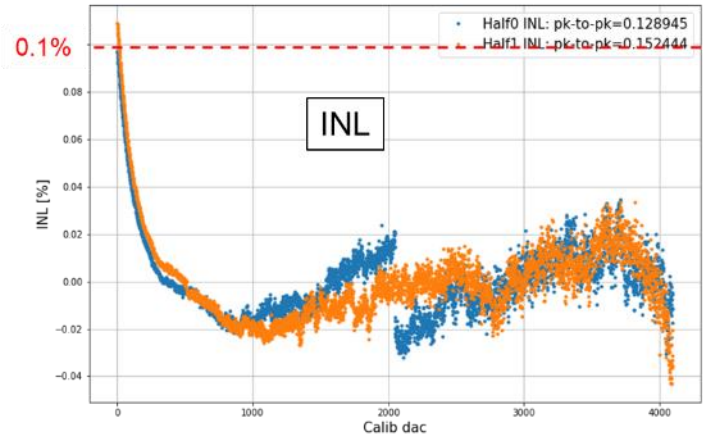


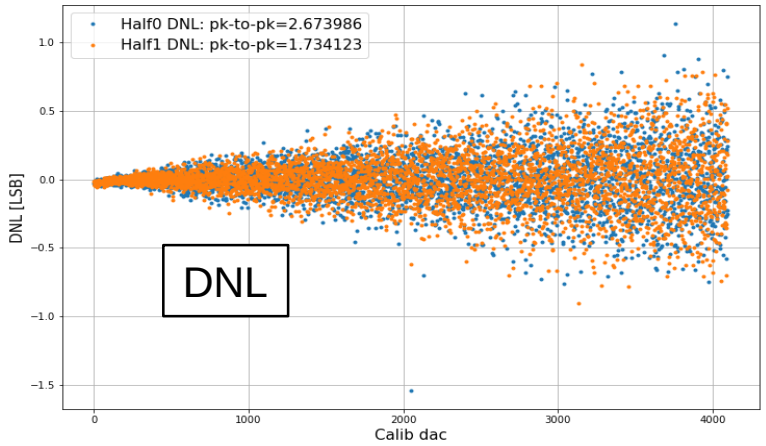


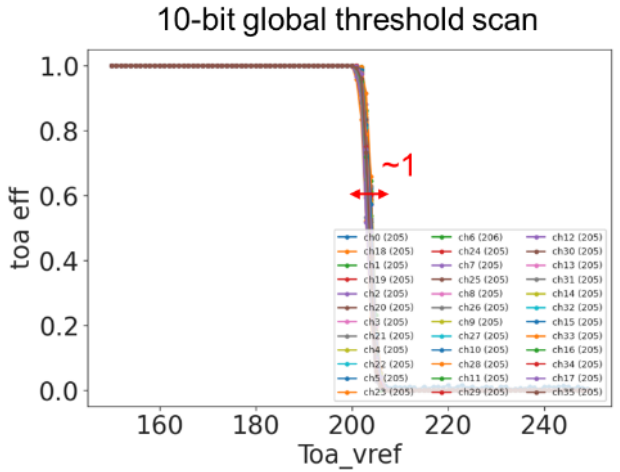


DACs & trimming

- 12 bits calibration DAC
  - ~ 2-3 mV offset due to leakage current (1 – 1.5 fC)
  - < 0.1 % linearity, temperature sensitivity: 60 ppm/K, stable after 350 Mrad
- Four 10-bit DACs to set pedestals, TOA & TOT thresholds + 3 channel-wise 6-bit DACs to reduce dispersion per channel
  - Pedestals: ~ 3 ADC counts dispersion after trimming,
  - TOA & TOT thresholds: 1-2 DAC counts after trimming
- 8-bit input DAC to compensate for the leakage current up to 45µA [cf backup]
  - Additional noise as expected from simulation

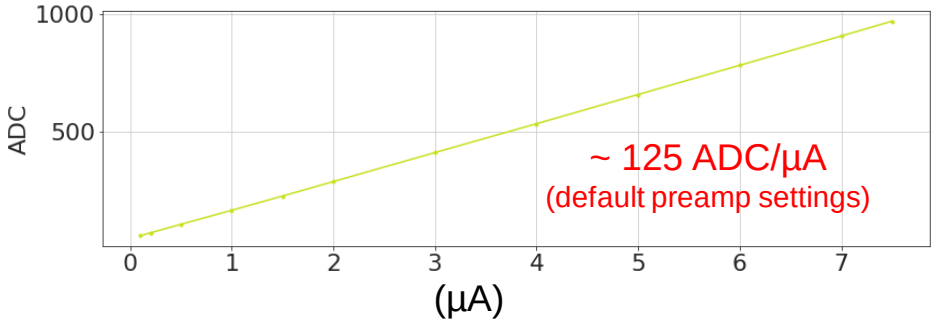




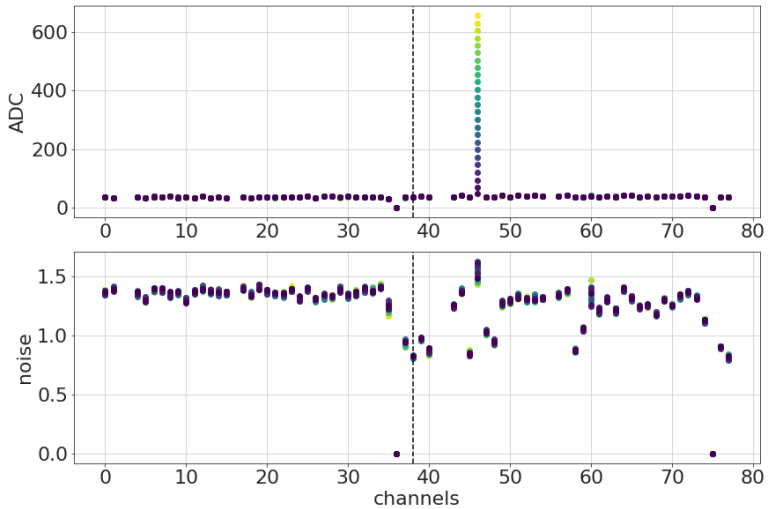


Leakage current

Pedestal vs. Leakage current



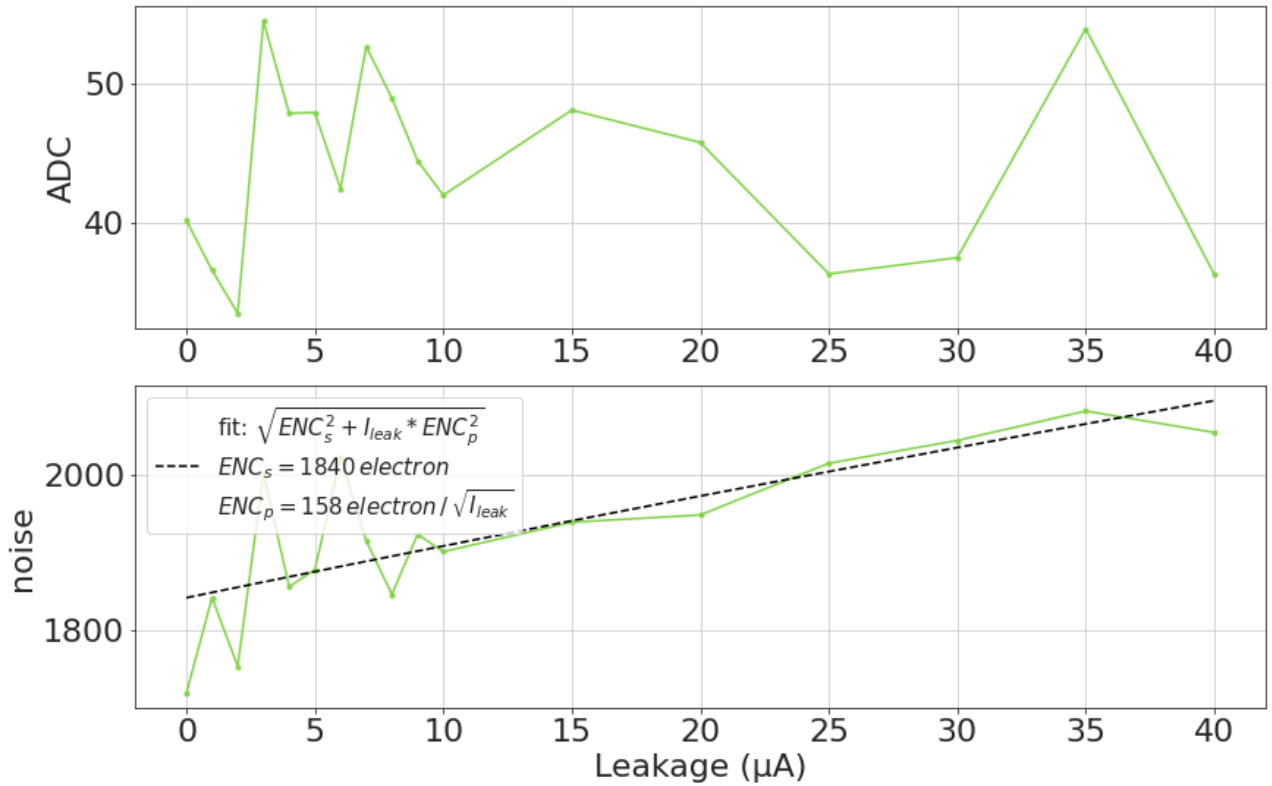
Pedestal vs. Leakage current



No shot noise from sensor leakage here!

Because leakage current provided with 100k resistor

ADC and noise wrt. input leakage current



More detailed plots in backup

H2GCROC3 tests [SiPM version]

- New circuitry to simplify the conveyor biasing wrt. Gain
  - No longer needs the complicated procedure on DACb adjustement
- Ability to compensate for up to 1 mA sensor leakage tested OK
- New 2.5V Calibration circuitry at conveyor input allows to calibrate up to 300 pC