# Design of a 8 Channel 40 GS/sec 20 mW/Channel Waveform Sampling ASIC in 65 nm CMOS

Jinseo Park[2],

D. Braga[1], F. Fahim[1], N. J. Pastika[1], P. M. Rubinov[1], T. N. Zimmerman[1],

T. England[1], H. J. Frisch[2], M. Heintz[2], E. Oberla[2], C. Poe[2], Y. R. Yeung[2],

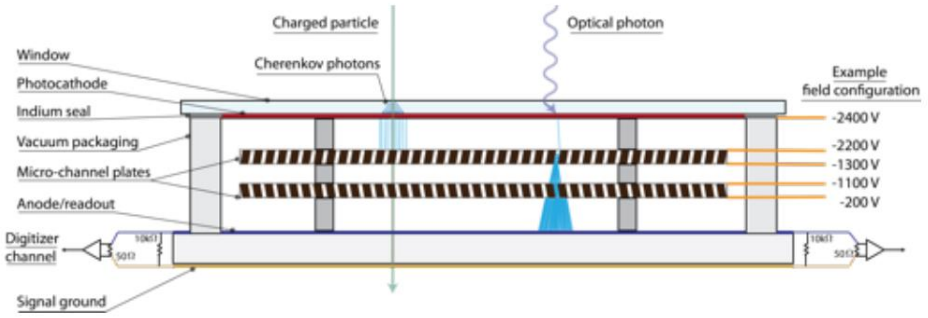
C. Ertley[3], N. Sullivan[4],

E. Angelico[5],

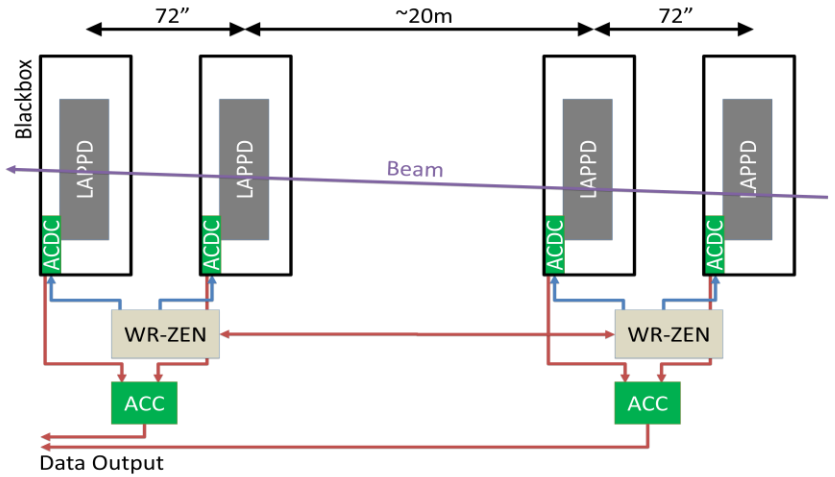
Hector Rico-Aniles[6]

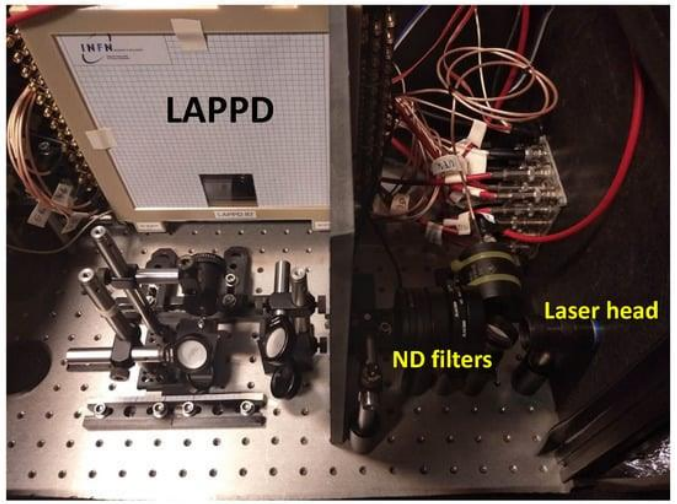
1. Fermi National Accelerator Laboratory 2. University of Chicago 3. Southwest Research Institute 4. Angstrom Research Inc. 5. Stanford University 6. North Central College

# Motivation: Detectors with ps level resolution

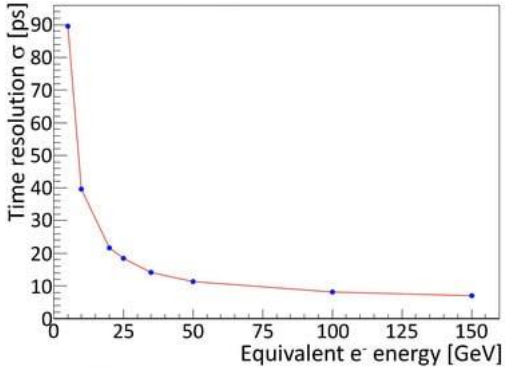


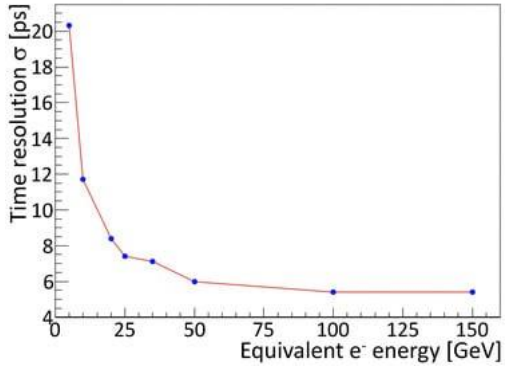

LAPPD$^{TM}$, psec.uchicago.edu




Perazzini S, Ferrari F, Vagnoni VM, on behalf of the LHCb ECAL Upgrade-2 R&D Group. Development of an MCP-Based Timing Layer for the LHCb ECAL Upgrade-2




Timing resolution for 200 pe =~5ps

## …WE ALSO NEED SUB-PS RESOLUTION FE ELECTRONICS!

# Primary goal

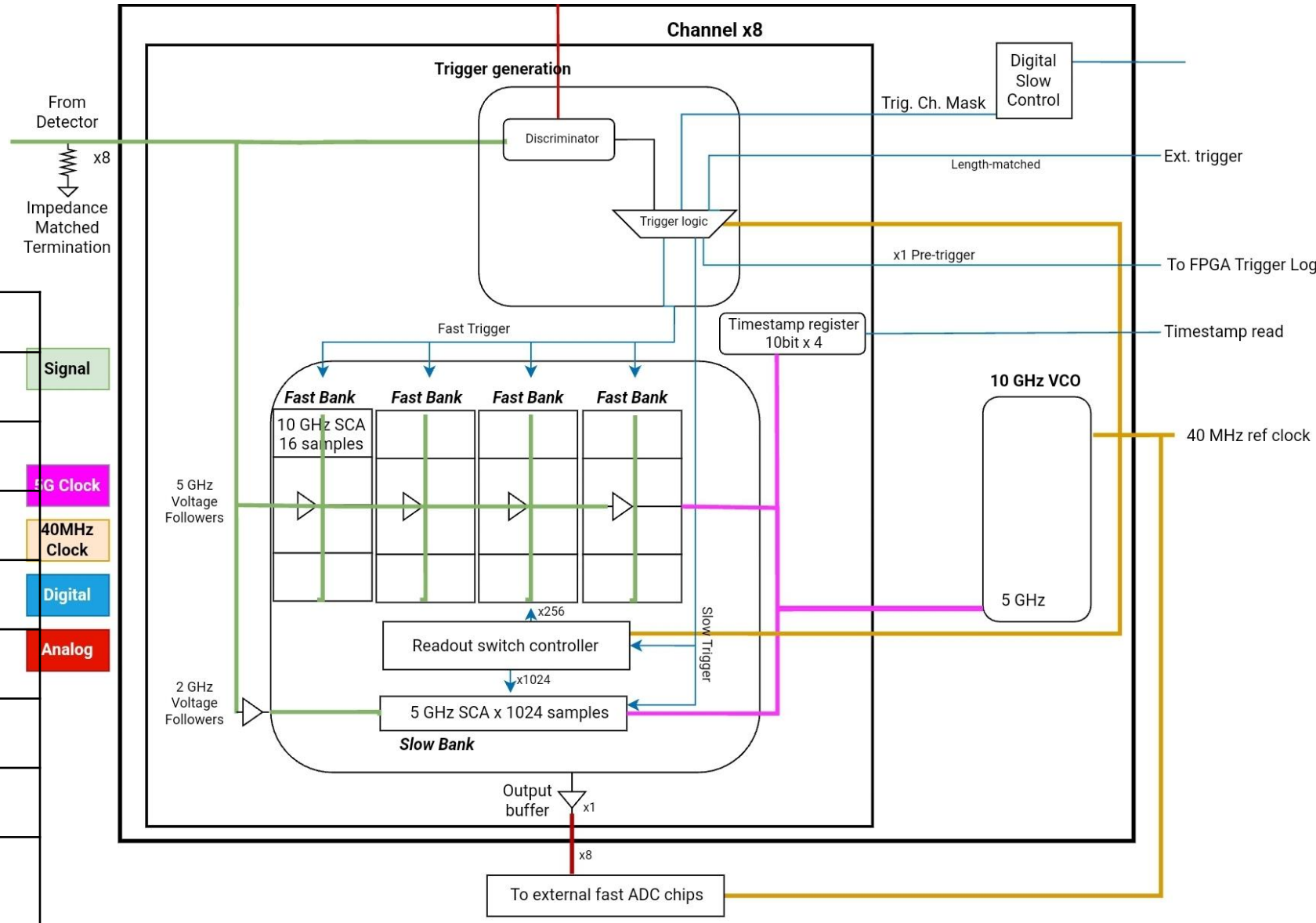
- Achieve **<1ps resolution** in measuring the arrival time of LAPPD pulses.

- But we also aim for a versatile chip, so that it is applicable to other fast-timing applications

- Sample and Hold at very fast frequency, and then digitize the held voltage values using commercial ADC chips.

# PSEC5

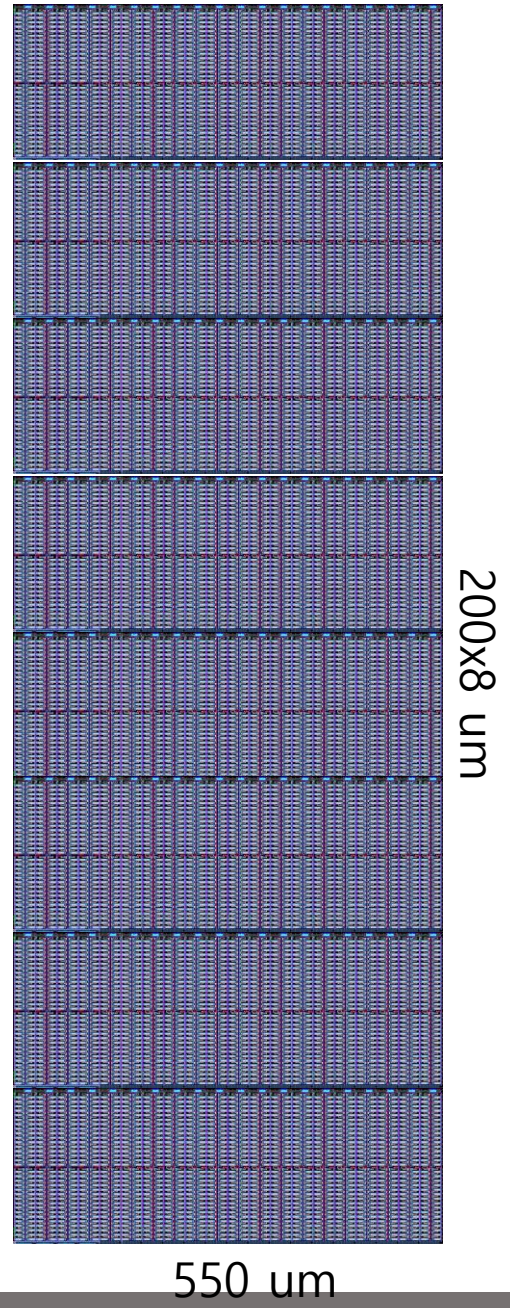
| | |
|---|---|
| Process | 65nm TSMC |
| Signal to Noise | 1000 |
| Sampling Rate | 40GSa/s(5GSa/s) |
| Buffer Length | 6.4ns(204.8ns) |
| Analog Bandwidth | 5GHz |
| Channels/Chip | 8 |
| Area | $2mm^2$ |
| Max. Readout Rate | 40KHz |
| Institution | UChicago & Fermilab |



# Schedule

| | |
|---|---|
| Schematic / Simulation | Sep. 2023 |
| Layout | Mar. 2024 |
| Post Layout Simulation | Apr. 2024 |
| Layout Optimization | Jul. 2024 |
| Tapeout without package (Pre-production) | Sep. 2024 |
| Testbench (Chip on Board) | Dec. 2024 |
| Production | 2025 |

Core Layout (Without Digital & Clock generation Block)

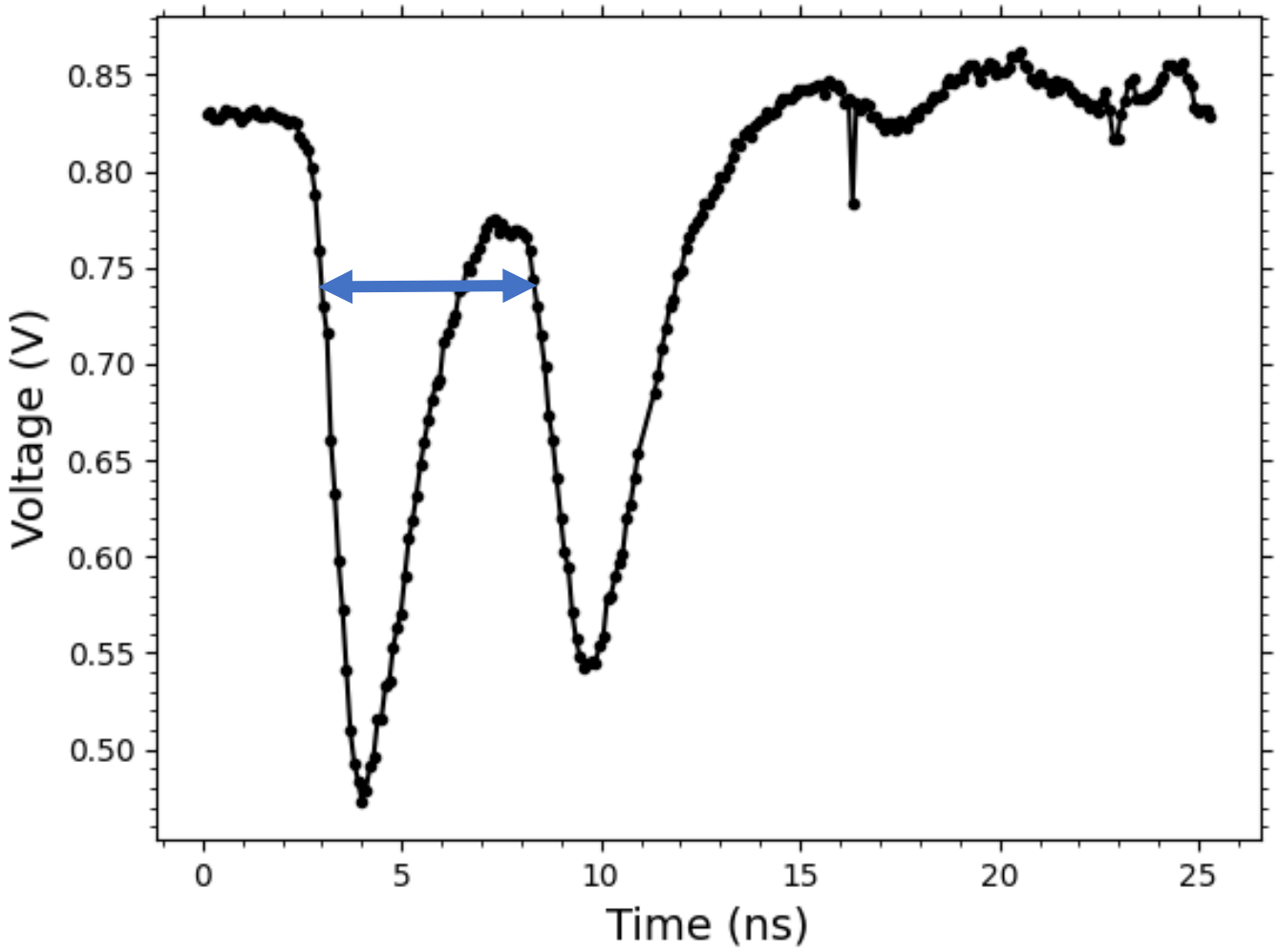


# Comparison with Oscilloscope

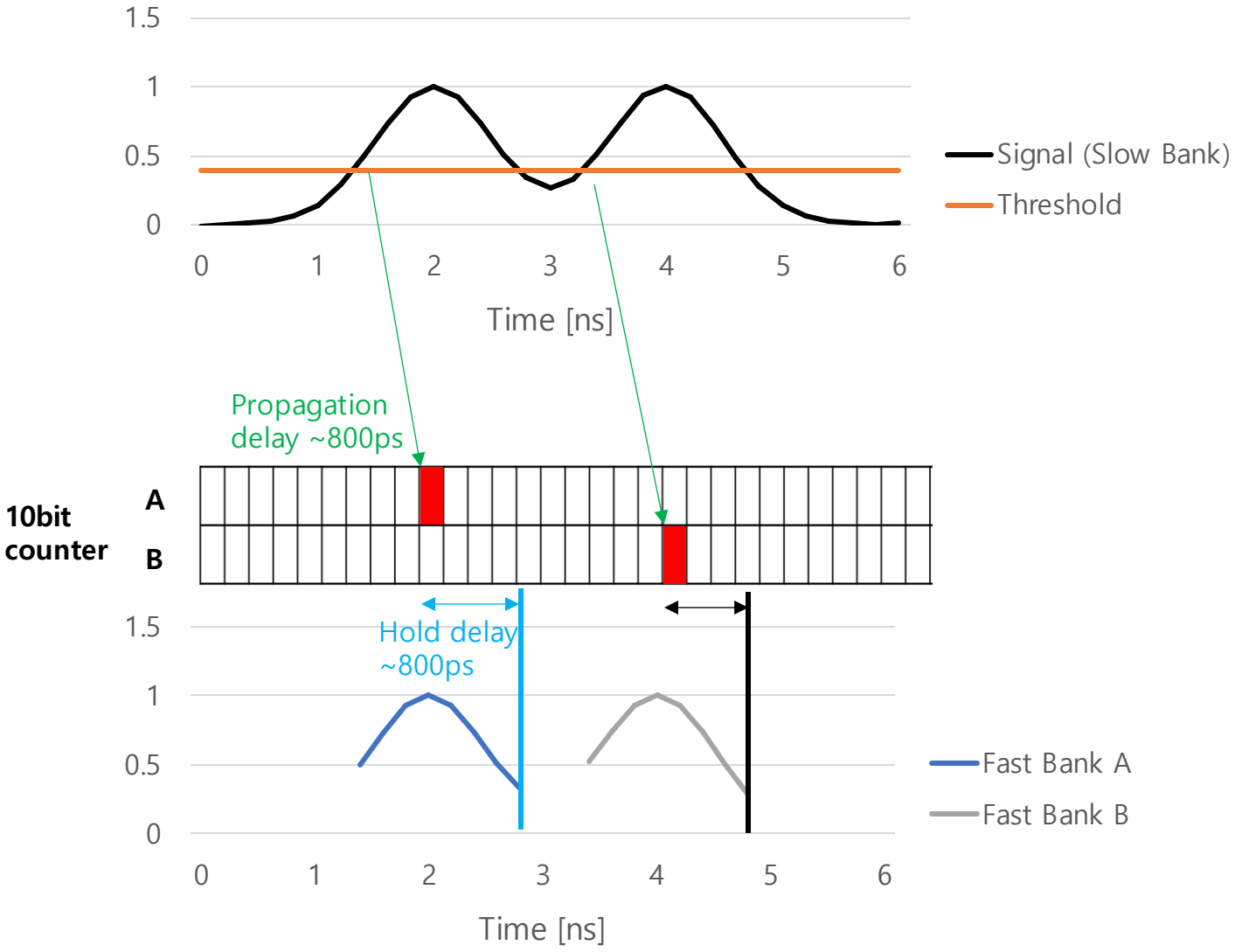
| | PSEC5 | Oscilloscope |
|---|---|---|
| Power/Channel | Low(20mW/Ch) | High |
| Output | Analog | Digital |
| Real Time | No(40k events/s) | Yes |
| Cost/Channel | Low | High |

# Point 1. Fast & Slow Banks

LAPPD event readout
with a stripline anode

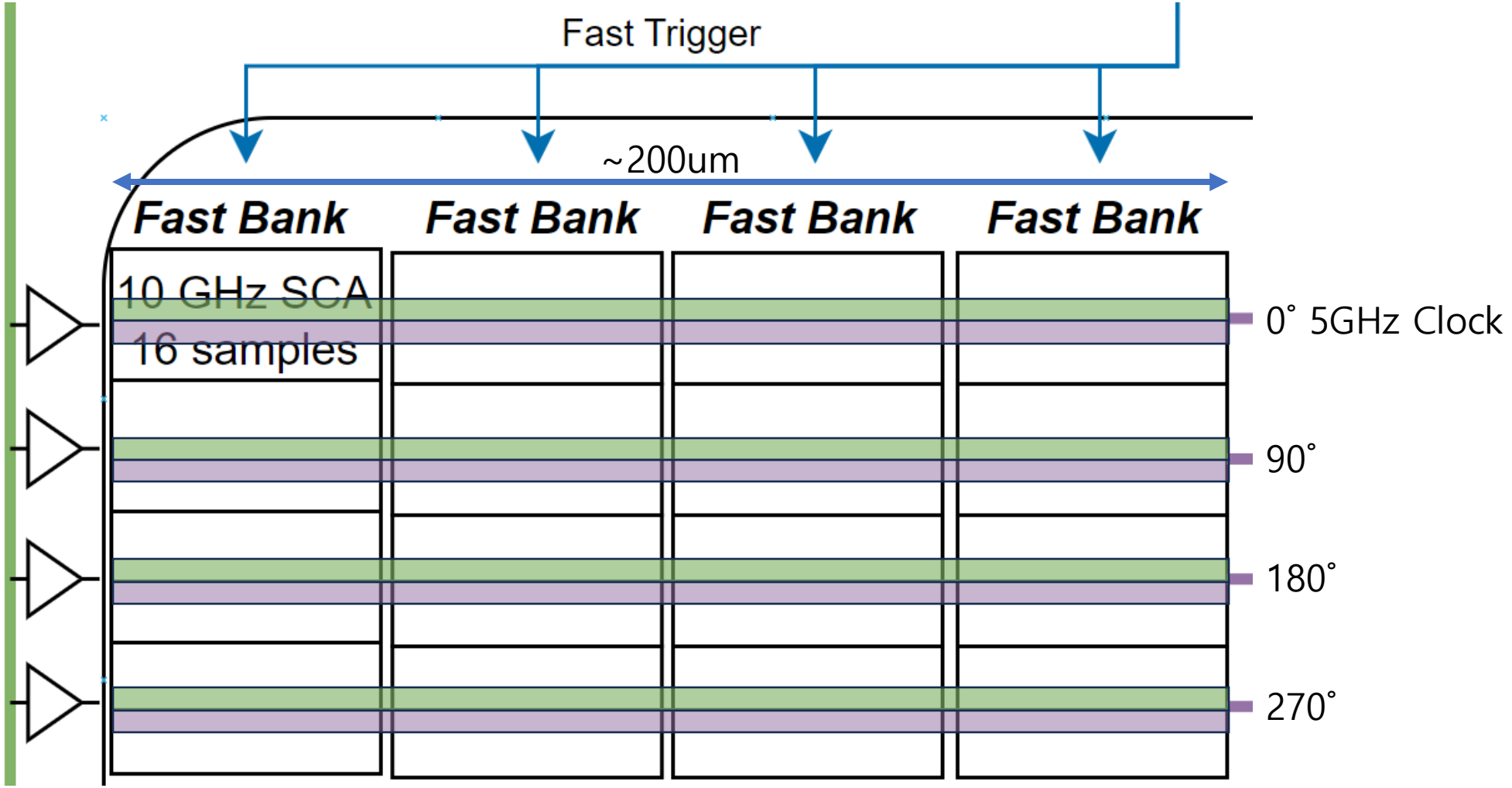


# Fast Bank Usage Example

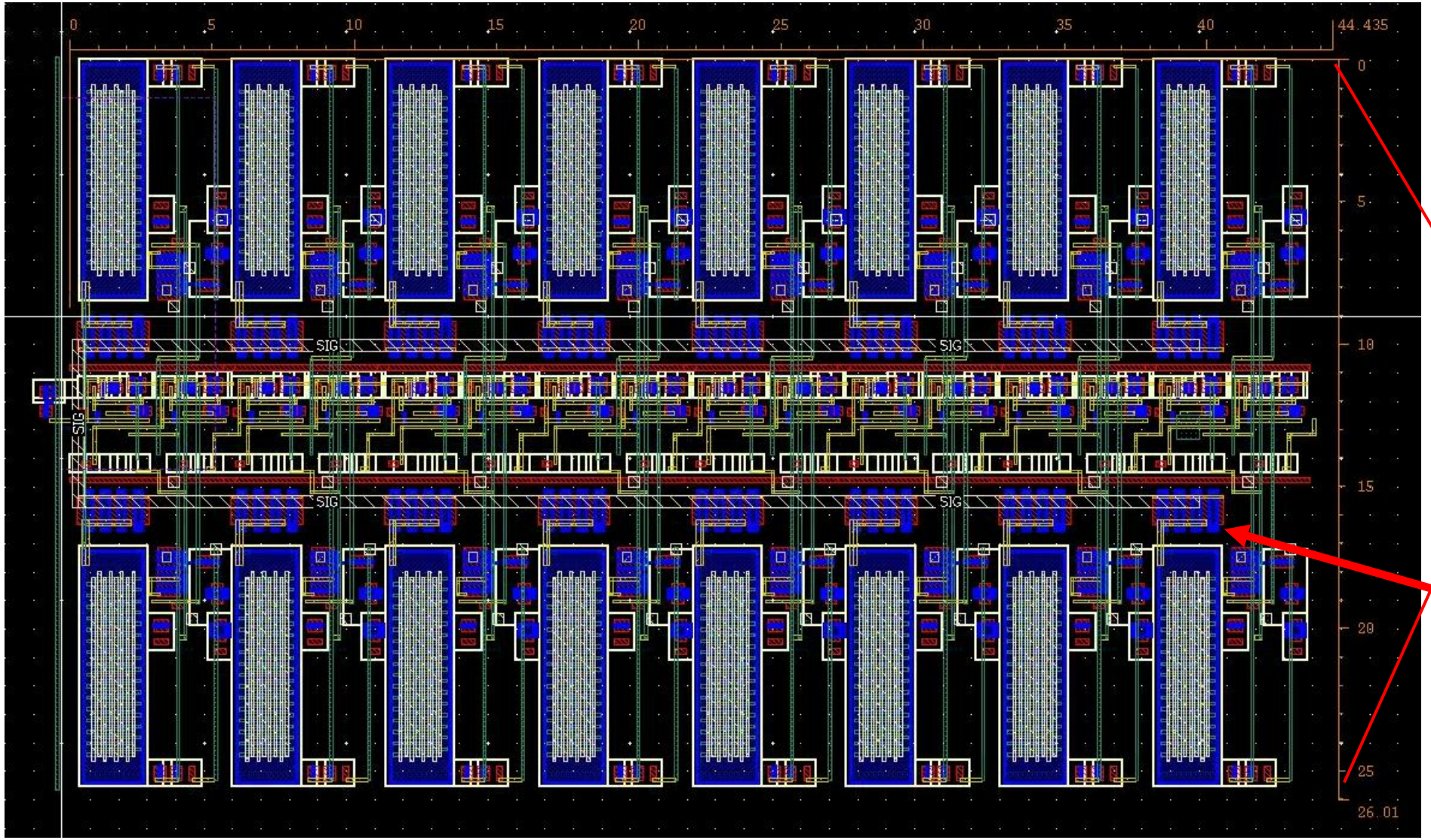



- 4 Fast Banks
  - 64×*4* samples
  - 1.6ns×*4* of sampling window
  - High power consumption
  - Run sequentially
- Slow Bank
  - 1024 samples
  - 204.8ns of sampling window
  - Low power consumption
  - Fast banks are triggered within the sampling window

# Fast sampling - interleaved

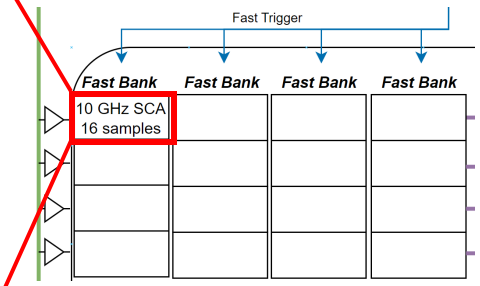


# Layout of a single column (16 cells)



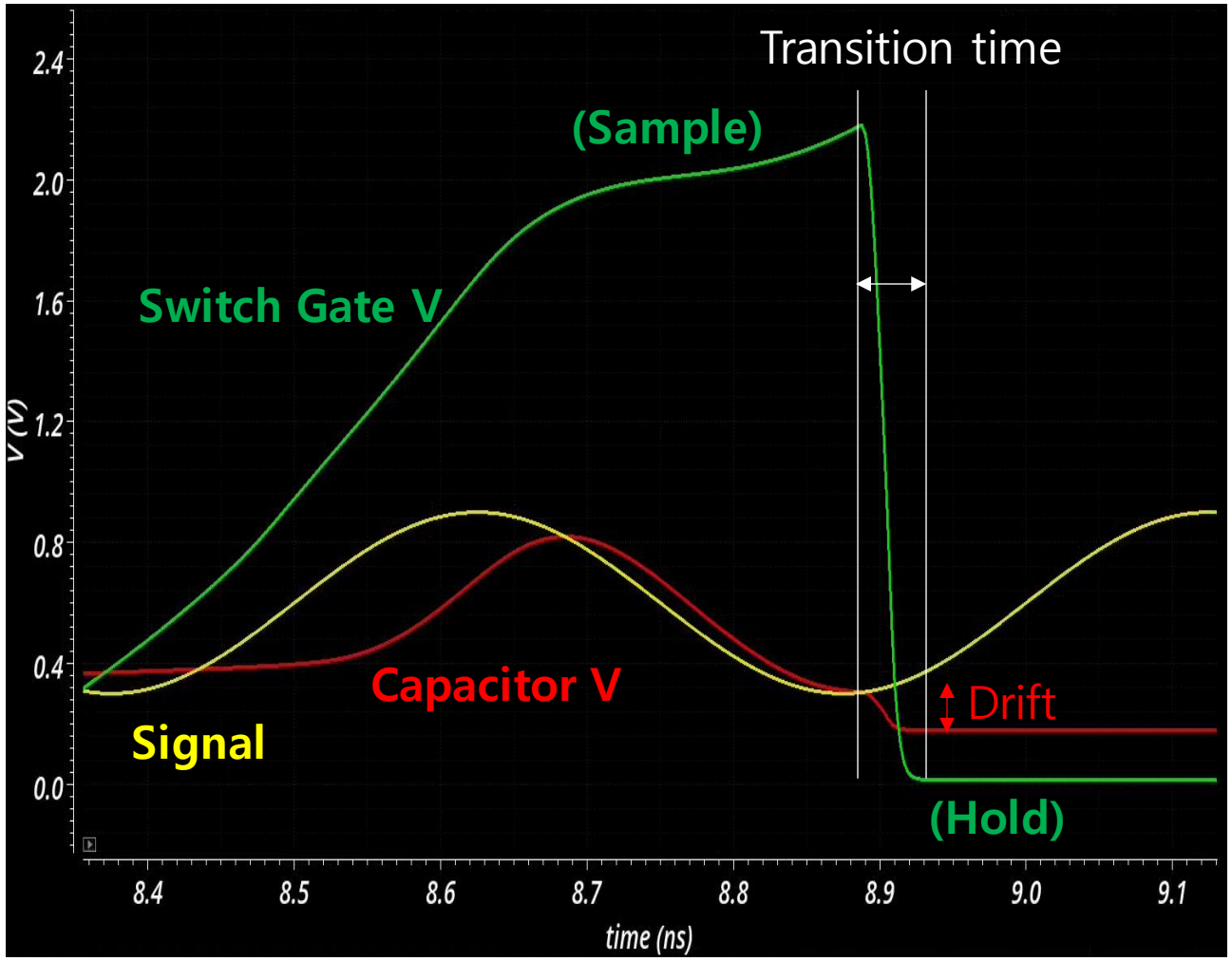

Size: $45\mu m \times 25\mu m$

Capacitor: 35fF




Sampling Switch
2.5V NMOS
Size: $4\mu m \times 280nm$

# Switching Drift

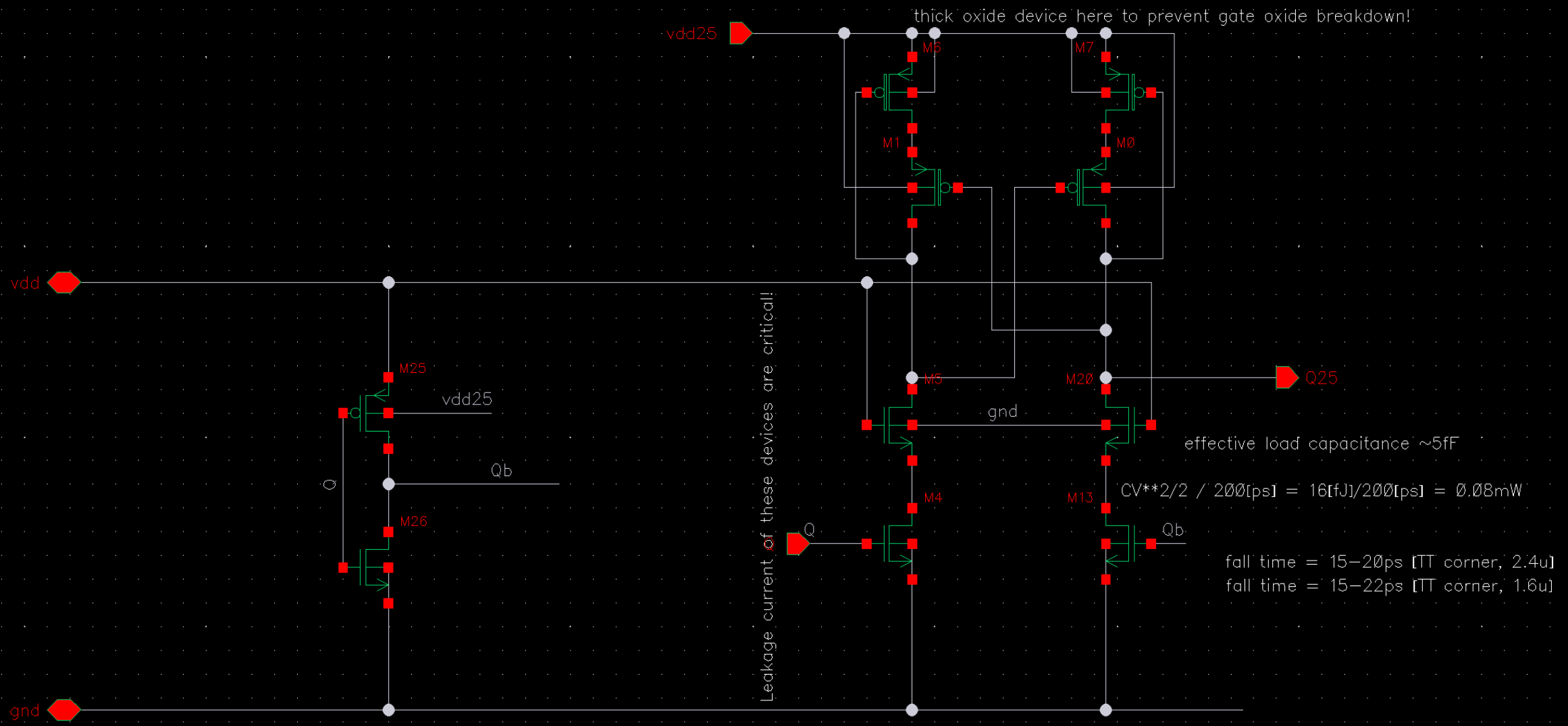



- The value of a capacitor **drifts while it switches off** from the signal line.
- Drift consists of **switch gate charge injection**, which is a fixed value and is calibratable, and **resistive drift**, which is dependent on signal V.
- It is essential to keep the

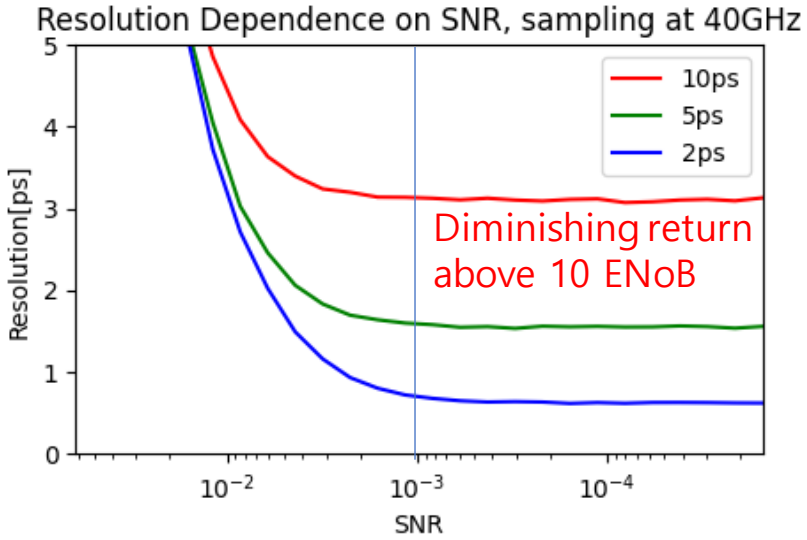
**[Sample → Hold]** transition time low.

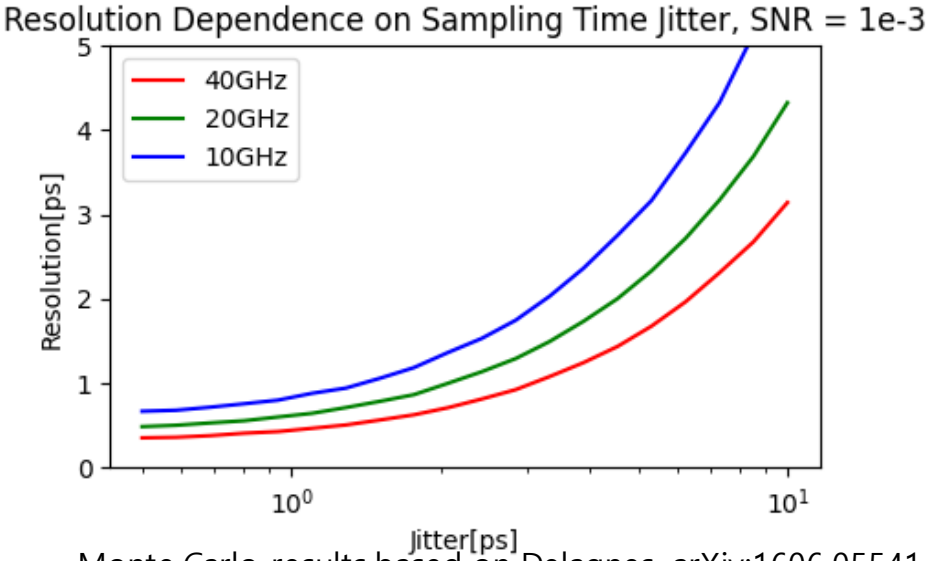
**→NMOS instead of CMOS for the sampling switch!**

# Voltage Level Shifter



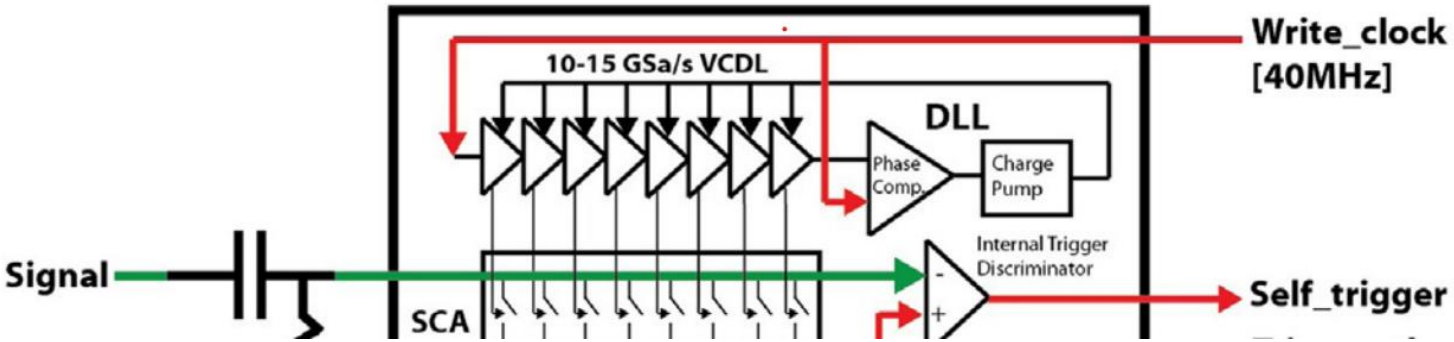
# Point 2. Sampling Time Uncertainty




Monte Carlo results based on Delagnes, arXiv:1606.05541

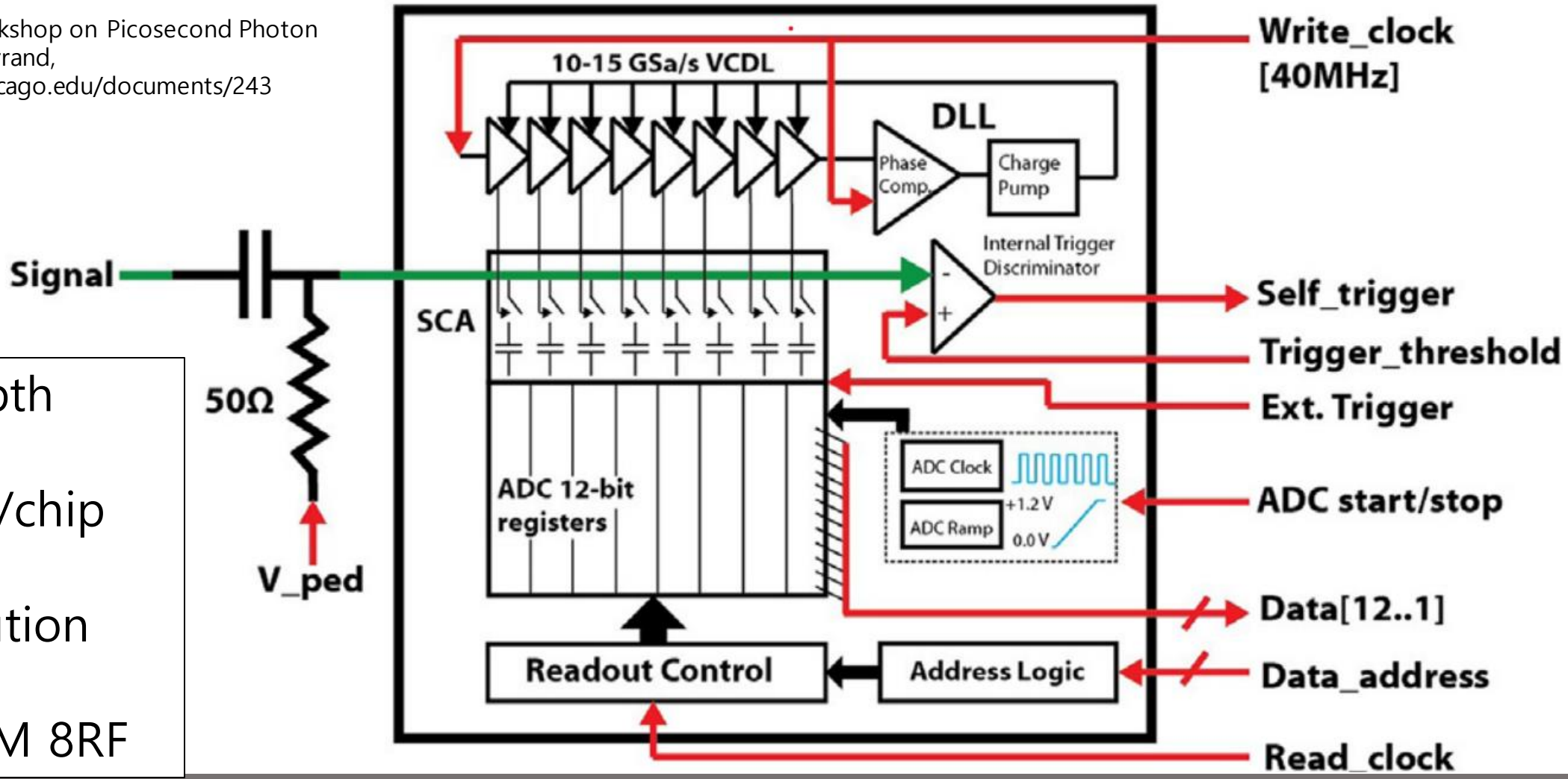
- At <1ps timing resolution region, it is a **dominant component** of the overall uncertainty.
- Previous Chip PSEC4 employed Delay Locked Loop (DLL) to control sampling switches.
- Process Variation is a major source of systematic timing uncertainty.



# PSEC4 ASIC(2014)

E. Oberla, H. Frisch, K. Nishimura, G. Varner, arxiv.org/abs/1309.4397

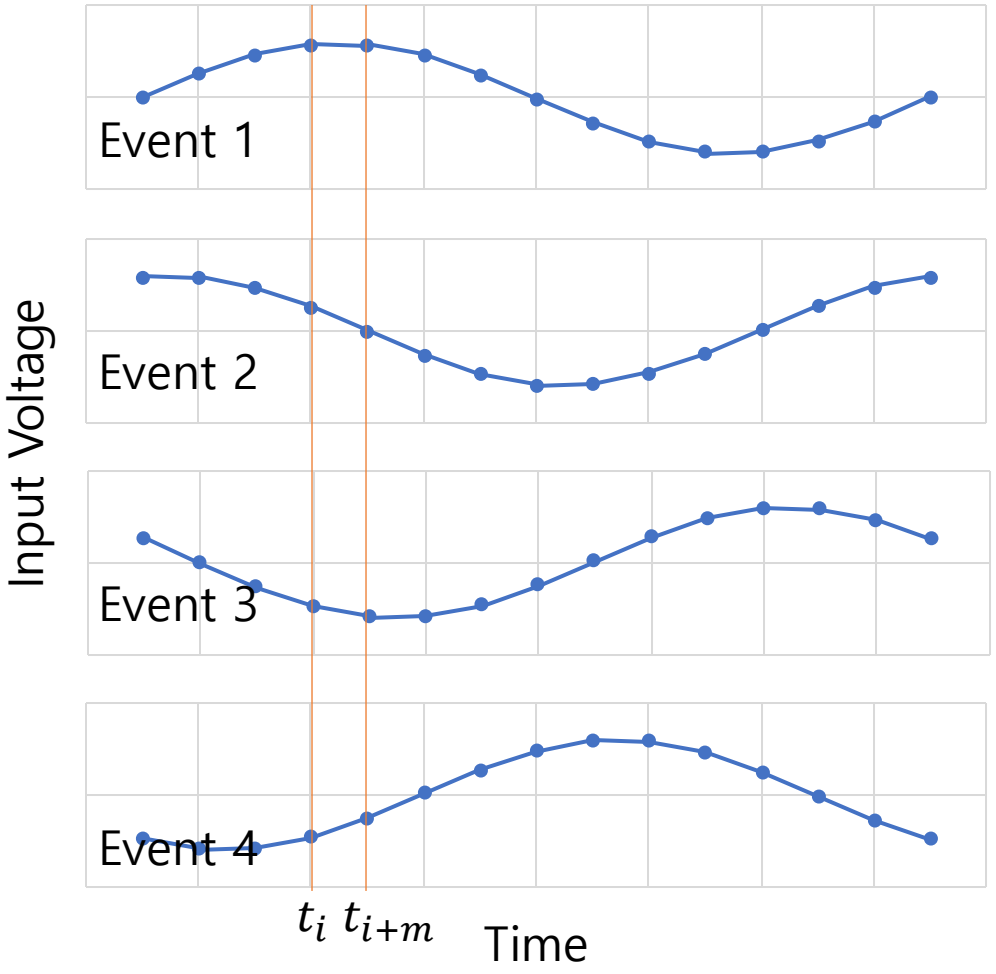
E. Oberla, Talk at Workshop on Picosecond Photon Sensors, Clermont-Ferrand, http://lappddocs.uchicago.edu/documents/243

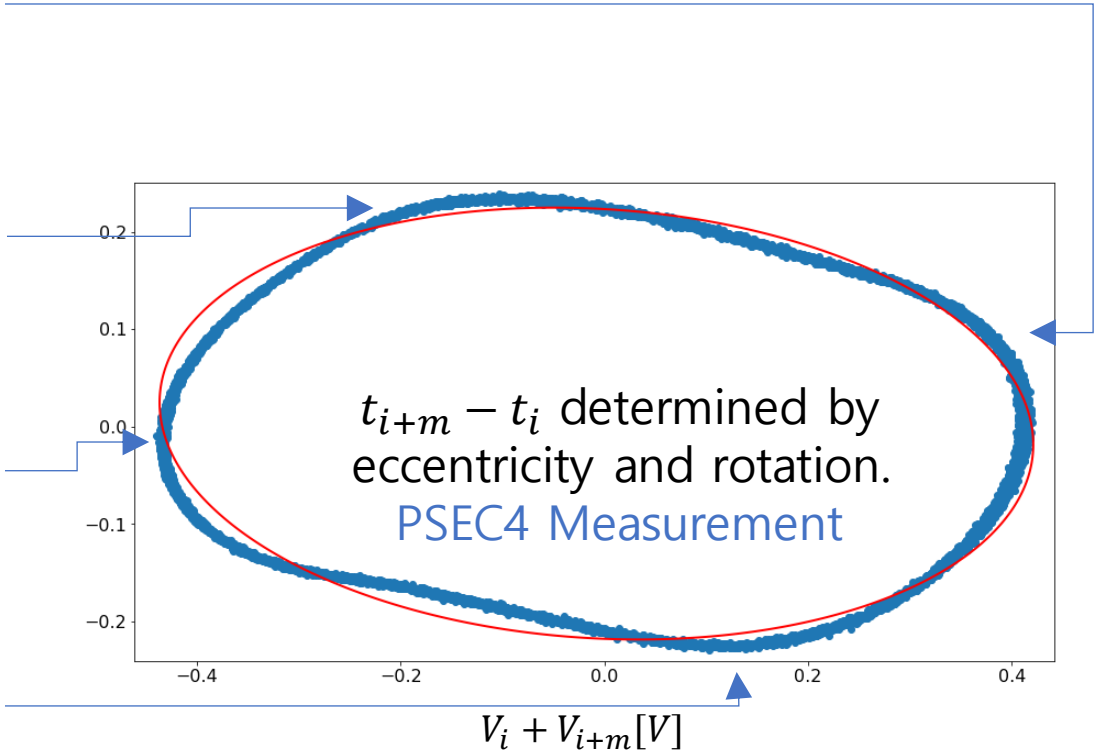



- 12-bit depth
- 6 channel/chip
- 5ps resolution
- 130nm IBM 8RF

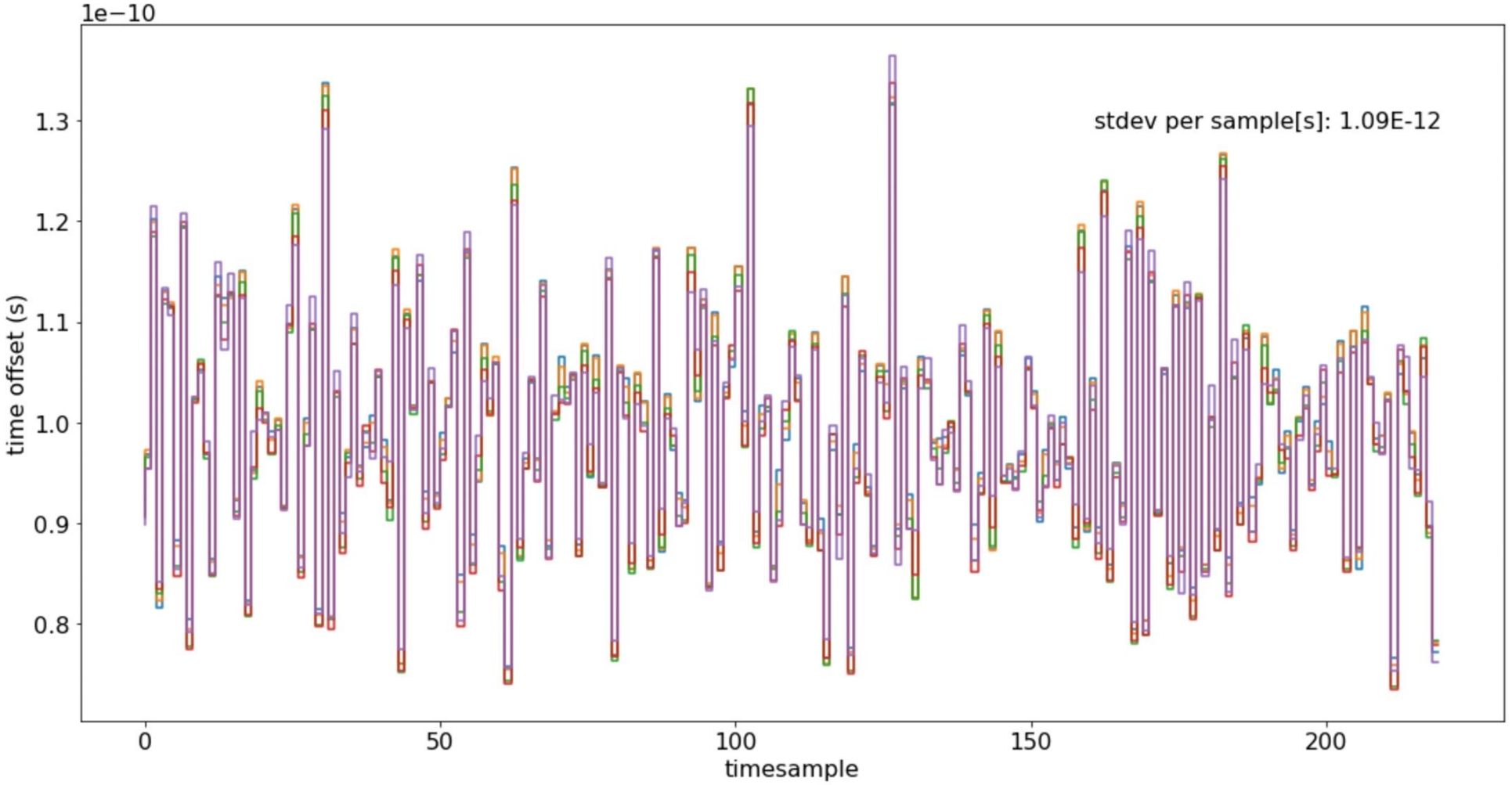
1. Measure many events of a sine wave.
2. Sum vs. Difference of two adjacent samples, over all events, form an ellipse.
3. Time offset can be determined from the coefficients.

Low SNR → fainter, more spread curve.
Nonlinearity → distorted curve

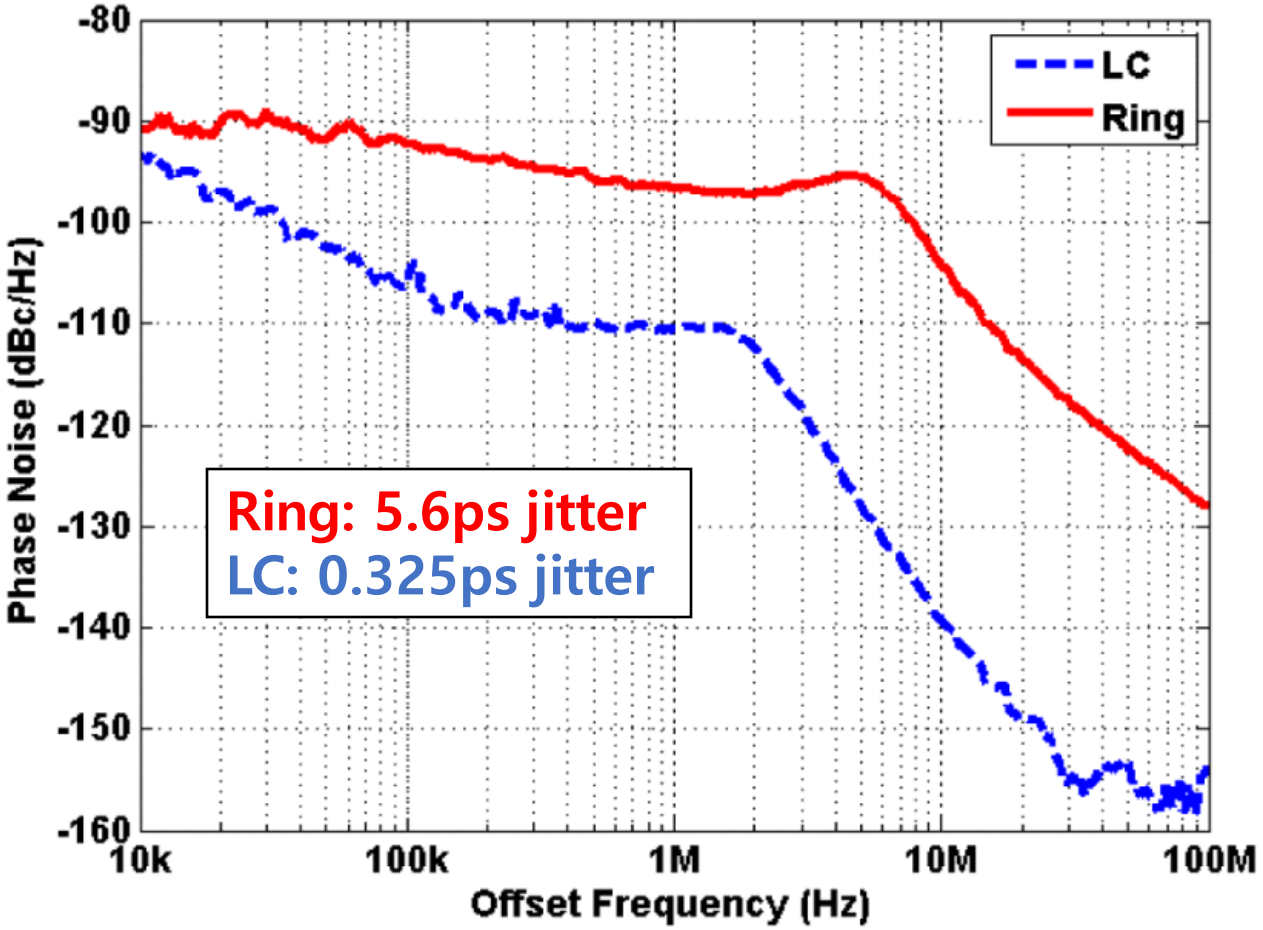


# Sample Time Distribution of PSEC4



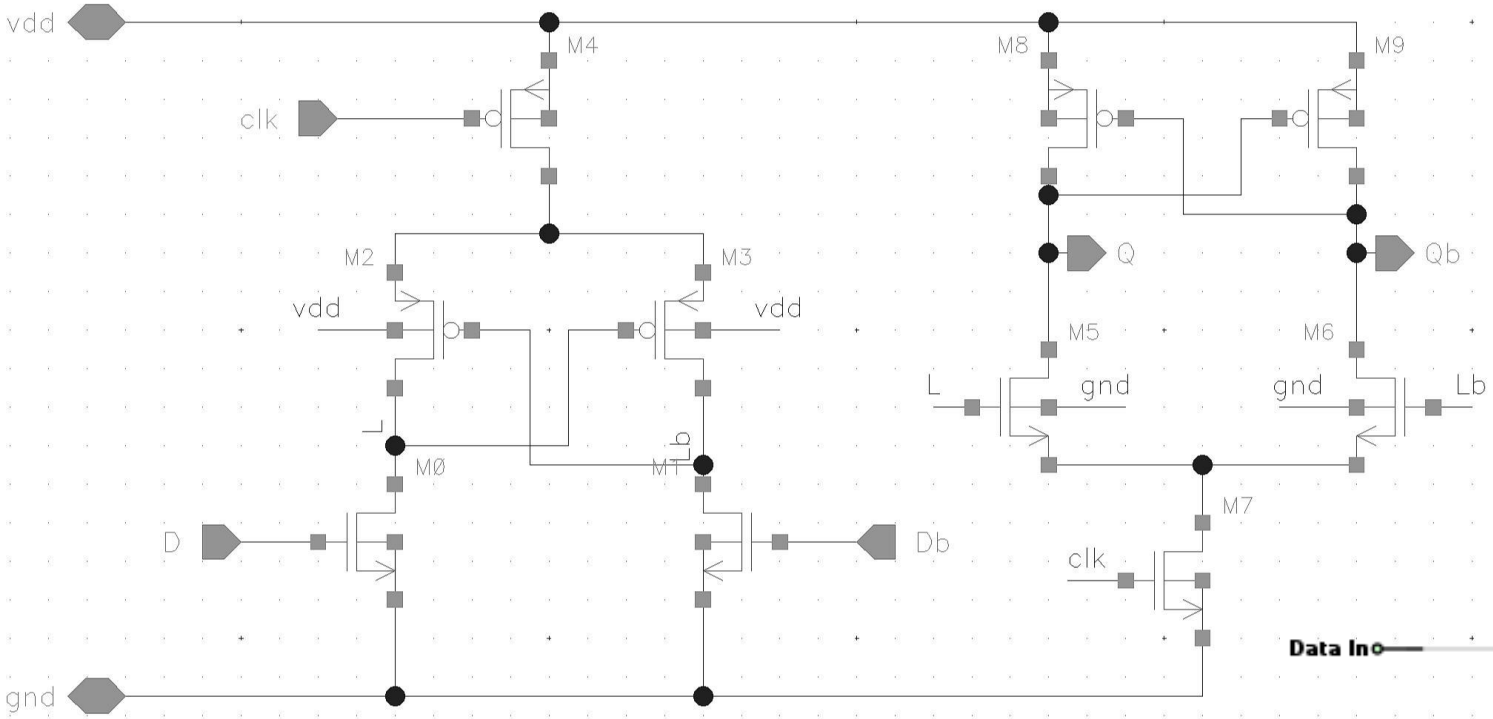
# Timing uncertainty reduced by an optimized LC-oscillator based PLL

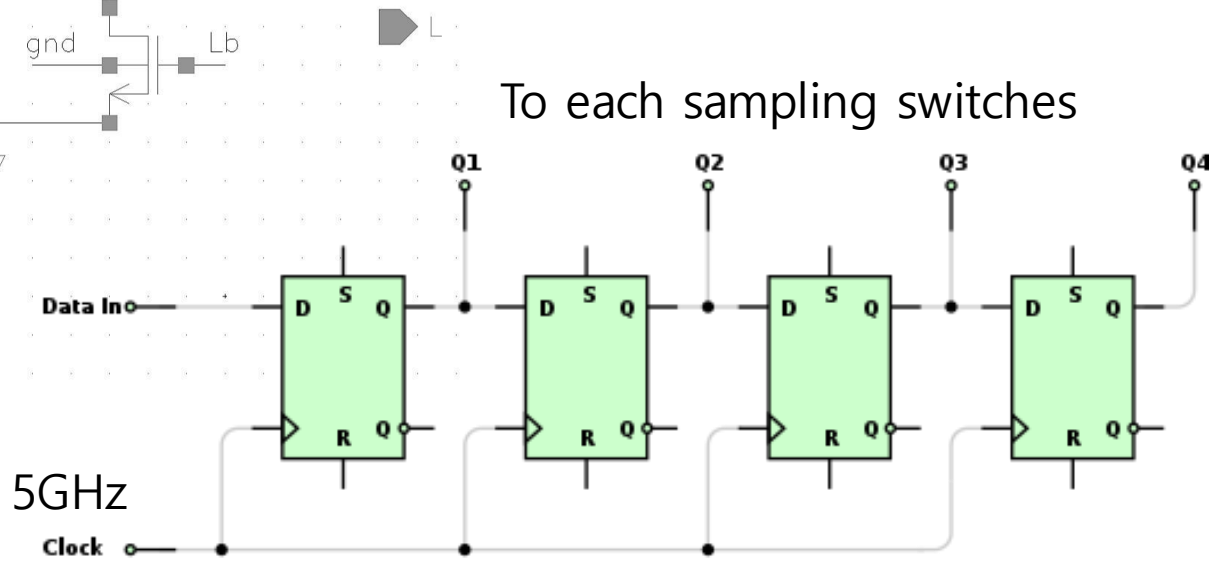



From abstract:
"Both independent PLLs have identical loop dynamics to allow a fair comparison …
Furthermore these circuits consume the same amount of power. The PLLs were processed in a commercial 65 nm CMOS technology."

J. Prinzie, J. Christiansen, P. Moreira, M. Steyaert and P. Leroux, "Comparison of a 65 nm CMOS Ring- and LC-Oscillator Based PLL in Terms of TID and SEU Sensitivity," in *IEEE Transactions on Nuclear Science*, vol. 64, no. 1, pp. 245-252, Jan. 2017.

# 5GHz Dual Edge Triggered D Flip-Flop




- Still, we expect to use similar calibration technique as PSEC4

# Summary

- PSEC5 is a reliable, reusable, and cost-efficient **waveform sampling** ASIC.
  - Lower power consumption and dead time
  - Avails various methods of external calibration
  - **High channel count** per chip
- The **fast-slow architecture** of the chip makes it relatively versatile
  - Long time window (204.8 ns) per event
  - While also achieving high timing resolution on regions of interest (6.4 ns)
- It can easily be incorporated as a front end of any detector system which requires **<1ps timing re solution.**

***THANK YOU FOR YOUR ATTENTION!***