4D-Tracking with Digital SiPM-ICs

Exploring the Potential of CMOS SPAD Arrays

Inge Diehl, Finn Feindt, Ingrid-Maria Gregor, Karsten Hansen, Stephan Lachnit, Daniil Rastorguev, Simon Spannagel, Tomas Vanat, **Gianpiero Vignola**

PM2024, 28 May 2024

HELMHOLTZ





Silicon Photomultipliers

State of the Art Solid State Photodetectors



SiPM-IC Using Commercial CMOS Processes

Exploring SPADs in Foundries Process Design Kits





DESY dSiPM in LFoundry 150 nm

Digital SiPM integrated circuit (dSiPM)

Advantages

- large and fast signals
- Customized readout architectures
- Masking of noisy pixels
- Hitmap readout possible
- Simpler DAQ system
- Large volume production
- Low-cost implementation
- New possible applications

Drawbacks

- Processes not (yet) specialized
- Higher noise compared to SiPMs
- Reduced fill factor (electronics)

CMOS SPADs Applications

Commercial and HEP Examples



LIDAR & 4D-imaging

- Automotive
- Industry
- Security

Images from: Fraunhofer IMS



Scintillating fibers readout

• Calorimetry, tracking





4D-Tracking of charged particles?

• MIPs tracking and timing

https://dx.doi.org/10.1088/1361-6633/aa94d3

dSiPM as Possible 4D-Tracker Candidate

Beyond Photon Detection Applications

MIP detection with analog devices

- SPAD/SiPMs already proved to be good MIPs detectors [1] [2]
- Excellent instrinsic timing performance O(10 ps)
- Photon detection is still possible (multipurpose detector)

Using CMOS dSiPM

- On-chip data processing and digitalization
- Tracking-like detector architecture possible
- High granularity with O(10 µm) spatial resolution
- Large area/volume production possible

Drawbacks

- Efficiency is limited by the fill factor
- High DCR compared to standard pixel detectors
- No distinction between signal and noise



MIP interaction in a SPAD

DESY dSiPM Prototype

ASIC in LF 150 nm CMOS

Layout

- In LFoundry 150 nm CMOS technology
- Main matrix: 32 x 32 pixels (4 SPADs per pixel)
- Sensor area: 2.2 x 2.4 mm² ٠
- Test structures in the chip periphery

Features

- Full hit matrix readout and timing measurements
- 4 x 12-bit Time to Digital Converters with ~95 ps bins ٠
- Pixel masking & 2-bit in-pixel hit counting
- Quenching can be tuned (quenching transistor)
- In chip trigger logic
- Readout is frame-based (3 MHz frame rate)
- Versatile Caribou DAQ system is used for biasing & readout

For details: I. Diehl et al 2024 JINST 19 P01020

DESY. |4D-Tracking with Digital SiPM-IC PM2024 | Gianpiero Vignola 28-May-2024



ASIC design of the DESY dSiPM







DESY dSiPM pixel picture (69.6 x 76 µm²)



Caribou DAQ system Fast & low cost implementation of solid state detector prototypes http://dx.doi.org/10.22323/1.370.0100 https://gitlab.cern.ch/Caribou/

DESY dSiPM Test Beam

Device Treated as a Particle Detector





DESY dSiPM test beam setup



- **EUDAQ** framework and AIDA TLU used for data acquisition and synchronization of devices.
- Corryvreckan Framework used for test beam data reconstruction and analysis

DESY dSiPM Spatial Properties

Direct MIP Detection (Only Silicon)



DESY dSiPM Timing

Direct MIP Detection (Only Silicon)



160

140

120

100

DESY dSiPM Efficiency

Direct MIP Detection (Only Silicon)





0.8

0.7

0.6

0.5

0.4

0.3

0.2

0.1

10 20 30 in-pixel x_{track} [μm]





DESY dSiPM + thin LYSO

- Overcome efficiency limit
- Reduce noise contamination (large signals for MIP events)
- Preserve good spatial resolution
- Concept already explored using analog SiPM [1] [2] [3]
- Three sample assembled with 100, 200 & 500 µm thick LYSO



Thin LYSO glued on DESY dSiPM



DESY dSiPM + Thin LYSO

Cluster Size, Signal & Noise with Different Tagging





MIP detection with thin radiator coupling



Small temperature (DCR) dependence

DESY dSiPM + Thin LYSO

Spatial Residuals, Good Spatial Performances Preserved







- Thinner LYSO has better spatial resolution
- Sigma ~32 μm (100μm LYSO) and ~38 μm (200μm LYSO)
- Small OV & temperature dependence

DESY dSiPM + Thin LYSO

Efficiency & Timing Performances



- From ~33% (bare silicon) to >99% using Thin LYSO coupling
- No OV or temperature dependence



MIP detection with thin radiator coupling



Faster radiators may improve timing

Summary & Outlook

dSiPM as 4D-Tracking Candidate

CMOS dSiPMs

- Combination of SPAD and CMOS electronics in the same silicon die opens new application possibilities
- Reduction of complexity & cost especially for large volumes

DESY dSiPM & MIPs 4D-Tracking

- dSiPM can be a possible candidate technology for 4D-tracking
- Spatial resolution down to ~20 µm and ~50 ps system timing
- Efficiency >99%, very low noise rate using thin LYSOs

CMOS dSiPMs R&D Potential

- dSiPM can play an important role in future HEP detector systems
- CMOS dSiPMs are a "young" technology, promising R&Ds ongoing
- Any new idea of possible HEP application is welcome

DESY dSiPM 4D-Tracking Performances

	dSiPM	dSiPM+LYSO
Signal Cluster Size	~ 1	10 – 40
Spatial Resolution	~ 20 µm	~ 35 µm
Efficiency in MIP detection	~ 33 %	> 99 %
Noise Rate	O(MHz)	O(Hz)*
Time Resolution	~ 50 ps	< 1ns **

* While cutting on cluster-size

** Currently under investigation

Thank you.

References:

I. Diehl et al, Monolithic MHz-frame rate digital SiPM-IC with sub-100 ps precision and 70 µm pixel pitch S.Lachnit, Time Resolution of a Fully-Integrated Digital Silicon Photo-Multiplier F.Feindt et al, The DESY digital silicon photomultiplier: Device characteristics and first test-beam results

Gianpiero Vignola gianpiero.vignola@desy.de

Deutsches Elektronen-Synchrotron DESY Notkestraße 85, 22607 Hamburg 1C, O1.331, ATLAS



The measurements leading to these results have been performed at the Test Beam Facility at DESY Hamburg (Germany), a member of the Helmholtz Association (HGF).

DESY dSiPM ASIC

More Details in Reference Publication



Figure 3. Simplified equivalent circuits of: (a) the dSiPM pixel, (b) the TDC, and (c) the validation logic.

From: <u>I. Diehl et al 2024 JINST 19 P01020</u>

IV Curves & Dark Count Rate

Basic Chip Characterization

- Detailed characterization performed on several samples (Chip4 shown in figures)
- IV & Dark Count Rate studies performed with controlled temperature (from -25 to 20 °C) and humidity (~ 0 %) in a dark environment
- Measurements compatible with expectations





DESY dSiPM Characterisations

Exploring the Potential of Digital SPADs

Studies possible thanks to digital features

- Effect of quenching transistor tuning in senor response
- Pixel masking: effect on IV and DCR reduction
- Pixel crosstalk characterisation: studying the correlation between avalanche position and CT probability in neighbours



Crosstalk studies as function of avalanche position



DESY. |4D-Tracking with Digital SiPM-IC PM2024 | Gianpiero Vignola 28-May-2024

DAQ System in Test Beam

AIDA TLU Core





hitmap





§0

Plastic scintillator with a hole used as VETO for Trigger

- · Anticoincidence with other scintillators
- Trigger only in a ROI slightly larger than DUT
- · Allows to save disk space and maximize yeld



Material budget image for DUT alignment

Corryvreckan modules: [TrackingMultiplets] [AnalysisMaterialBudget]

Material Budget Image (AAD)



AAD(kink) [mrad

3.5

2.5

1.5

0.5





TestBeam data reconstruction

Using Corryvreckan Framework

- Corryvreckan use hit ^(c) (pixels above threshold) and Clusters ^(c) (groups of adjacent hits) to reconstruct particle trajectories.
- DUT response is then investigated on associated events





SiPM-IC tesbeam setup



- Real Track
- Hit
- Cluster
- Cluster center
- Reconstructed
 Track
- Residuals

http://cern.ch/corryvreckan



dSiPM + LYSO Sr-90 Data

Random Selection (100, 200, 500 from the top)

Overvoltage ~1.5 Temperature on Chip ~25C

