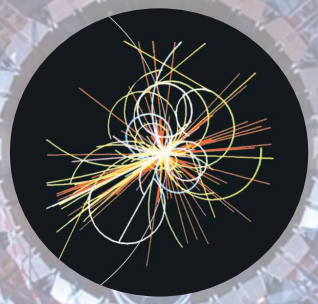
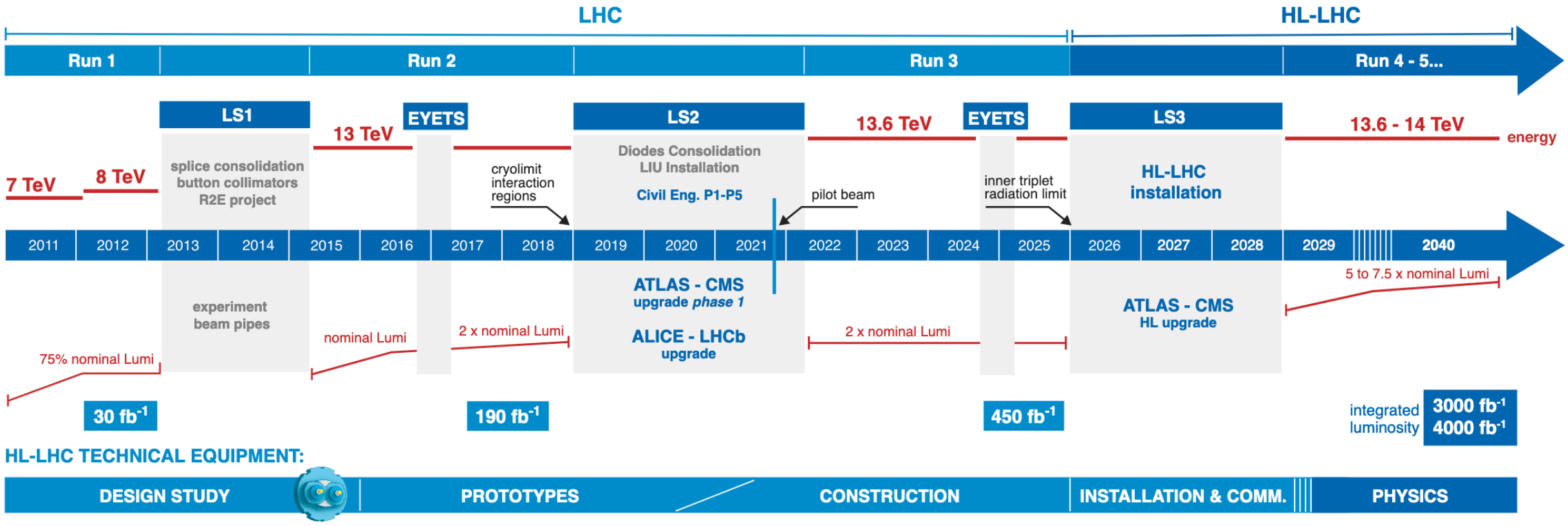
The Upgrade of the CMS Tracker for the High Luminosity LHC

Anna Macchiolo
University of Zurich
on behalf of the CMS Tracker group

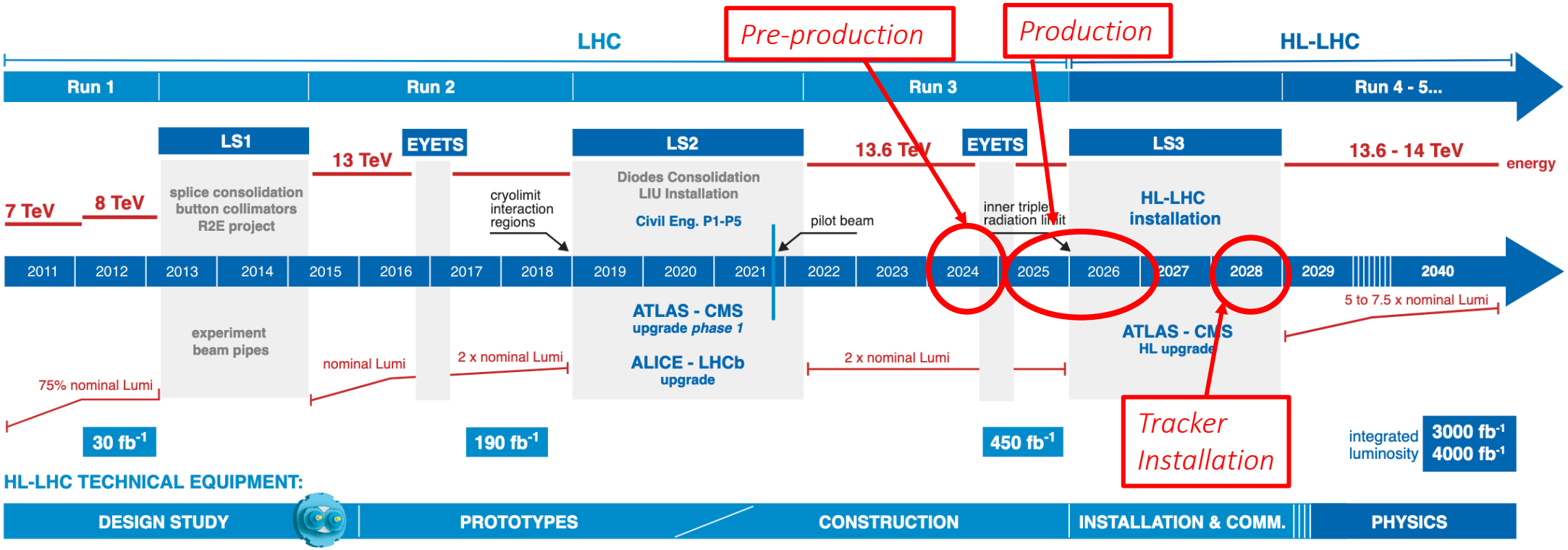


16th Pisa Meeting on Advanced Detectors, Elba,27 May 2024

LHC / HL-LHC Plan



The roadmap for the CMS Tracker at HL-LHC

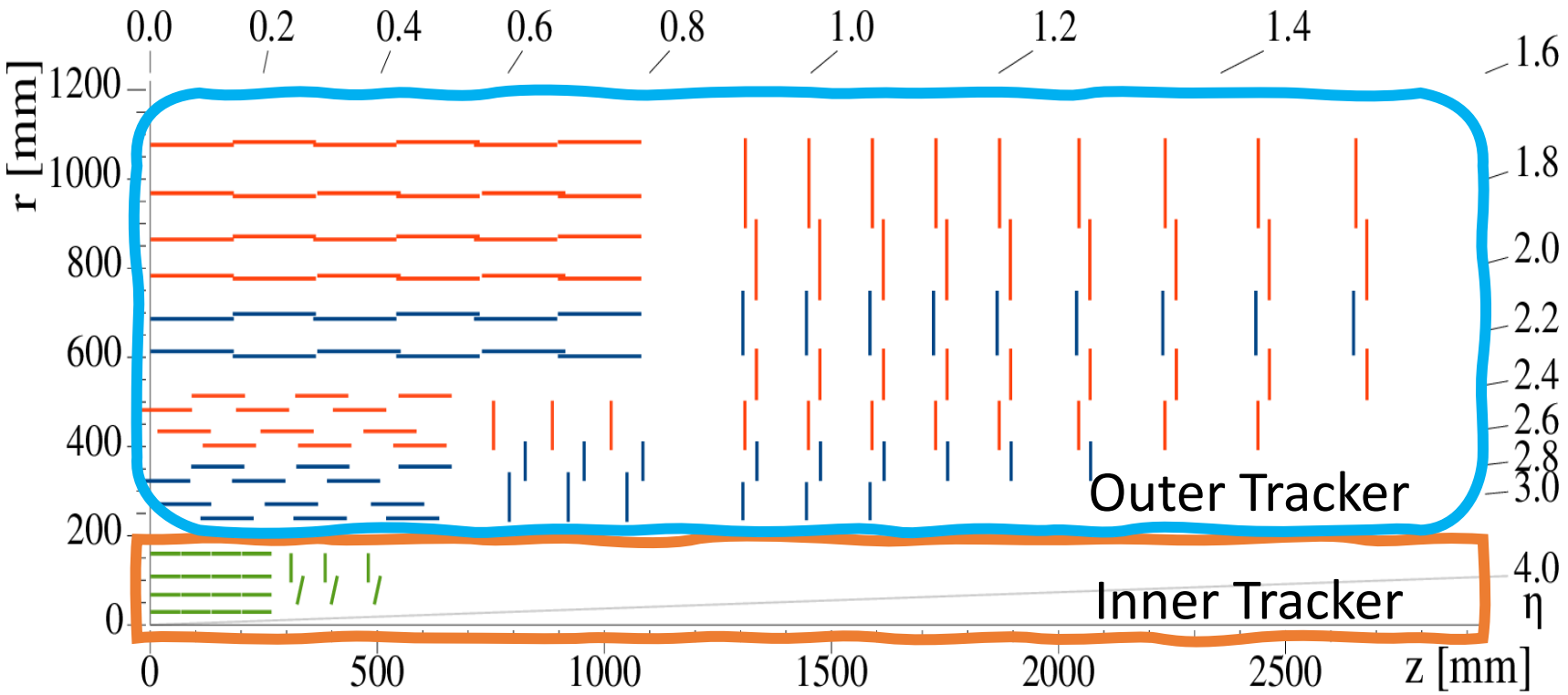


The new **HL-LHC** upgrade environment:

- Luminosity @ **5-7 x 10^{34} $cm^{-2}s^{-1}$**
- Pile-up to **<μ>** = **200** (4x times more than Phase 1)
- Integrated luminosity $\geq$ 3000 **fb^{-1}** (~10x times more than Phase 1)

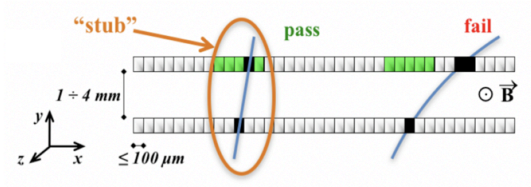
The present CMS Tracker

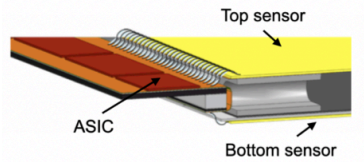
- **StripTracker**
  - ≃ 9.3x10⁶ strip channels (198 m²), Mono-phase cooling
- **Pixel system**
  - ≃ 125x10⁶ pixels (~1.9m²) , Bi-phase CO_2 cooling

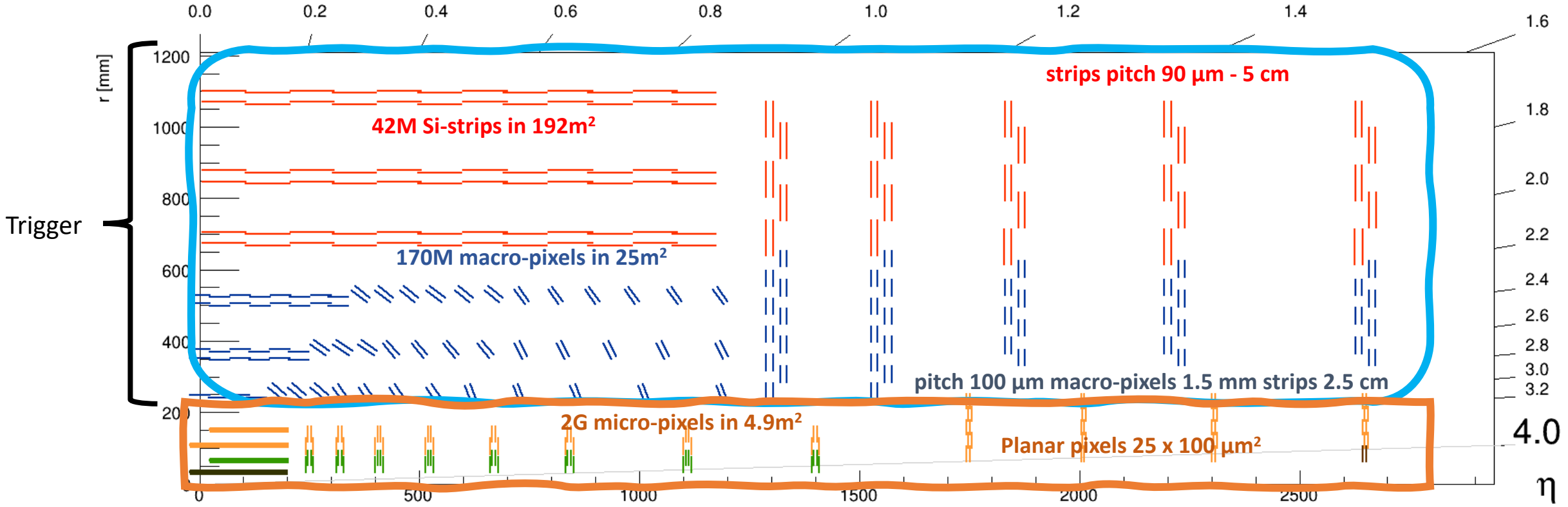


Phase-2 Tracker

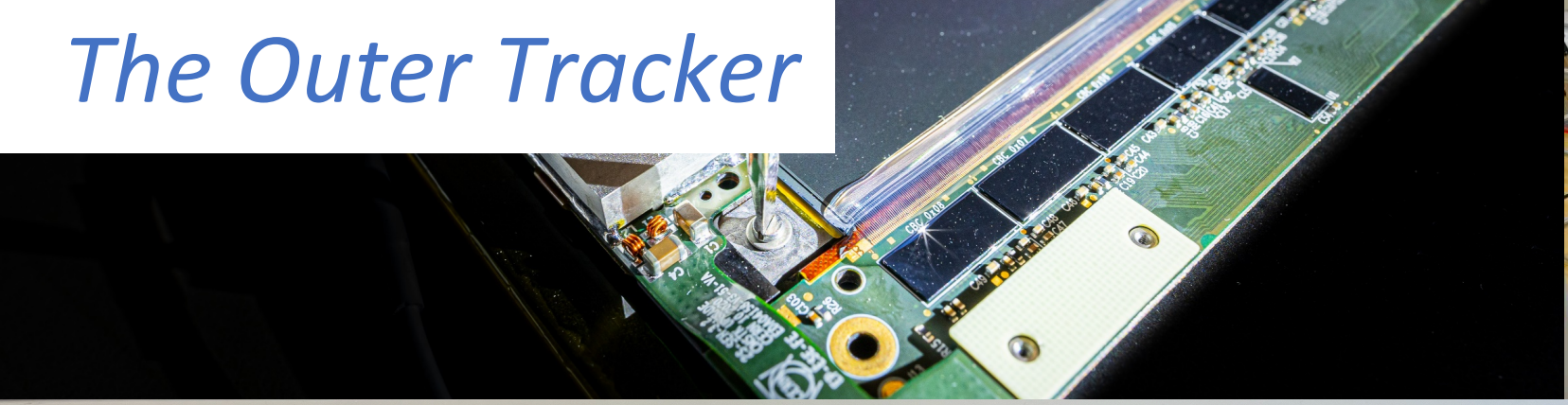
- **Outer Tracker design driven by ability to provide tracks at 40 MHz to L1 trigger**
  - ≃ 200 m^2 – 200x10^6 channels
  - Track stub / double sided p_T module @ bunch crossing rate of 40 MHz
  - Track finding for L1 implemented in FPGAs
  - Tilted geometry
- **Inner tracker with extended coverage in pseudo-rapidity**
  - ≃ 4.9 m^2 - 2x10^9 channels
  - Innermost layer at 2.8 cm (2.9 cm in Phase-1) from beam pipe but same occupancy as in Phase-1 (~2x10^{-3})
  - One replacement foreseen for innermost layer in the barrel and first ring in the disks of the forward system at a fluence of 1-1.5 x10^{16} n_{eq}/cm^2

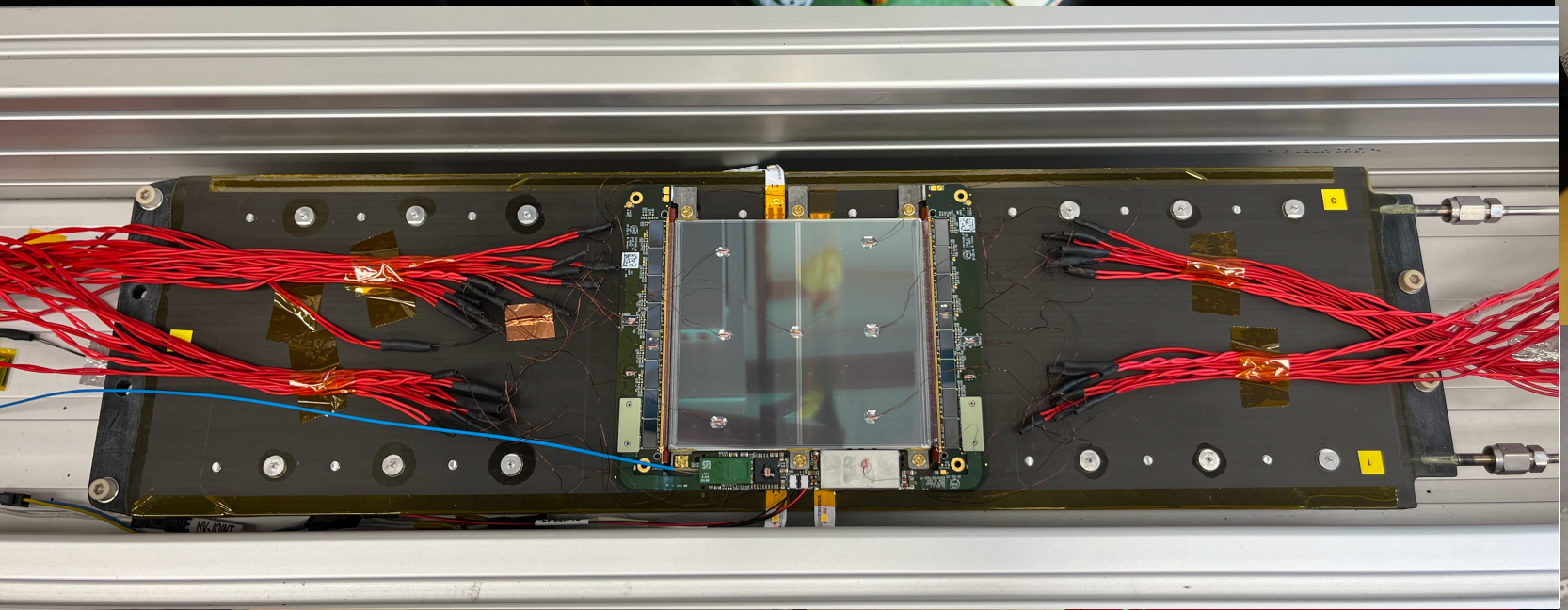






The Outer Tracker



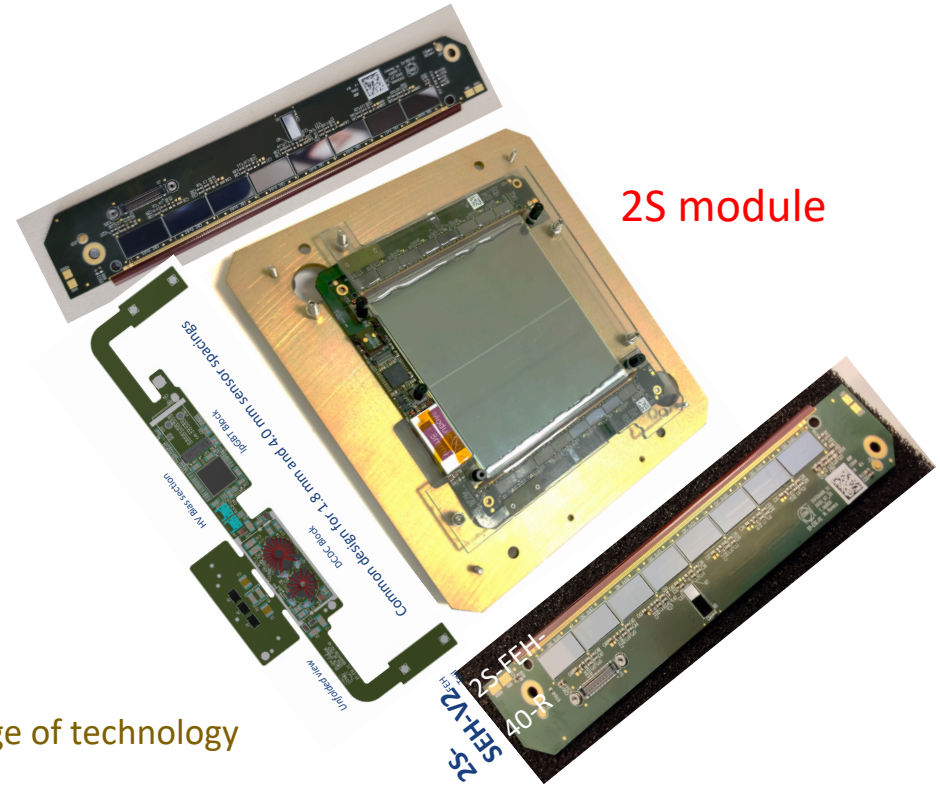


Outer Tracker module concepts

Modules provide p_T discrimination in front-end electronics

New concept

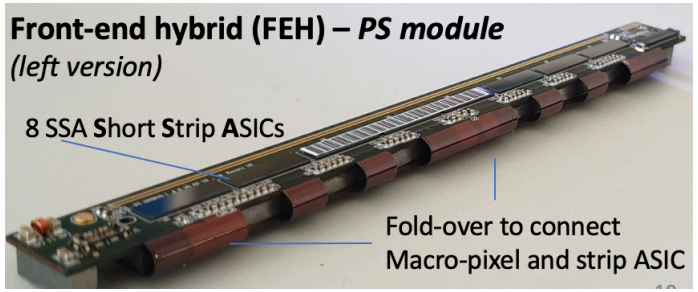
- Tag high p_T segments locally on the same module
- Contains ALL electronics = full system
- Effective way to have 2 space points in single mechanics – lightweight
- Frontend electronics gives Level-1 track finder 'vectors' instead of points

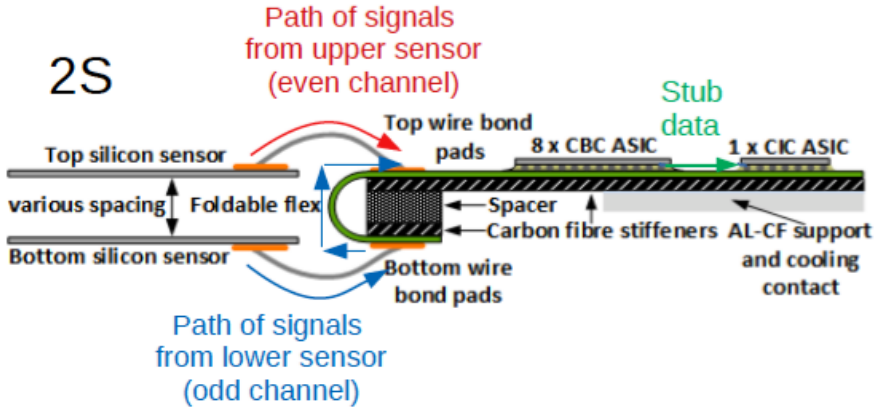


Hybrids at the edge of technology

Hybrids with fold-over:

- Allow to wire-bond both sensors to the same hybrid
- Provide adequate stiffness for wire bonding
- Minimize material
- **Complicated fabrication and delicate part!**





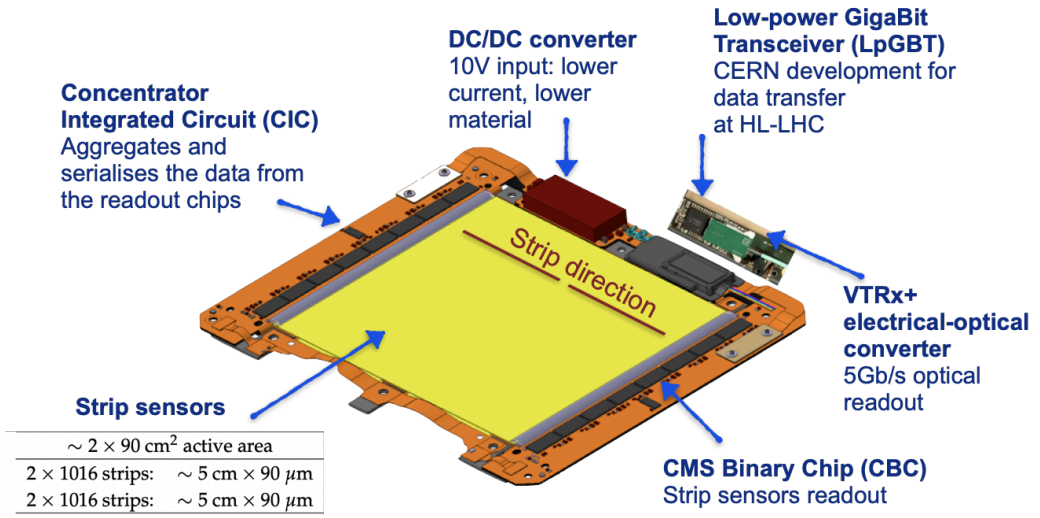
2S and PS modules: design and production

Strip-strip (2S) module

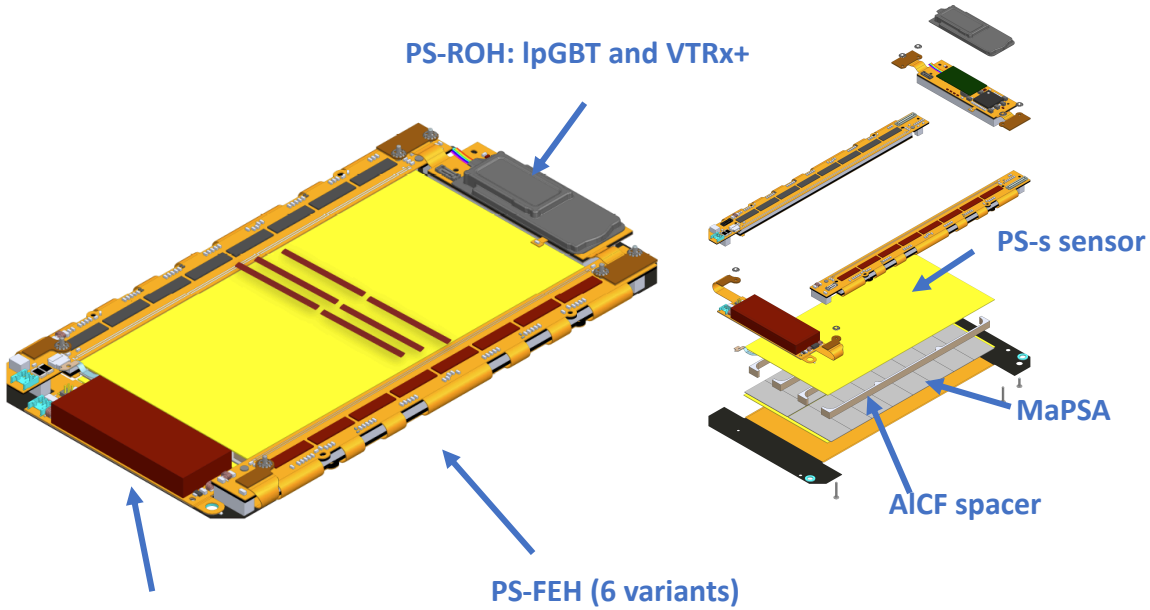
- 2 AC-coupled strip sensors
  - 10cm x 10cm (5cm long strips, 90µm pitch)
- 2 sensor spacings: 1.8mm* and 4.0mm
- R> 60 cm

Pixel-strip (PS) module

- AC-coupled strip sensor
  - 5cm x 10cm (2.5cm long strips, 100µm pitch)
- Macro-Pixel Subassembly (MaPSA)
  - DC-coupled pixel sensor (1.4mm long macro-pixels, 100µm pitch) bump bonded to 16 MPA chips
- 3 sensor spacings: 1.6mm, 2.6mm* and 4.0mm
- R< 60 cm



$\sim 2 \times 90$ cm^2 active area	
2×1016 strips:	~ 5 cm $\times$ 90 μm
2×1016 strips:	~ 5 cm $\times$ 90 μm

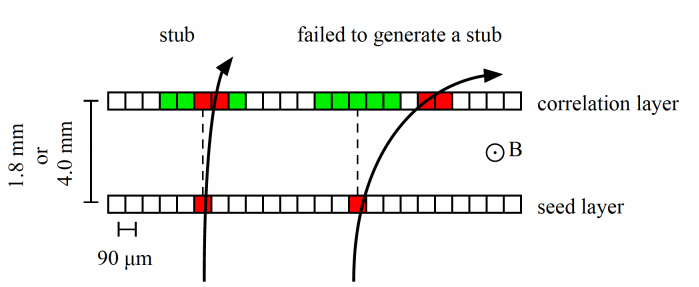


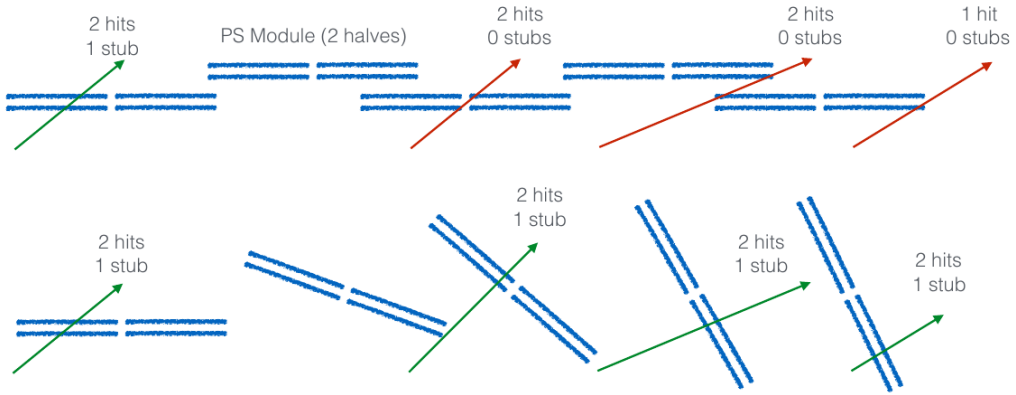
- **Good noise performance found with pre-series PS and 2S modules**
- **Almost all components are in pre-production or production**
- **Module design is final**

See Poster by I. Margjeka: *Noise and performance tests results of the PS modules for the phase-2 CMS outer tracker*

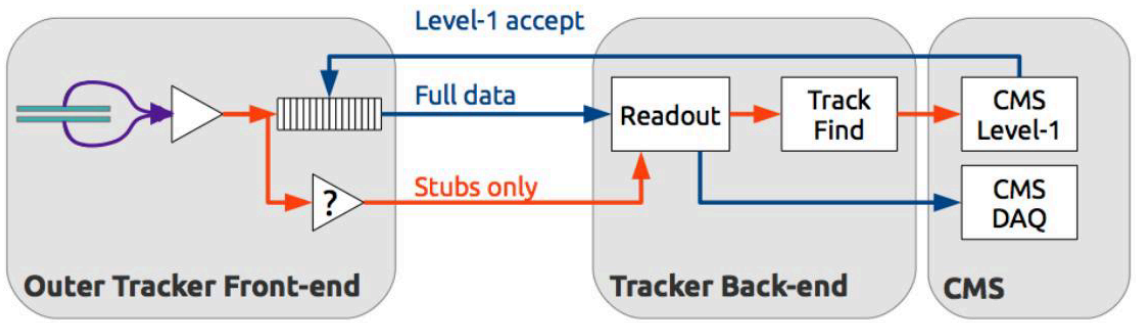
OT modules for the L1 Track Trigger

Programmable window ➔ p_T threshold for stub selection



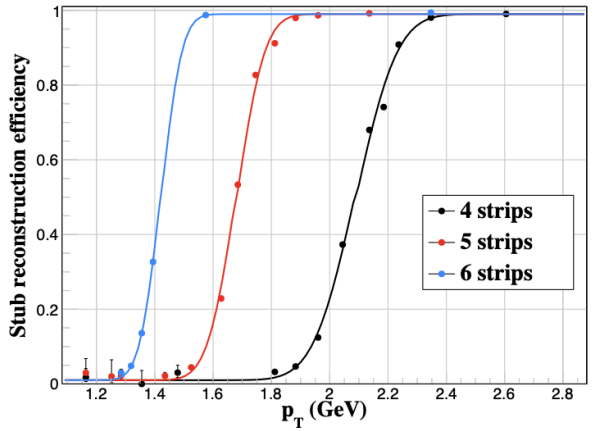


Two simultaneous data-streams
– Stub read-out at the full 40MHz rate
– Full data read-out at up to 750kHz



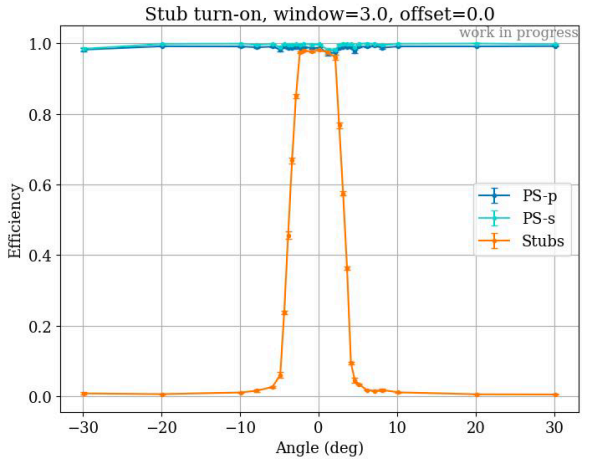
I. Zoi, https://doi.org/10.22323/1.448.0021

Stub efficiency for 2S prototypes



D. Rastorguev, BTTB12 20024

Stub efficiency for PS prototypes

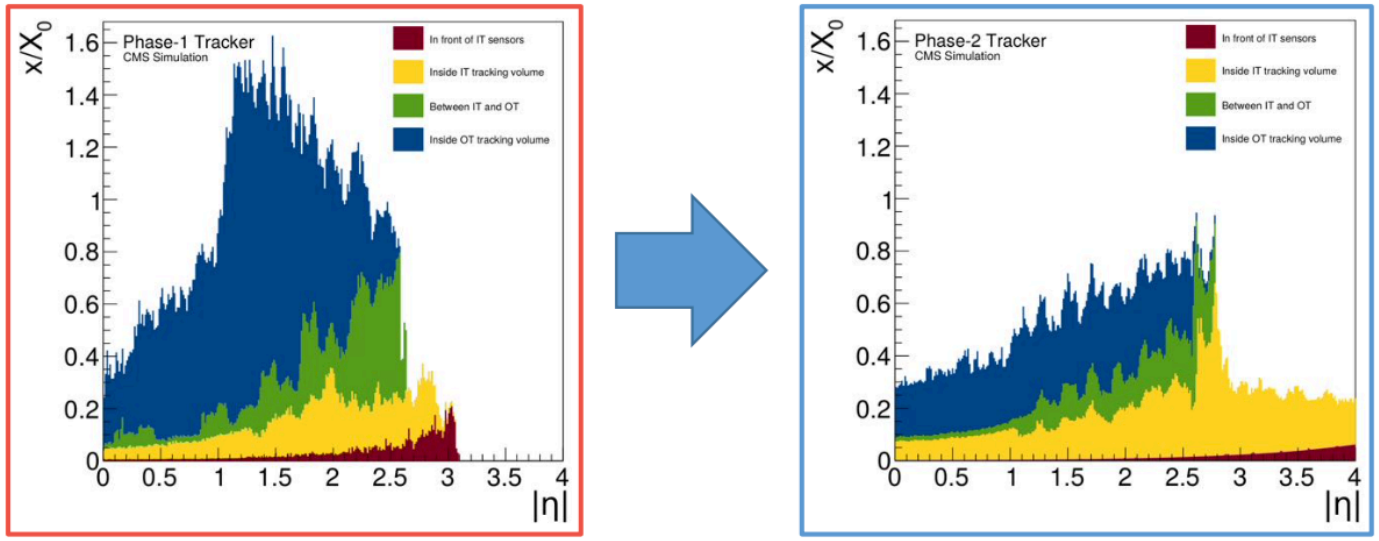


See poster by D. Monk: 40MHz Readout of CMS Silicon Modules in a High Intensity Beam

Clustering → Correlation between two planes → Discrimination by a given window → if passed: a **stub** is generated → Stubs are sent out via dedicated low-latency data path

$$\mathcal{E}(\text{Stub}) = \mathcal{E}(\text{PS-p}) \cdot \mathcal{E}(\text{PS-s}) \cdot \mathcal{E}(\text{Acceptance})$$

Material budget and mechanics

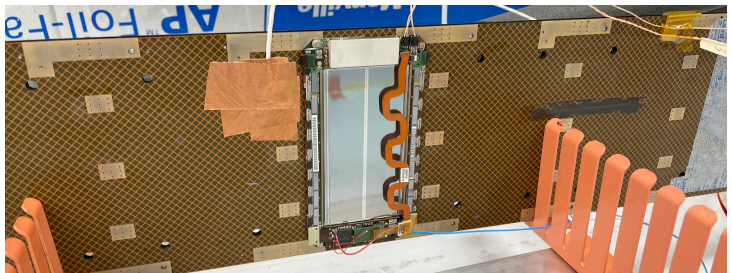


- *DC-DC converters – fewer cables*
- *Fewer layers*
- *Lighter materials*
- *Optimized service routing – 3D modelling*
- *CO_2 bi-phase cooling – thin pipes*
- *Inclined geometry*

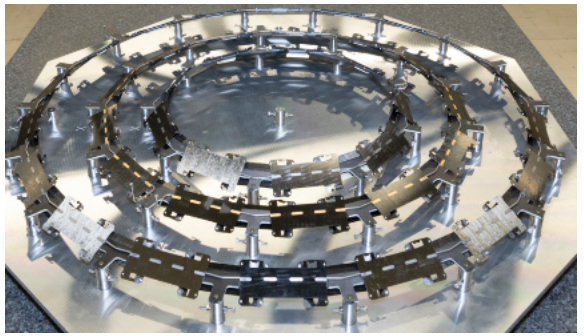
CMS Tracker TDR, ***CERN-LHCC-2017-009***

2S ladder

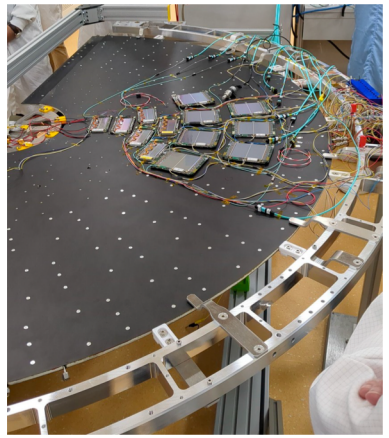
PS module on TBPS plank



OT tilted rings



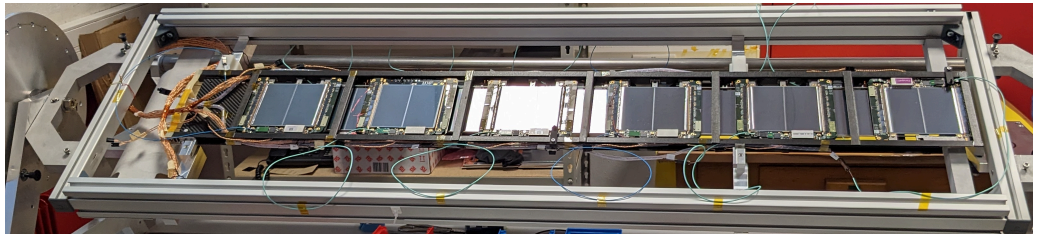
OT endcap dee



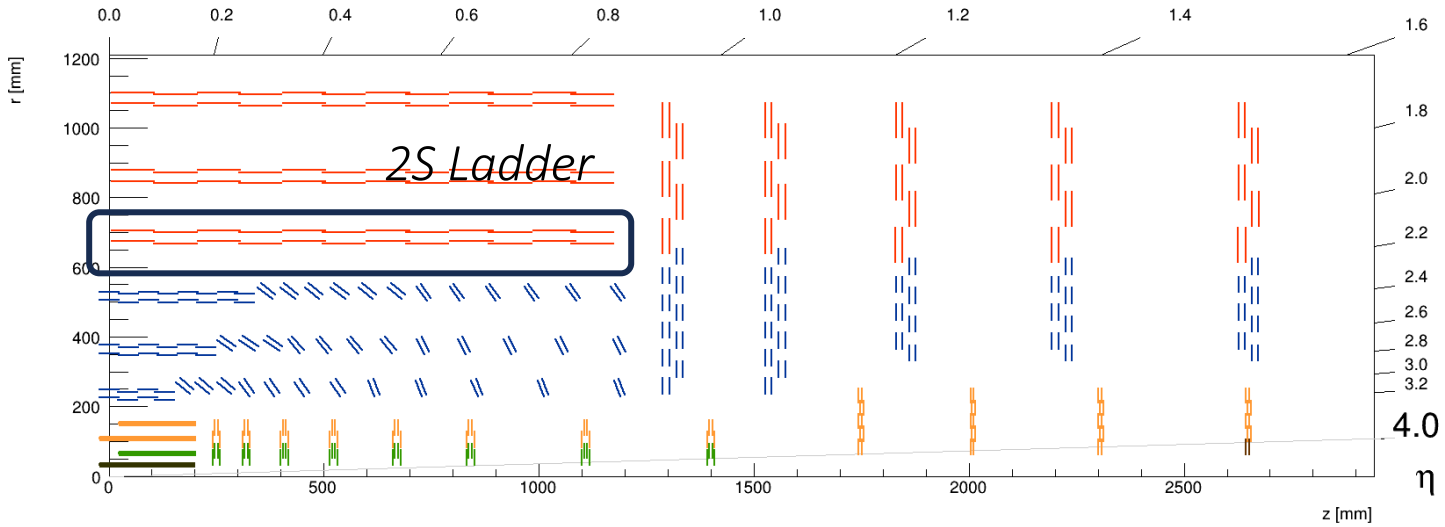
Carbon foam layer 3 end ring pieces

All OT mechanical support structures in pre-production or production

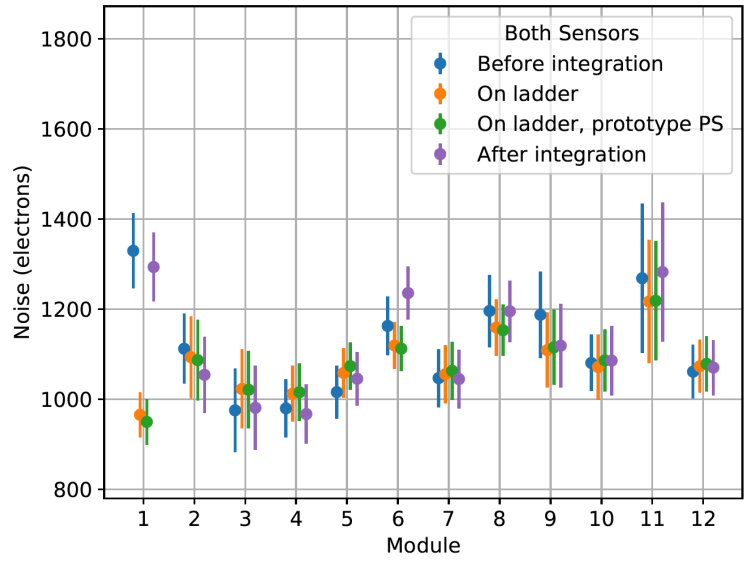
OT System tests – 2S ladders



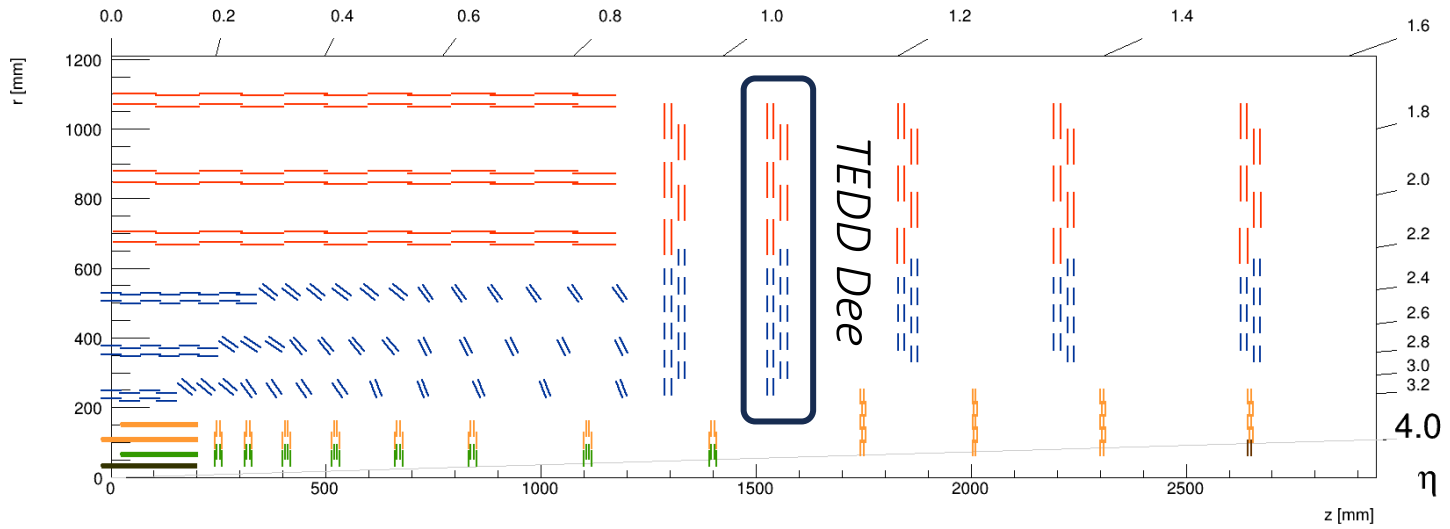
- 12 2S modules on a ladder with prototypes of electrical and optical services:
  - Prototype power supply for the Phase-2 Tracker with 60 m long cable
  - Module noise shows no significant increase on the ladder compared to the measurement before integration
  - No noise degradation throughout integration test



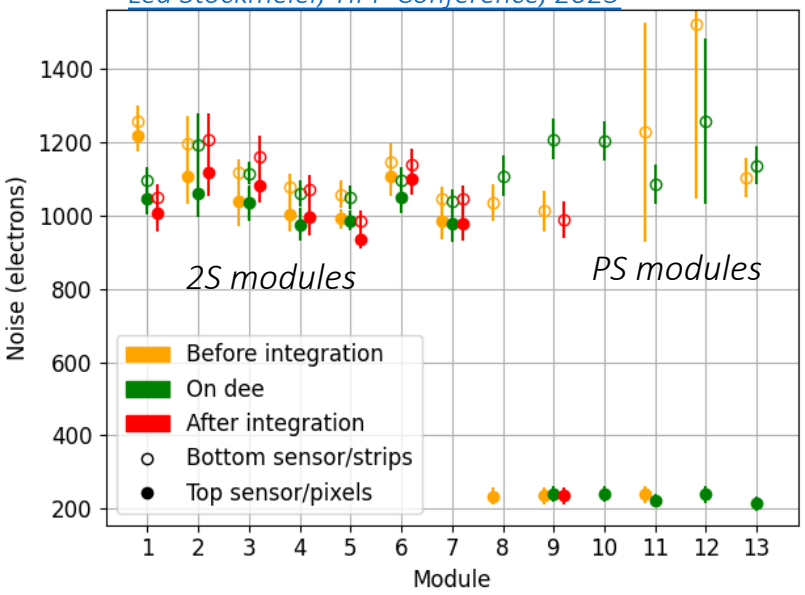
Lea Stockmeier, TIPP Conference, 2023



OT System tests – TEDD Dee

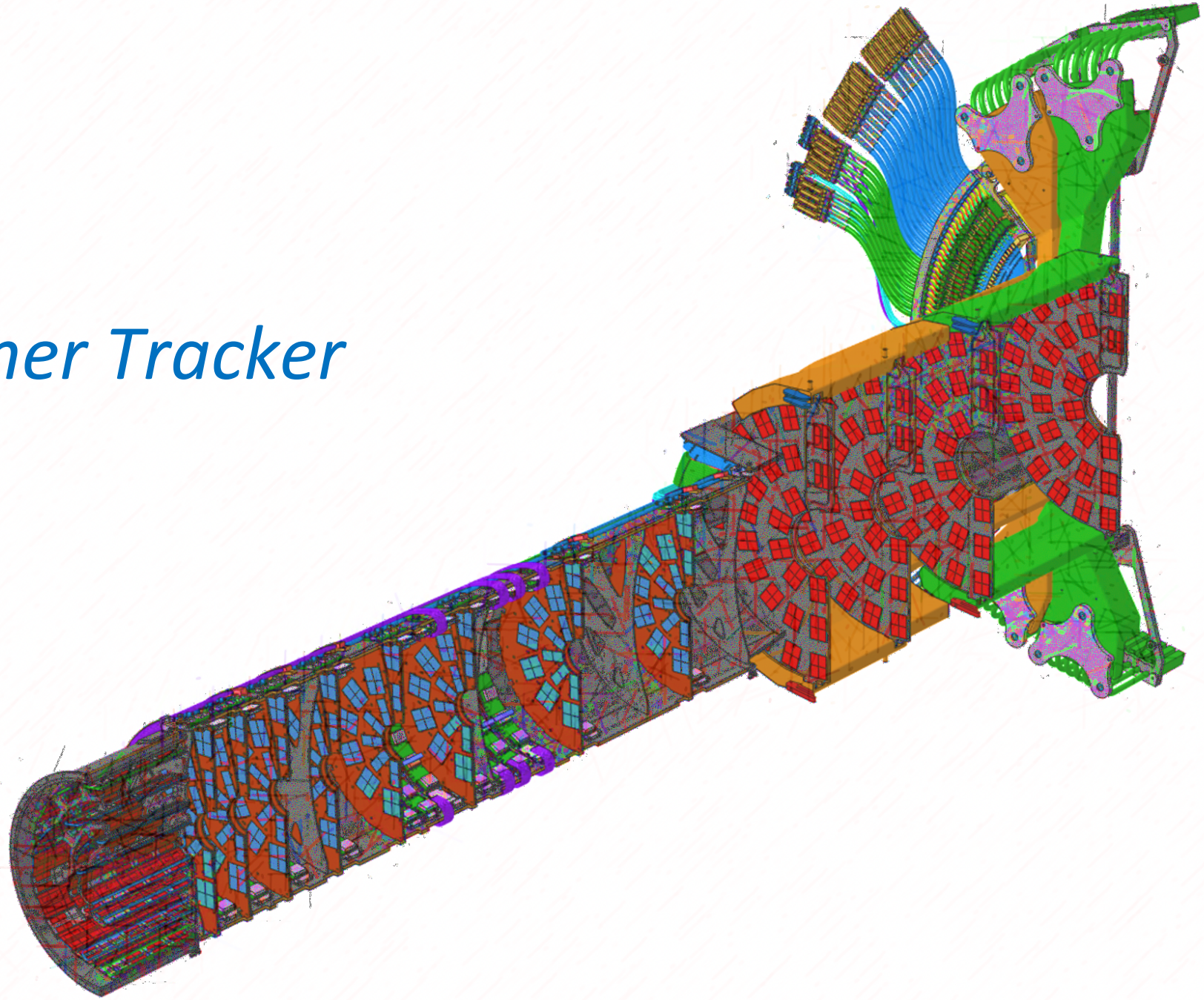


Lea Stockmeier, TIPP Conference, 2023

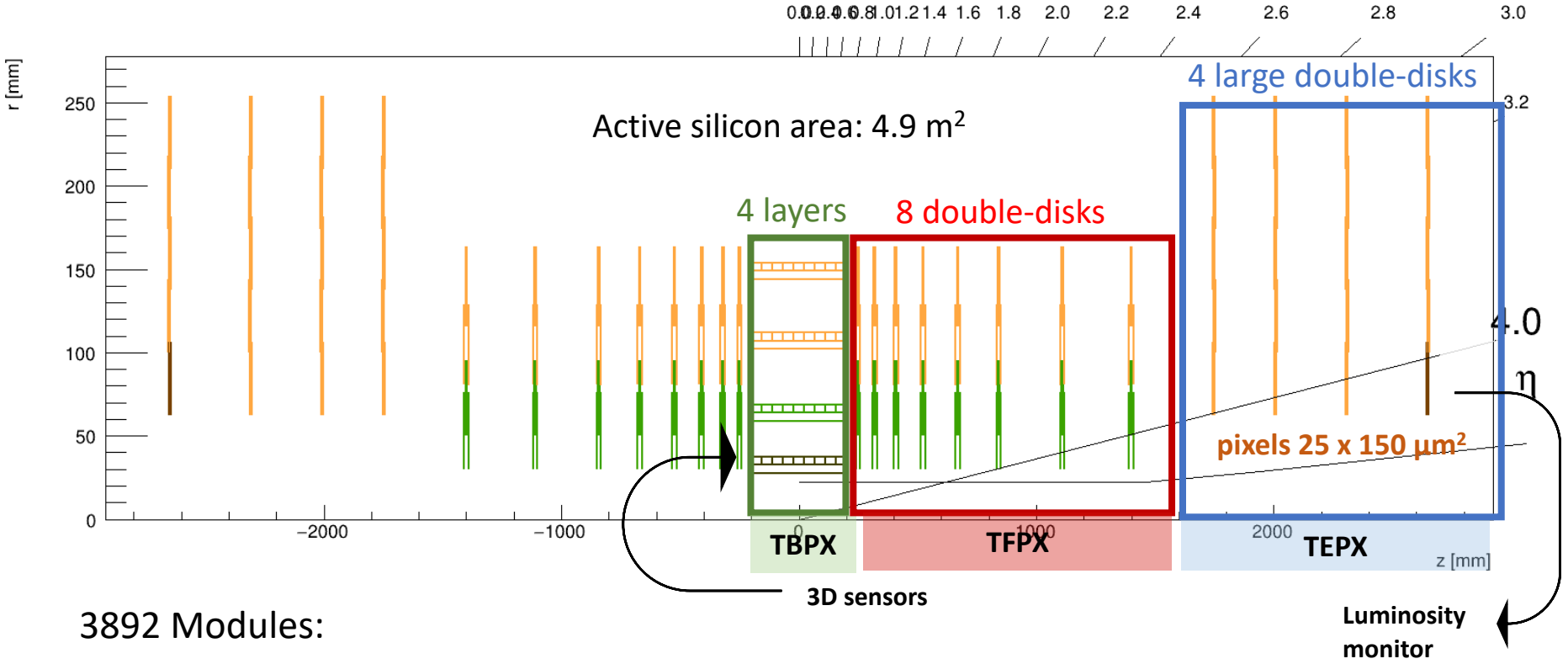


- 13 2S and PS modules on a TEDD half disk:
  - PS module noise different in some cases, due to prototype-specific known issues
  - 2S module noise shows no significant increase on the dee compared to the measurement before integration
- Outlook
  - Further integration tests planned
    - With final modules
    - With final support structures

The Inner Tracker

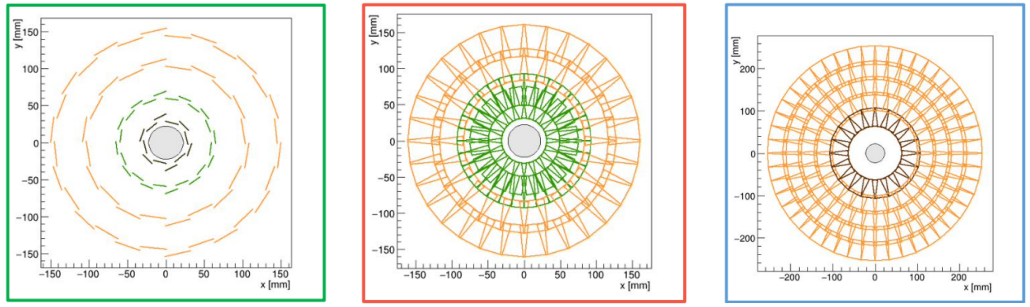


Inner Tracker for Phase-2

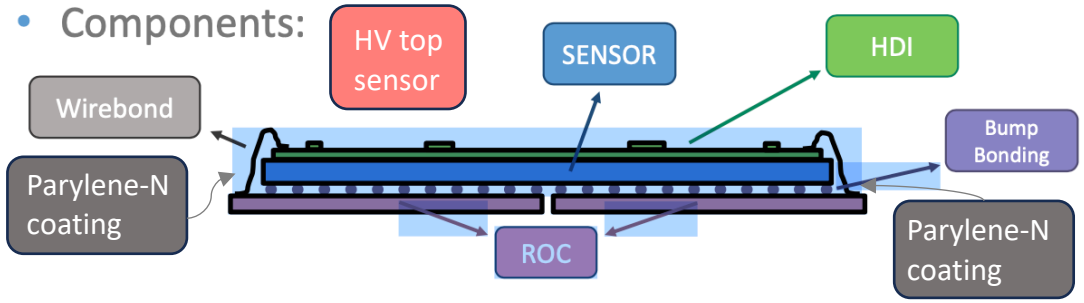


3892 Modules:

- Read Out Chip (ROC) only active element on module
- (1156) 1x2 ROC module and (2736) 2x2 ROC module

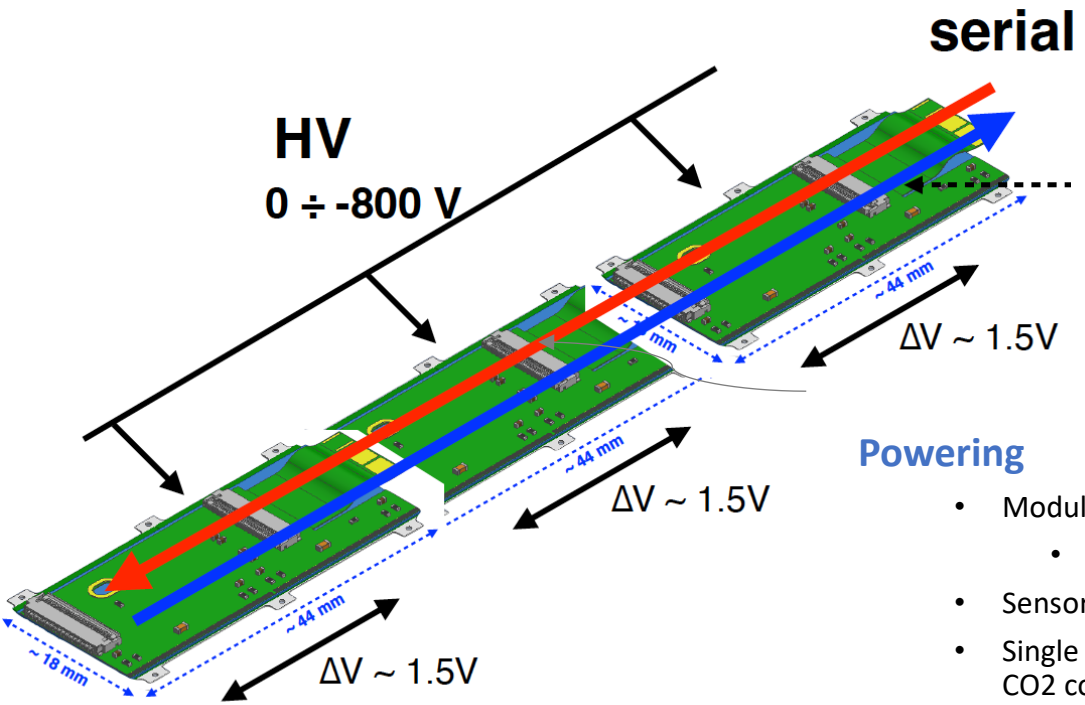


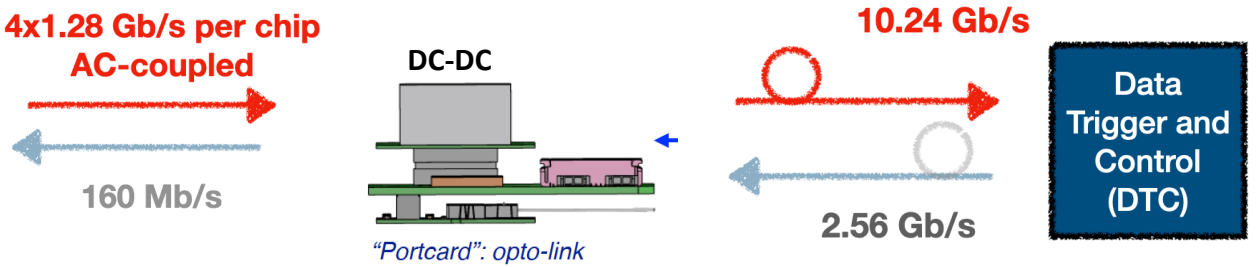
- Components:

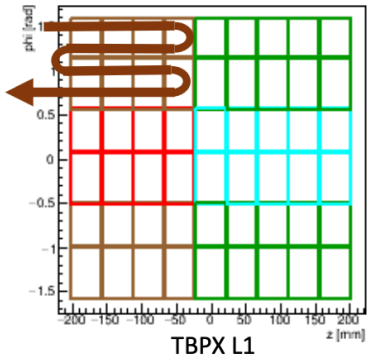


IT Electronics system architecture

Innovation - new technology 65 nm TSMC ASIC enabling 50(25) x 50(100) µm² pitch at ≃ **3 GHz/cm²** (inner layer)
Innovation - *serial powering* - only way to power 50 kW detector with reasonable material budget







Powering

- Modules grouped in 576 serial power chains, up to 11 modules in a chain
  - Modules powered in series, chips within each module powered in parallel
- Sensor bias following the serial power chains with single return line
- Single power supply module: current source (SP), HV for sensor (0-800V), LV for portcards and pre-heaters required by CO2 cooling

Readout/communication

- Hit rate ~ 3 GHz/cm² (inner layer), trigger latency 12.8 µs → ASIC buffer length
- Modules to LpGBT Up to 6 electrical up-links at 1.28 Gb/s
- LpGBT to Module One electrical down-link at 160 Mb/s

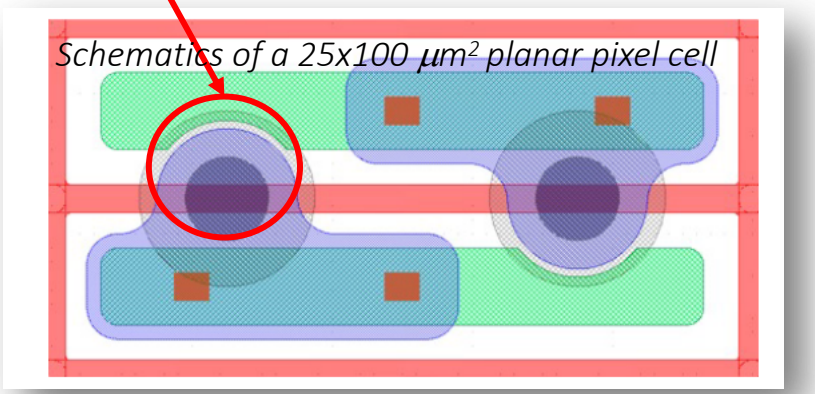
Pixel sensors

- 150 μm bulk thickness, 25x100 μm^2 pixels cells everywhere
- Planar n-in-p sensors:
  - Bias up to 600V and spark protection between ROC and sensors
  - Bump bonding pattern is 50x50 μm^2
    - Production started at HPK

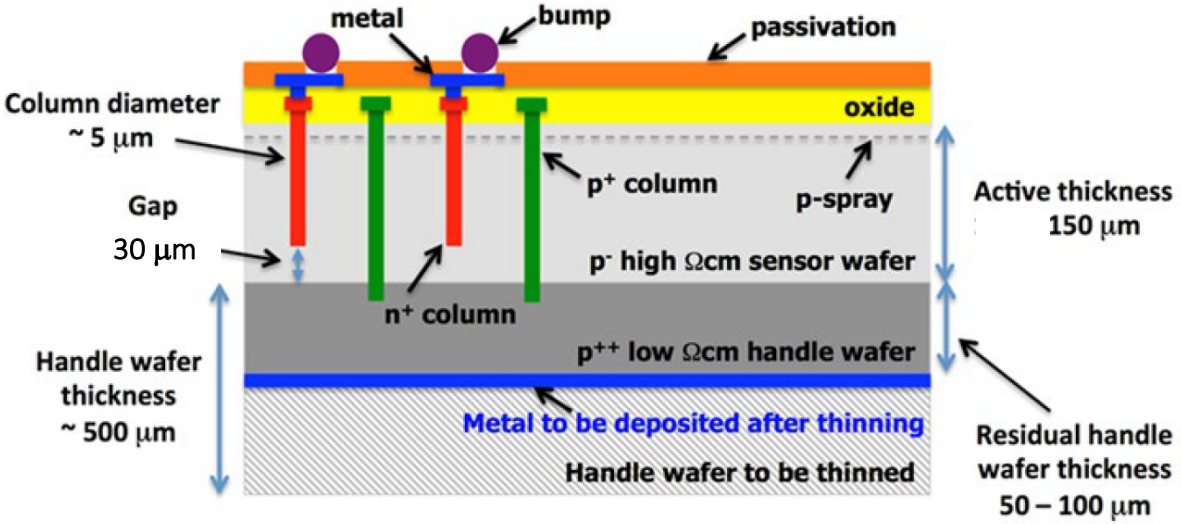
- 3D sensors for barrel L1
  - Short drift distance ~50 μm (3D) vs 150 μm (Planar)
  - Slim edges (150 μm) vs planar (~450 μm) → smaller dead zone
  - Sensors pre-production well under way at FBK on 6" wafers

See characterization results before and after irradiation in the posters by D. Zuolo (3D Sensors) and B. Raciti (planar sensors)

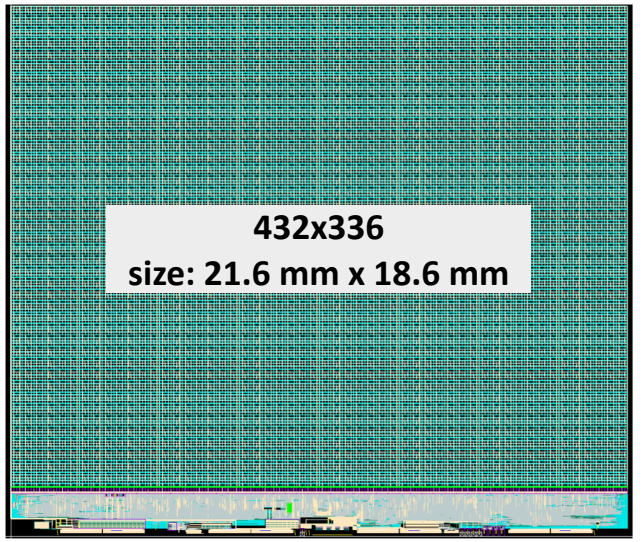
No n$^+$ implant under metal to reduce x-talk



Structure of a 3D sensor – FBK process



The CMS IT read-out chip

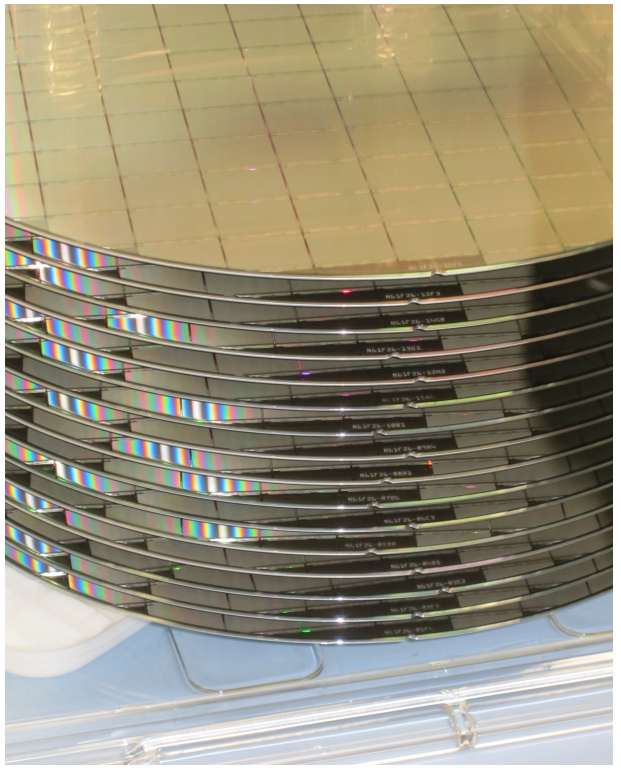


Designed by the RD53 collaboration

- 65 nm CMOS technology (current detector 250 nm)
- Radiation hard at least up to 0.5 Grad
- 50 x 50 μm^2 pixel size → compatible with 25 x 100 μm^2 pixel size on sensors
- A shunt-LDO (SLDO) on each chip provides voltage regulation for each chip while maintaining a constant current
- 4 data links per chip at 1.28 Gb/s using Aurora encoding
- Data merging: read-out of up to three secondary chips through a primary one in the same module → reduction of data lines in low-occupancy layers

First engineering run delivered in January with a preliminary estimation of the yield at 77%

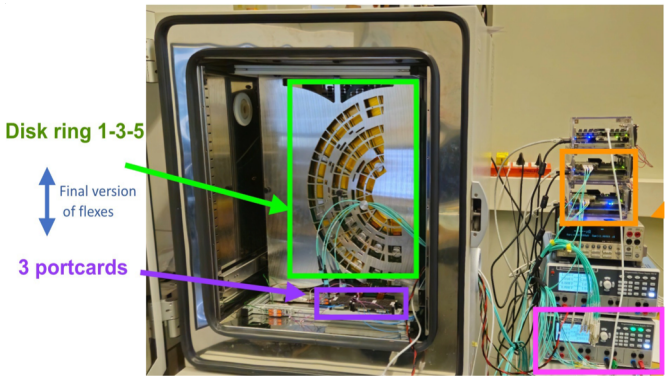
See poster of M. Grippo: First results on the final readout chip for the High-Luminosity LHC upgrade of the CMS Inner Tracker



- Test of the CROCv2 chips is on-going with digital (no-sensor) modules while waiting for the pre-production modules (~ August 2024):
  - Good performance observed up to now (bugs on data merging affecting CROCv1 have been fixed)
  - More detailed characterization after irradiation will follow

System tests – Data integrity

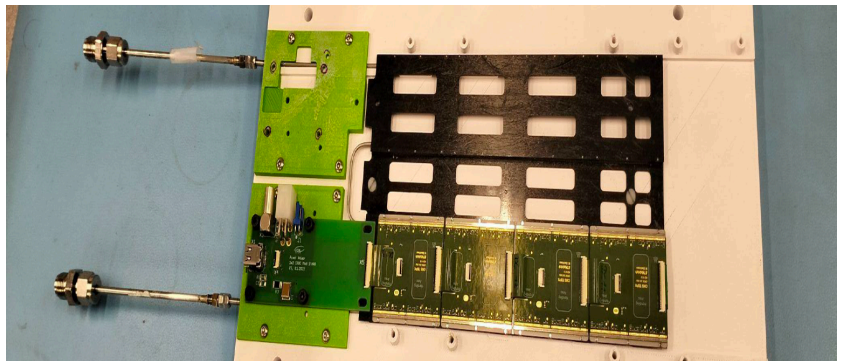
TEPX Disk PCB with digital quad modules



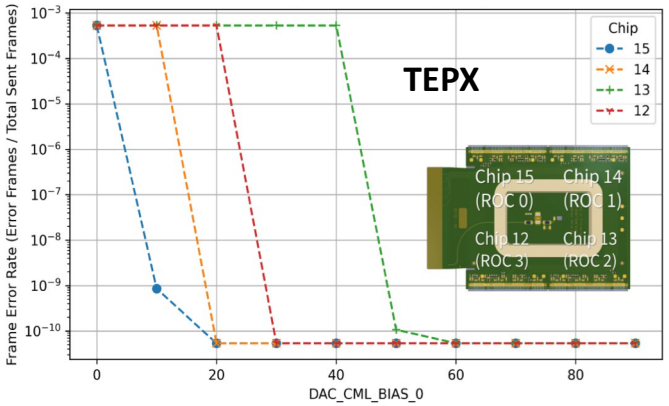
- Test of the data transmission through the electrical and optical stages with modules powered in serial mode for the three subsystems
- Data integrity (Bit error rate) is studied as a function of a programmable overshoot to compensate for the signal attenuation in the transmission line

Target values of the Bit Error Rate achieved

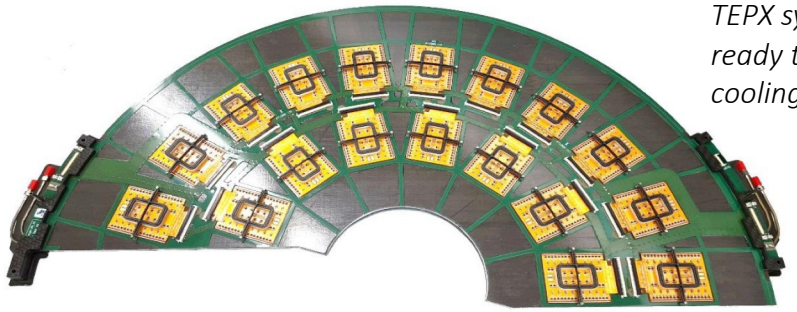
TBPX system test with modules mounted on L4 ladder



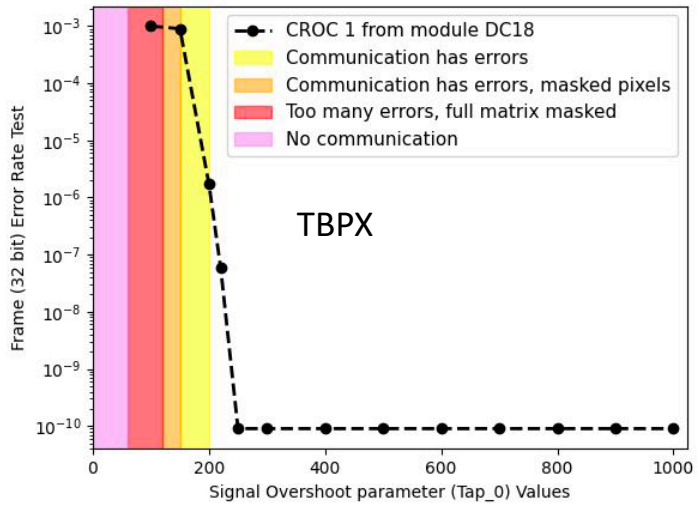
Bit Error Rate vs Signal overshoot



TEPX system test with half-disk ready to be connected to CO2 cooling system for thermal tests



Bit Error Rate vs Signal overshoot



G. Bardelli, IFAE 2024

- Under planning: tests of substructures with final components to ultimately validate the electronics and thermal performance

Conclusions

- Design of the new CMS Tracker for Phase-2 driven by the inclusion of the Outer Tracker in the decision forming process for the L1 Trigger
- Highlight of the Inner Tracker is increased granularity and extended acceptance in the forward region from $|\eta|<3$ to 4

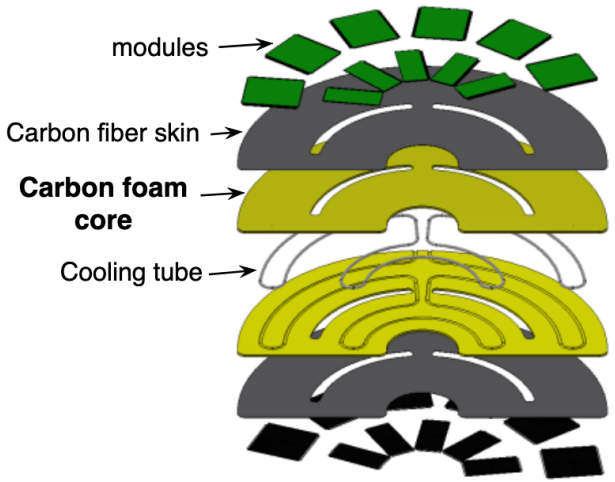
- Most of the components for Inner and Outer Tracking are in production or pre-production phase
  - With the delivery and testing of the final version of the CROC ASIC for the Inner Tracker, all the Tracker ASICs have been validated and have entered production

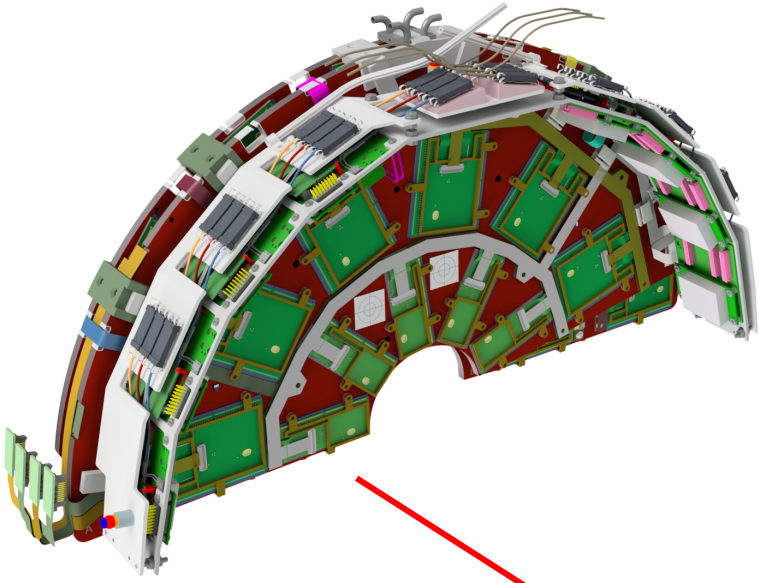
- System tests being conducted to validate all the components, powering, read-out and thermal performance of the sub-detectors

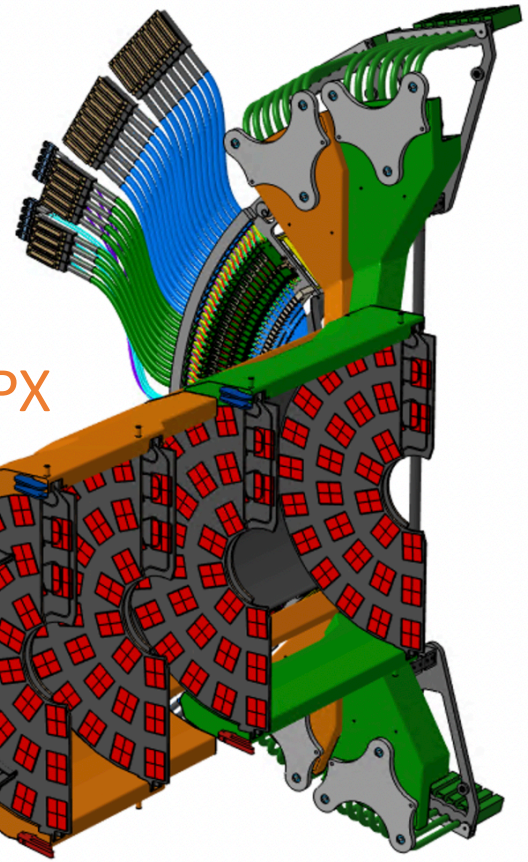
- Still many challenges ahead of us for the timely accomplishment of the production and integration steps and the achievement of the design performance

Additional slides

IT mechanics



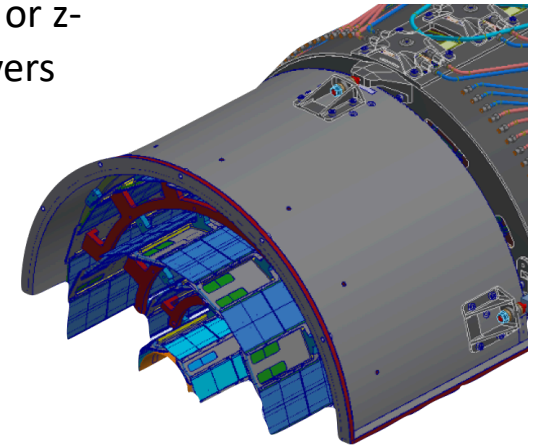




TEPX

TFPX

TBPX

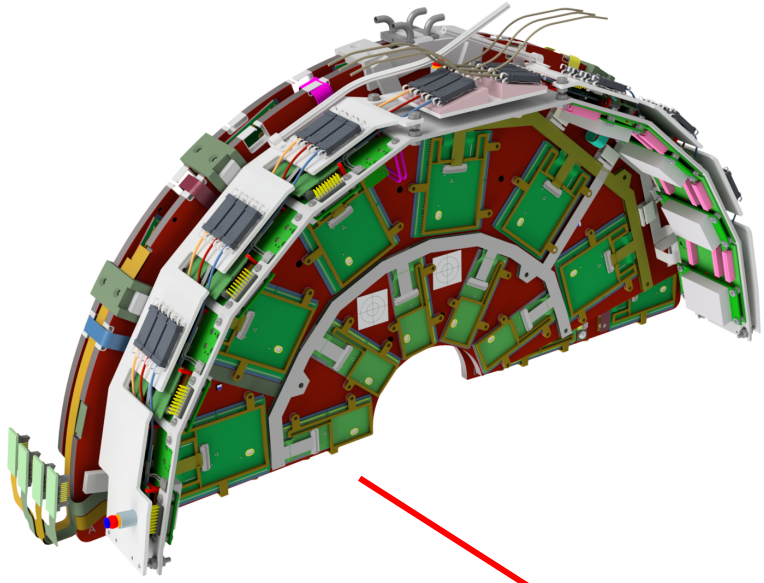


- Barrel split in half along z but at z!=0 → Central modules belong to z+ or z- half in consecutive layers

TEPX: Integrated PCB for powering and data read-out

IT mechanics

Light and simple mechanics: Inner Tracker can be removed for maintenance in an extended Year End Technical Stop



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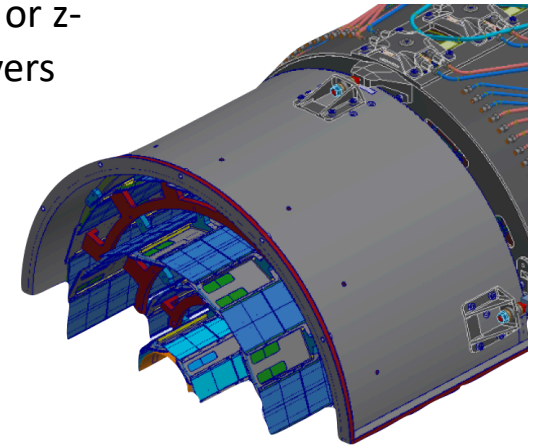

TEPX: Integrated PCB for powering and data read-out