Development of a Photon-to-Digital Converter in 65 nm

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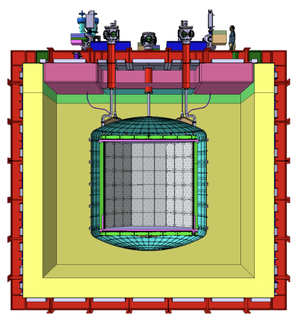
Research context

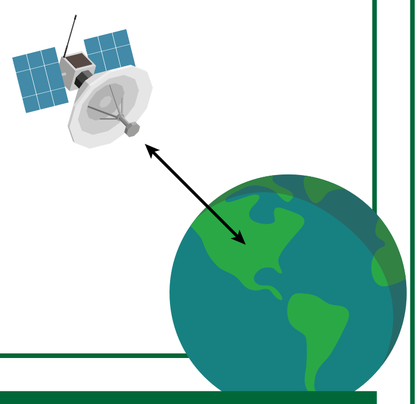
Research and development on 3D integrated Photon-to-Digital Converters (PDC) is motivated by the growing interest in high-energy physics, medical and quantum communication communities. High timing resolution on photon time-of-arrival (ToA) can help achieve precise vertex reconstruction [1].

Particle detectors [2] (e.g. accelerators, noble liquid experiments)



Medical imaging (e.g. ToF PET, ToF CT)

Quantum communication (e.g. Quantum Key Distribution)



Photon-to-Digital Converter

The Groupe de Recherche en Appareillage Médical de Sherbrooke (GRAMS), in collaboration with Teledyne DALSA Semiconductor, is developing a PDC aiming to timestamp photons with an RMS precision below 10 ps.

▶ PDCs adopt single photon avalanche diodes (SPADs) vertically integrated to a CMOS electronic readout layer.

▶ The first PDC prototype was developed in TSMC 180 nm technology. The detection layer includes an array of 64 × 64 SPADs and a custom wafer-to-wafer bonding technology is being developed.

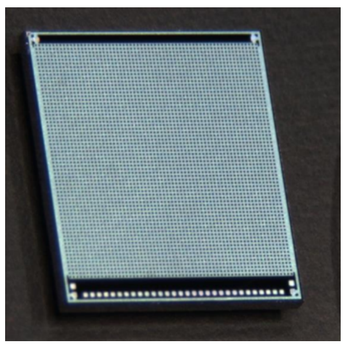


Fig 1a: 5 × 5 mm² die of one 64 × 64 SPAD array

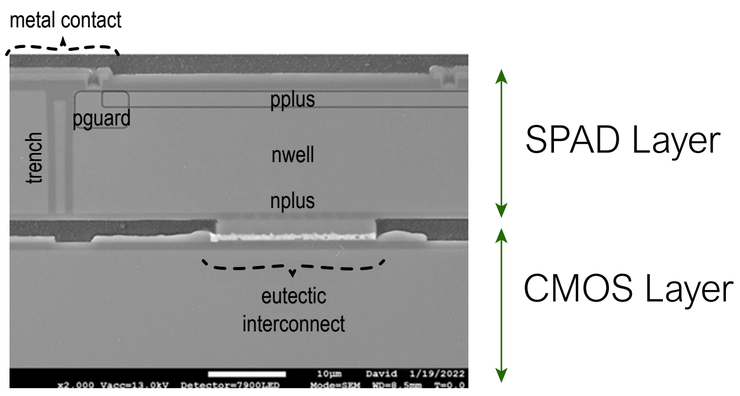


Fig 1b: Cross-section of wafer-to-wafer bonding

The 180 nm PDC outputs a digitized count of the number of SPADs that have been hit by a photon. A fast-OR signal at the output of the PDC starts a time-to-digital converter (TDC) that can timestamp to a timing precision below 100 ps. This timing precision makes this system the solution of choice for noble liquid experiments or pulse-shape discrimination analysis in low-energy particle detectors.

▶ For even more precise timing precisions, a 65 nm technology PDC is being developed. It will feature one TDC per 4 SPADs, implying 1024 TDCs for each PDC.

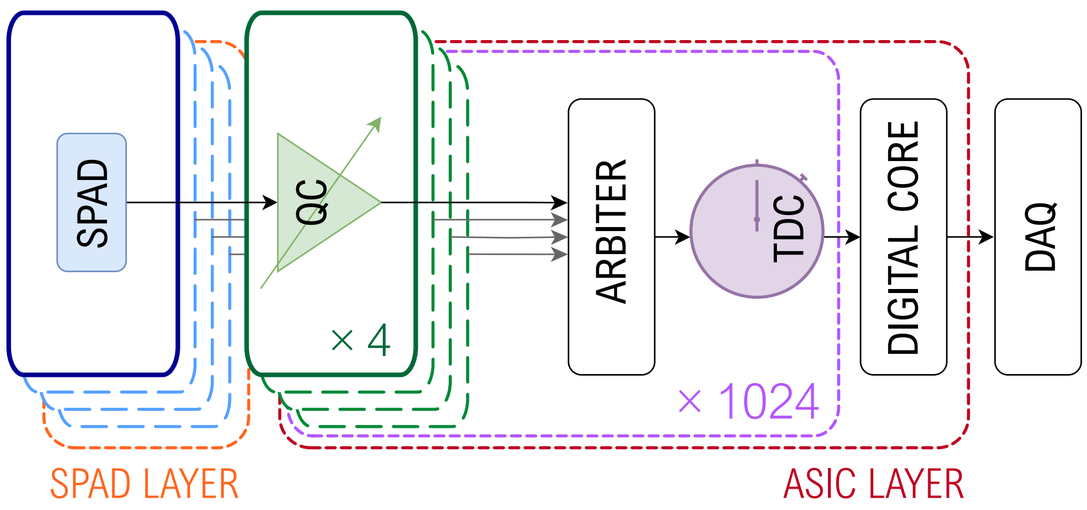


Fig 2: 65 nm PDC readout architecture

Prototype in 65 nm technology

A new test-chip prototype, designed in TSMC 65 nm LP technology, was developed. The ASIC comprises 2 arrays of 4 × 4 quenching circuits (QC). The test-chip aims to timestamp the ToA of the first photon impinging on a 2×2 SPAD subset of the array, with a timing precision below 10 ps.

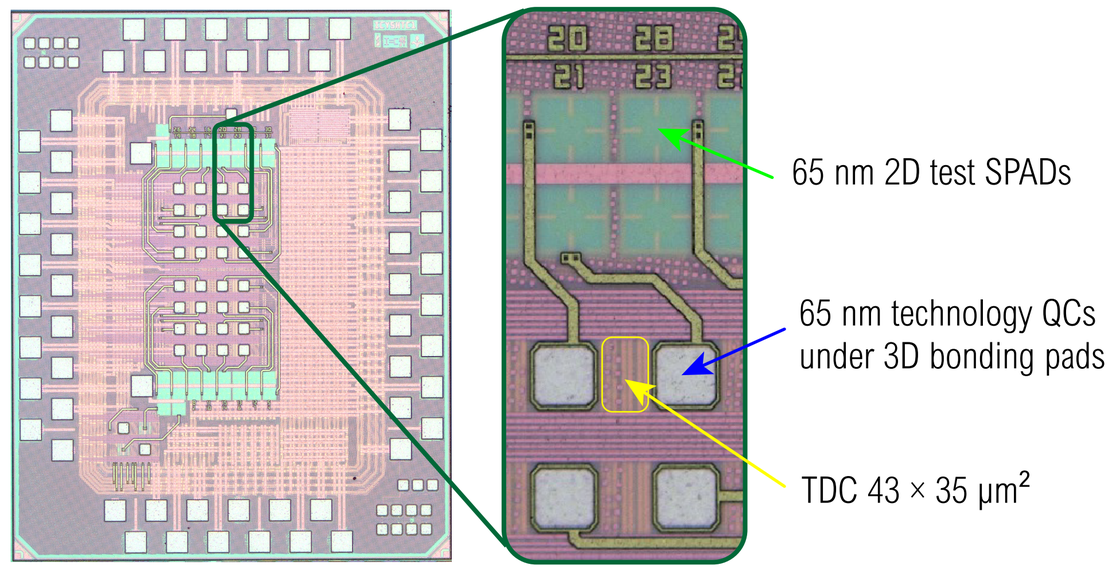


Fig 3: Microscope image of the PDC prototype with zoom in a 2 × 2 subset of the array

The QC adopts a configurable inverter as event discriminator. The first inverter is designed with a PMOS with switched fingers enabling the configuration of the threshold voltage. Considering the requirement for precise timing, the risetime of the fb signal (Fig. 3) and the QUENCH delay must be optimized. This is done by unbalancing all the inverters of the QC to optimize their threshold voltage. Moreover, the QC topology uses an active quench and recharge design for the SPAD.

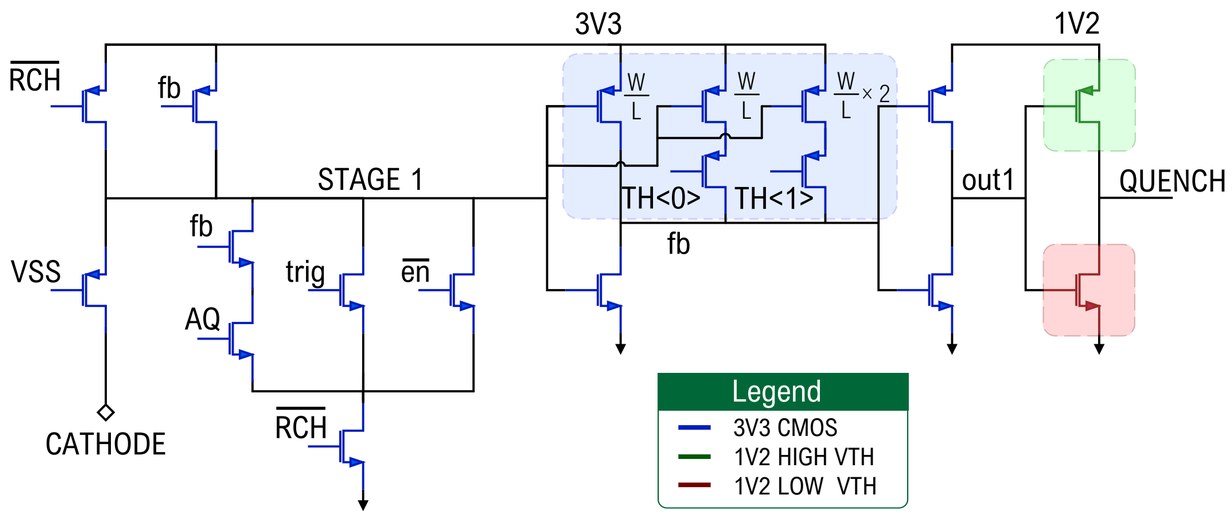


Fig 4: Schematic transistor level design of the quenching circuit. Highlighted in blue is the configurable PMOS topology

Conclusions

The characterization of the new ASIC prototype in TSMC 65 nm will lead to the optimization and development of the future high timing precision PDC, with timing resolutions below 10 ps RMS.

The 65 nm PDC will be connected to the same 64 × 64 SPAD array as the PDC in 180 nm technology.

The prototype test campaigns will include:

▶ Validating the threshold voltage configurability
▶ Measuring the timing jitter of the QC through dedicated test structures
▶ Testing the new TDC design

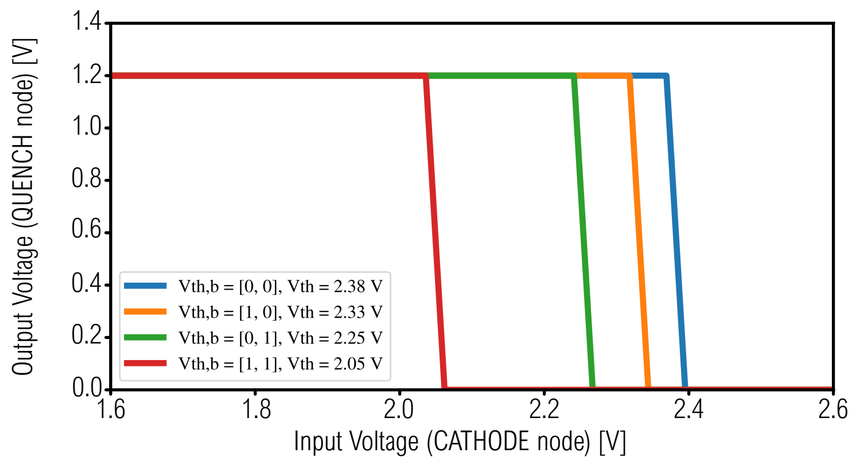


Fig 5: Simulated comparator threshold voltage configurability

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