First results on the final readout chip for the High-Luminosity LHC upgrade of the CMS Inner Tracker

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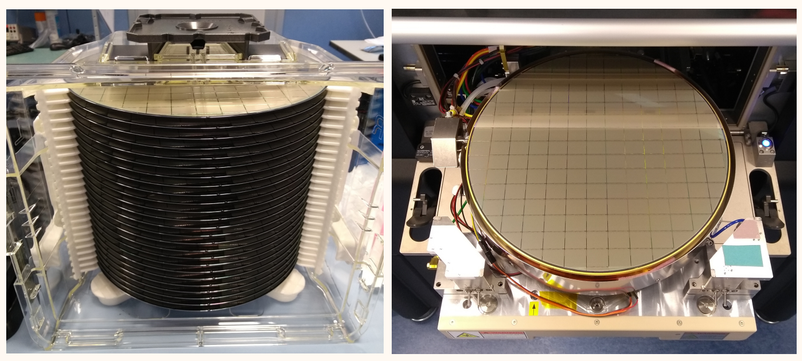
The CMS Readout Chip (CROC)

- **CMS Inner Tracker** for **High-Luminosity LHC** (HL-LHC): pixel detector instrumented with 10^4 **CMS Readout Chips (CROCs)**
- **CROC characteristics**:
  - **65 nm technology readout chip**
  - Developed by the joint ATLAS-CMS RD53 collaboration
  - 432×336 pixel cells in approximately 4 cm^2
  - Very complex digital architecture for high energy physics
  - **Serial powering** for detector modules
- **Prototype chip (CROCv1) produced in 2021**
- **Production chip (CROCv2) received in 01/2024**
  - Engineering run with 20 wafers (4 on hold at foundry)
  - **First tests performed at wafer level**

Logos on a CROCv2 chip

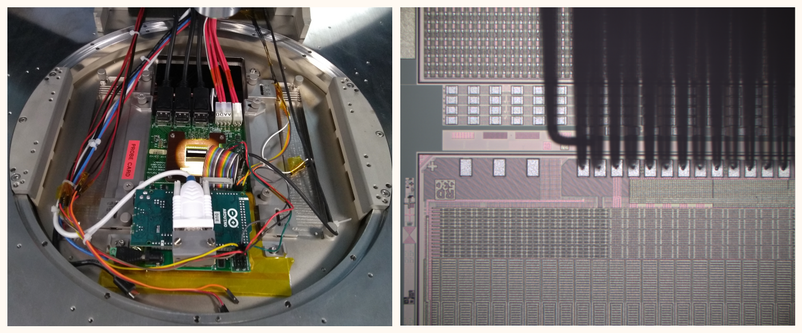
CROC waferprobing setup

- **Waferprobing facility**: clean room of the INFN-TO Technological Laboratory
- **14 CROCv2 engineering run wafers tested**
  - $\varnothing = 300$ mm; 136 chips / wafer



CROCv2 wafers in foundry box and on probe station

- **Automated wafer testing**: 21.5 h for each wafer
- **Wafer-level testing hardware**
  - Probe station: Cascade Microtech CM300xi (semi-automated)
  - Probe card: 194 tungsten needles to contact aluminium pads
  - Waferprobing auxiliary card: probe card control from PC
  - DAQ: FC7 board (Kintex 7 FPGA)
  - Remotely controllable instruments



Waferprobing hardware and chip under test

- **Wafer-level testing software**
  - WLT software (Python): `croc_wlt`
  - DAQ software (C++): `Ph2_ACF`
- **Chip testing procedures**
  - Power consumption and chip signals
  - Chip trimming (main reference current and core voltages)
  - Communication testing
  - Global and pixel registers
  - Chip calibrations (ADC, DACs, ring oscillators and *T* sensors)
  - Scan chain
  - Shunt-LDO *IV*
  - Pixel array testing (occupancy and S-curves)

Results from the CROCv2 engineering run

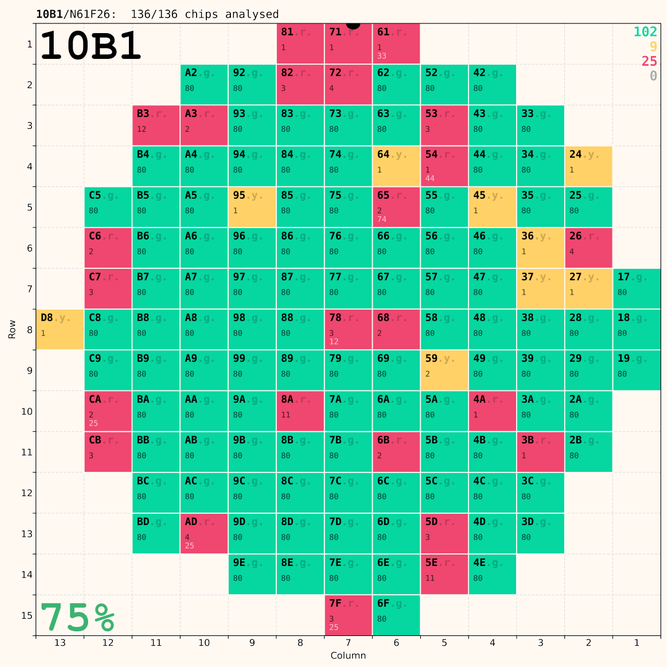
Composite picture of CROCv2 ASIC

- **CROCv2 ASIC verified at wafer level**
  - Most functionalities tested
  - Quickly verified several **design improvements** (CROCv1 $\rightarrow$ CROCv2)
  - Confirmed few known limitations not expected to affect detector operation

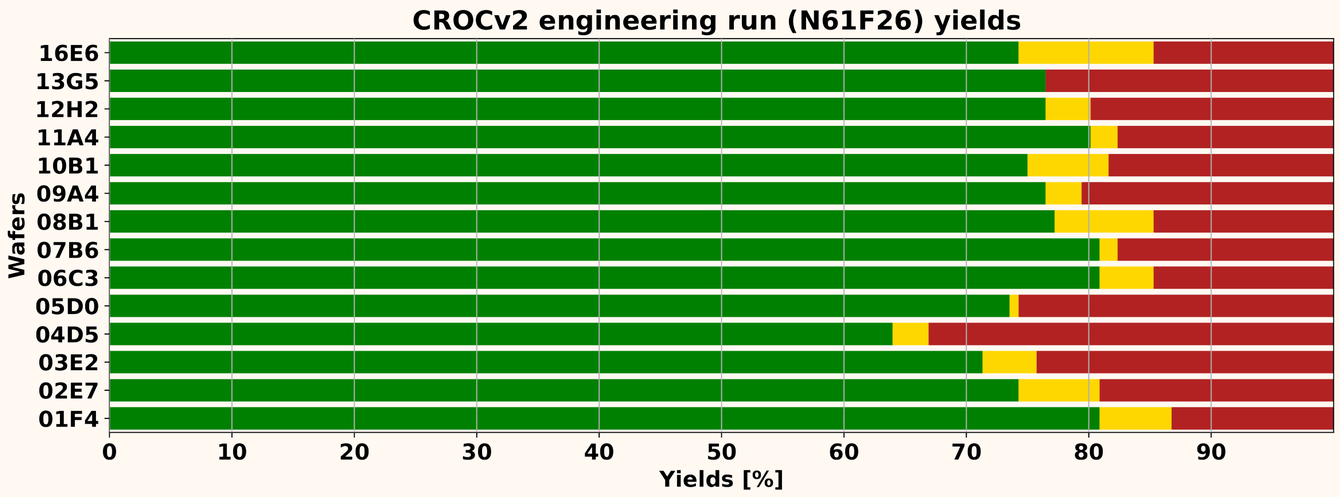
➔ **CROCv2 chip functioning as expected**

- Collected **characterisation data** for approximately 1900 chips
  - Startup current: 0.69 A (ana) + 0.40 A (dig)
  - Pixel current: 5.1 µA (ana) + 2.9 µA (dig)
  - Threshold σ after tuning (2700 e): ~ 40 e
  - Mean noise: ~ 70 e

- **Average yield for CROCv2 wafers**: **77 %**
  - **104 green chips per wafer on average**
  - **Higher yield than CROCv1 (75 %)**
  - **Green chips**: on detector ✔
  - **Yellow chips**: marginal !
  - **Red chips**: defective ✗
- **Failure rates of waferprobing tests**
  - **Results match CROCv1 data overall**
  - Defects mostly in **pixel array**
  - Digital signal injections: 11 % failure rate
  - Pixel registers: 5 % failure rate
- **Higher die failure rate near wafer edge**
  - Can be up to ~ 80 %



Example of CROCv2 wafermap



Chip yields for CROCv2 engineering run

Discussion

- Verified and characterised first CROCv2 wafers from engineering run
- **CROCv2 chip functioning as expected**
- **Higher chip yields from waferprobing** with respect to CROCv1, even with more tests
- Produced first single-chip testing boards and digital detector modules (i.e. without sensors)
- First CROCv2 production batch received in **May 2024**: **currently under test!**

Acknowledgements

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References

- *The Phase-2 Upgrade of the CMS Tracker* - CMS Collaboration (2017). Link: **cds.cern.ch/record/2272264**
- Chip reference manuals. Link: **cds.cern.ch/record/2890222**
- Wafer-level testing software repository. Link: **gitlab.cern.ch/croc_testing/croc_wlt**