Analog Front-End for the Readout of LGAD Based Particle Detectors

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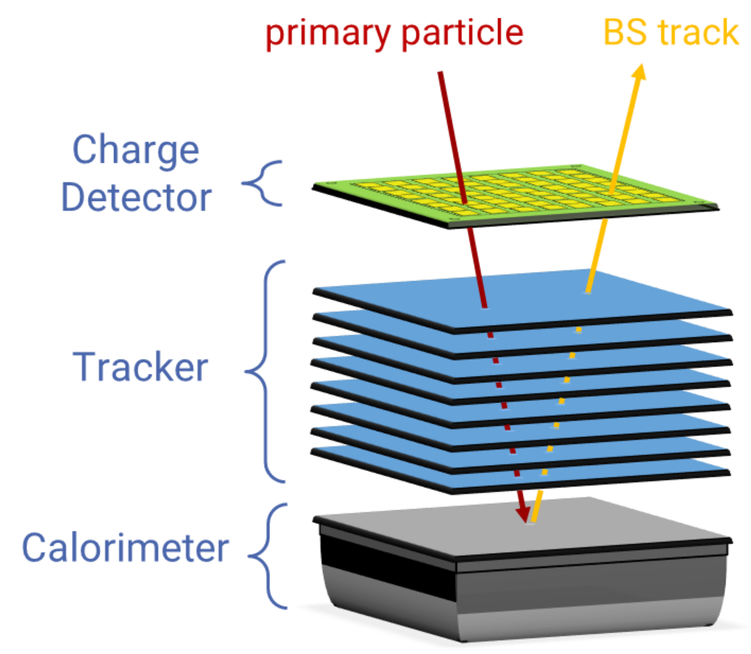
Abstract

An analog front-end circuit for the readout of LGAD based particle detectors has been designed. The front-end has to work over a range of **input charge larger than three decades** (from tens of fC to a few pC), achieving a time resolution better than 100 – 150 ps as required by the **ADA-5D project**, for which the front-end circuit has been designed.

The front-end circuit consists of a **Charge Sensitive Amplifier** (CSA) implementing a dynamic signal compression feature to achieve improved noise performance, along with enhanced time resolution capabilities over the wide range of input charge to be detected [2]. The CSA is then followed by an **RC-CR shaper**, a **fast comparator** and a **Time-to-Amplitude Converter** (TAC) [3].

Post-layout simulation results are in agreement with project specifications.

ADA-5D Project



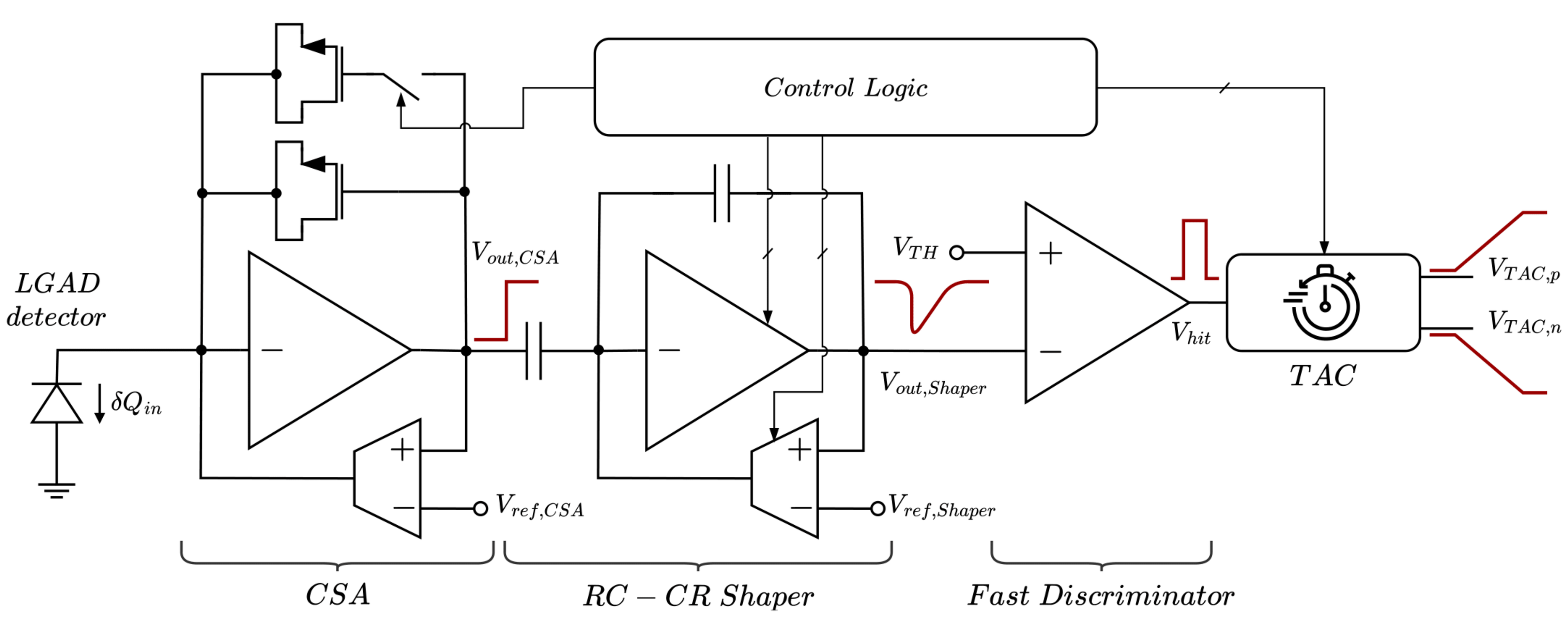
In space experiments, **charge identification** of individual cosmic-ray elements with energies larger than hundreds of GeV is seriously limited by the backscattered radiation (BS) from the calorimeter [1].

BS **degrades** the **charge resolution** every time it falls onto the detector traversed by the incident cosmic ray. This issue can be solved by **exploiting the difference in the arrival time** between the incident particle and the backscattered radiation hitting the detector.

With a flight time of around 700 ps between the detector and the calorimeter, in order to efficiently reject BS to better than five sigma, front-end circuits for particle detectors should provide a time resolution better than 100–150 ps.

This is the target of the **ADA-5D project** (funded by INFN), aiming at the development of an innovative **5D particle detector** for the simultaneous measurement of the incident particle position (for tracking purposes), charge (for nucleus identification) and timing (for false signal rejection).

Analog Front-End



Charge Sensitive Amplifier

- Dynamic signal compression feature
- Trilinear charge-to-voltage transcharacteristic: high-gain for $Q_{in} \in$ [38 fC — 1 pC], mid-gain for $Q_{in} \in$ [1 pC — 4 pC] and low-gain for $Q_{in} \in$ [4 pC — 16 pC]
- Equivalent feedback capacitance: [1.2 pF — 53 pF]
- Output dynamic range: 0.8 V / Recovery time: 10 µs
- Input dynamic range: [38 fC — 8 pC] / [38 fC — 16 pC] (selectable)
- $V_{ref,CSA}$ = 0.2 V

Semi-Gaussian Shaper

- First order RC-CR shaper. $V_{ref,Shaper}$ = 1.1 V
- Selectable shaping time: 10 ns, 15 ns, 25 ns, 45 ns

Fast Discriminator

- 4.2 V/ns positive slew-rate
- Jitter at discriminator output: 100 ps

Time-to-Amplitude Converter (TAC)

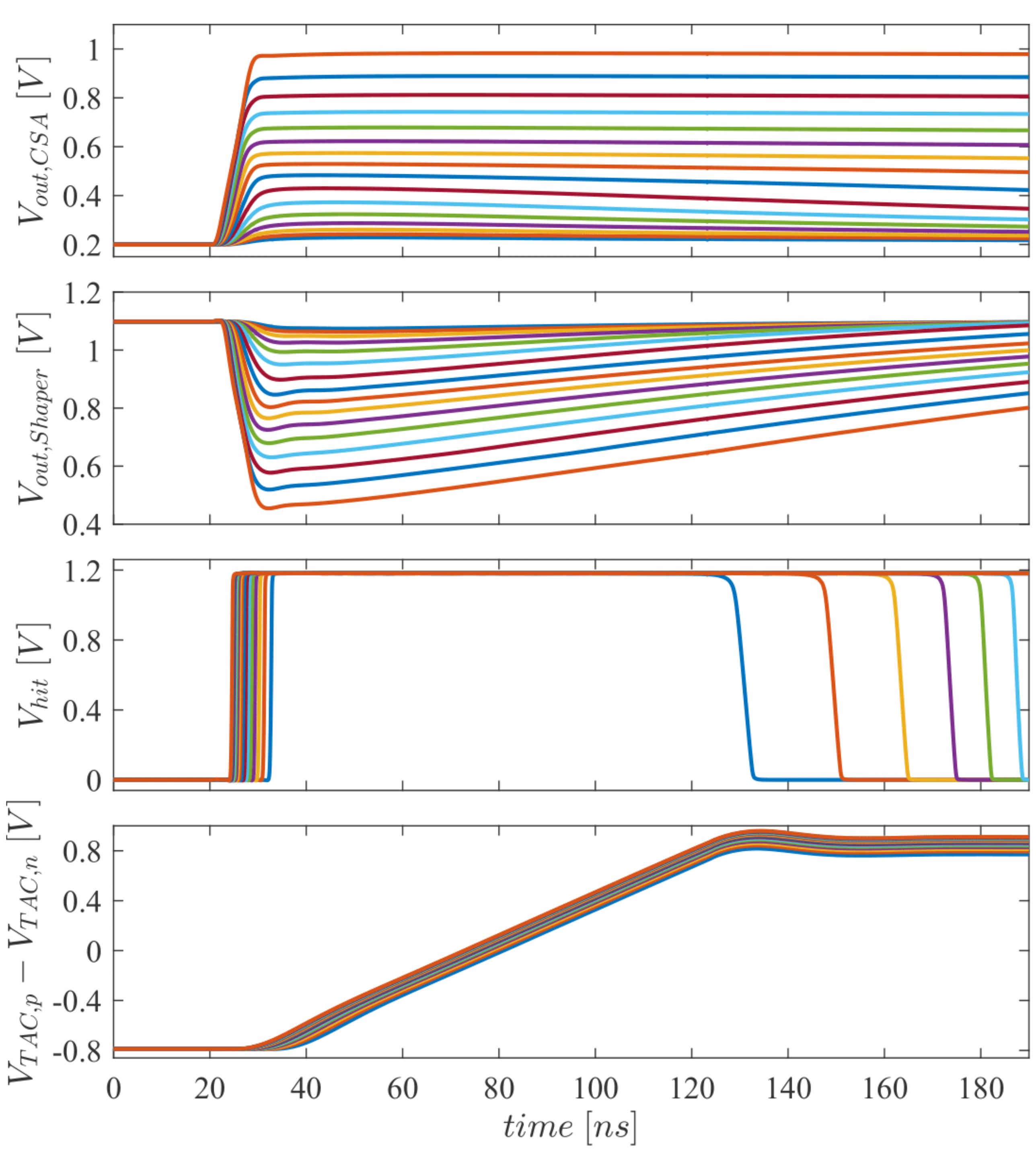
- Two selectable full-scale ranges (FSRs): 100 ns / 1 µs
- TAC differential output dynamic range = 1.6 V

Control Logic

- Slow control network for the configuration of the front-end blocks.

The front-end circuit has been designed in a 65 nm CMOS technology.

Post-Layout Simulation Results



Post-layout transient response of the analog front-end channel to an input charge varying from 38 fC to 16 pC, with 6 steps per decade (the ratio between two consecutive steps is $\sqrt[6]{10}$). The horizontal scale is the same for all graphs.

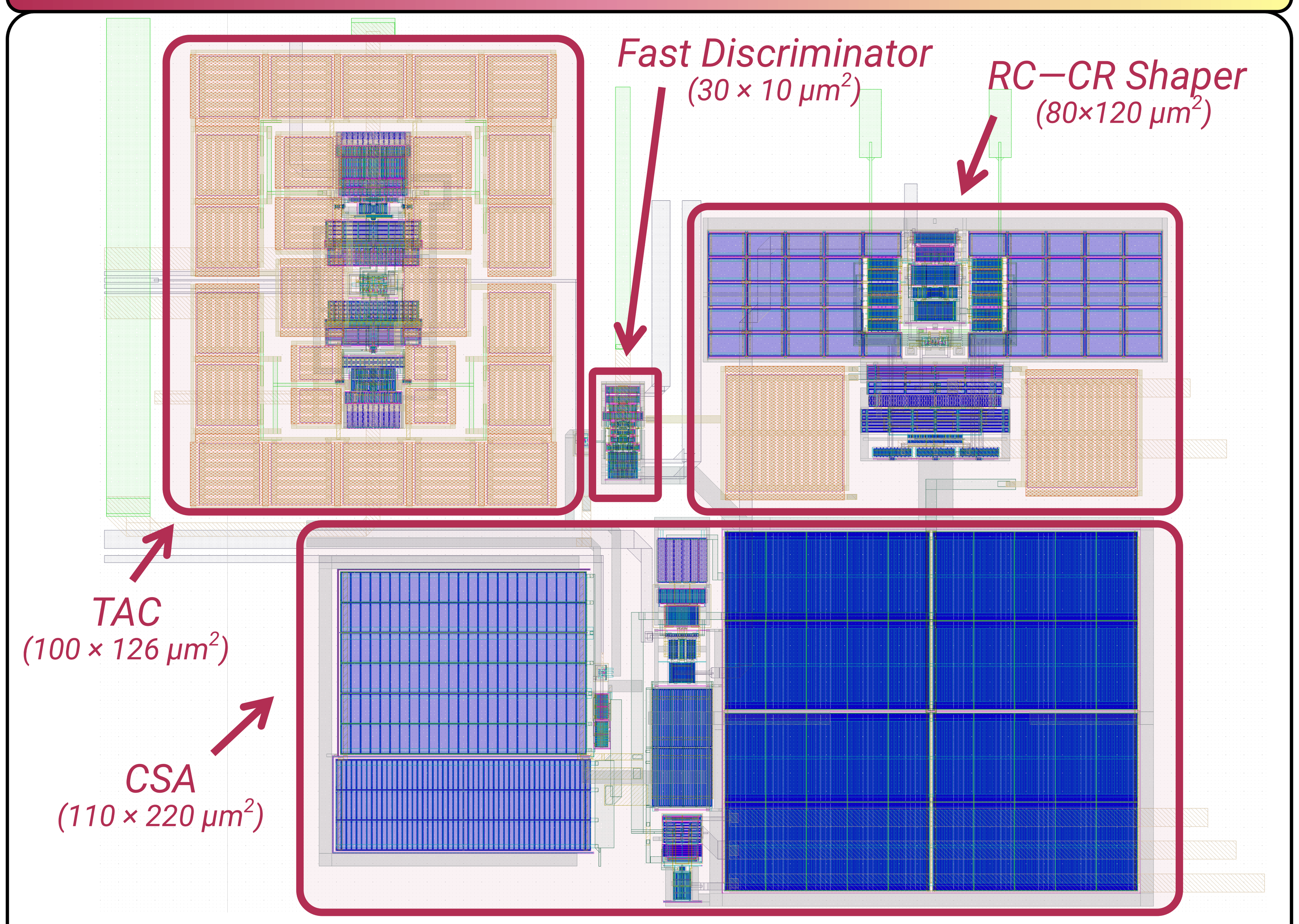
Simulation results are given for the CSA working over the maximum charge input range and for a shaping time of 10 ns

Q_{in}	CSA Charge Sensitivity
[38 fC — 1 pC]	833 mV/pC
[1 pC — 4 pC]	52 mV/pC
[4 pC — 16 pC]	19 mV/pC

RC-CR Shaping Time	ENC / SNR
10 ns	147 aC / 306
15 ns	146 aC / 307
25 ns	134 aC / 333
45 ns	136 aC / 330

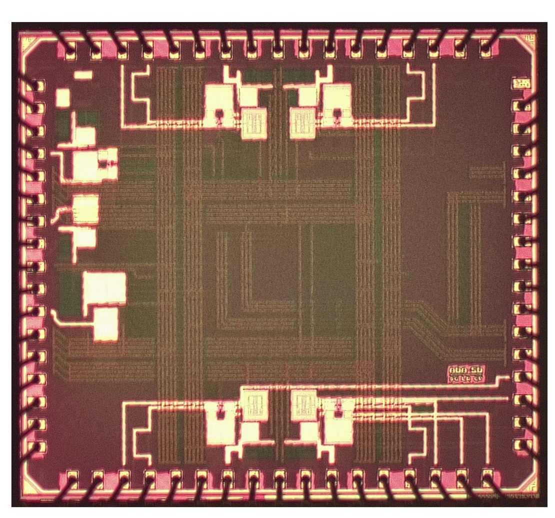
Time-to-Amplitude Converter (TAC)	
Jitter (FSR = 100 ns)	≤ 55 ps
Jitter (FSR = 1 µs)	≤ 180 ps
|INL| (FSR = 100 ns)	≤ 0.44 ‰
|INL| (FSR = 1 µs)	≤ 0.067 ‰

Front-End Layout



The complete front-end channel features an overall area of 240 x 270 µm² (TAC and RC-CR Shaper MIM capacitances included) and a total power consumption lower than 2 mW.

Conclusion



Test Chip

- The front-end circuit designed is capable of working over a range of input charge larger than threee decades (from 38 fC to 16 pC)
- CSA implementing a dynamic signal compression feature allows to achieve improved noise performance along with enhanced time resolution capabilities over the wide range of input charge to be detected
- Measurements are currently in progress on the test chip. It includes four complete front-end channels and additional structures for characterization purposes

References

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[3] S. Giroletti, L. Ratti and C. Vacchi, "Pseudo-Differential Time-to-Amplitude Converter for LGAD Based Particle Detectors," 2024 IEEE Int. Symp. Circuit Syst. (ISCAS) , Singapore, May 2024. Waiting for pubblication.