Characterization results of MAPS digital prototypes for the ALICE ITS3

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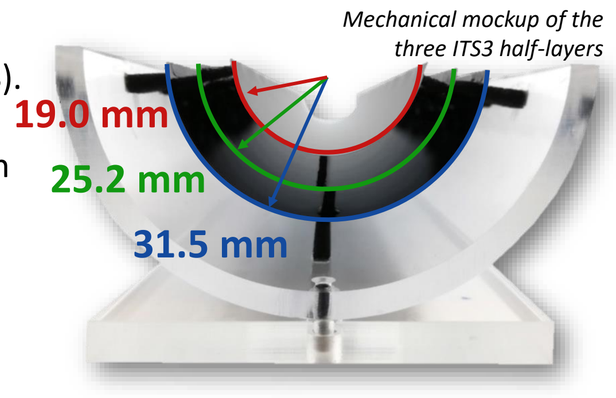
The ALICE Inner Tracking System for LHC Run 4

- A new Inner Tracking System **ITS3** [1] will replace the innermost layers of the ALICE ITS2 during LHC Long Shutdown 3 (2026-2028).
- **Tracking efficiency** and **pointing resolution** will be further improved by this upgrade, thus allowing to increase the precision of **measurements in the heavy-flavour sector** and to bring **another set of fundamental observables** into reach [2], e.g.:
  - $\mathbf{B_s^0}$ and $\mathbf{\Lambda_b^0}$ at low transverse momenta
  - **Non-prompt $\mathbf{D_s^+}$ and $\mathbf{\Xi_c^+}$** decays in heavy-ion collisions



Mechanical mockup of the three ITS3 half-layers

Detector layout:
- 3 truly cylindrical **self-supporting** layers
- Each half-layer made by 1 **flexible MAPS** sensor which:
  - has a **large-area** O(10×26 cm^2)
  - is **ultra-thin** (≤50 µm)
- Ultra-light **carbon foam support structures** keep in position the sensors
- **Innermost layer at 19 mm** from the interaction point
- Unprecedentedly **low material budget** of 0.09% X_0/layer
- Air cooling system

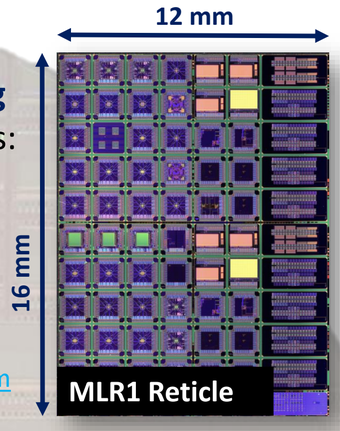
- Talk by L. Aglietta

1. ITS3 MAPS prototypes

The Tower Partners Semiconductor Co. [3] **65 nm CMOS imaging process** for MAPS was chosen for the ALICE ITS3. Key advantages:
- High **radiation hardness**
- Low **power consumption**
- **5 µm** 2D spatial resolution
- **Large wafers** (Ø 300 mm)

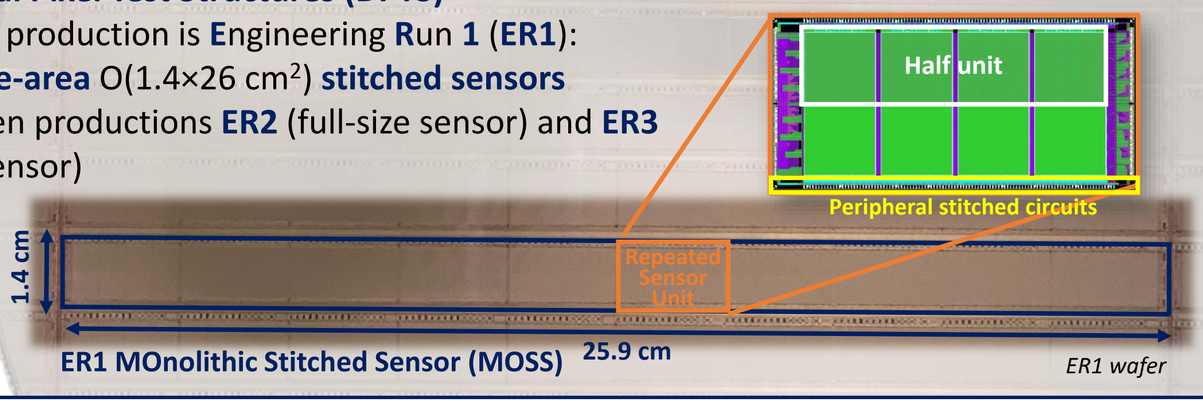
First production is **M**ultiple **L**ayer **R**eticle **1** (**MLR1**):
- Transistor test structures → radiation hardness studies
- Diode matrices → charge collection studies
- Analog building blocks
- **Digital Pixel Test Structures (DPTS)**

- Poster by K. Gautam



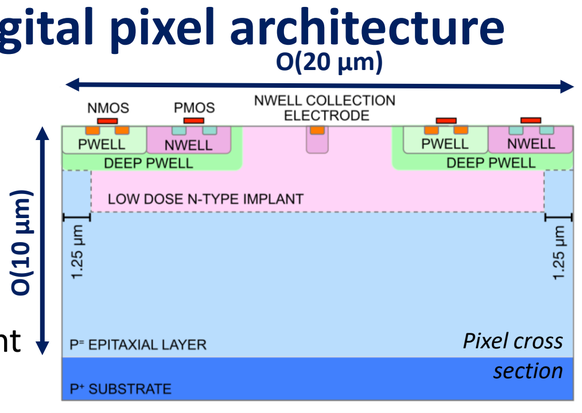
Second production is **E**ngineering **R**un **1** (**ER1**):
- **Large-area** O(1.4×26 cm^2) **stitched sensors**

Foreseen productions **ER2** (full-size sensor) and **ER3** (final sensor)



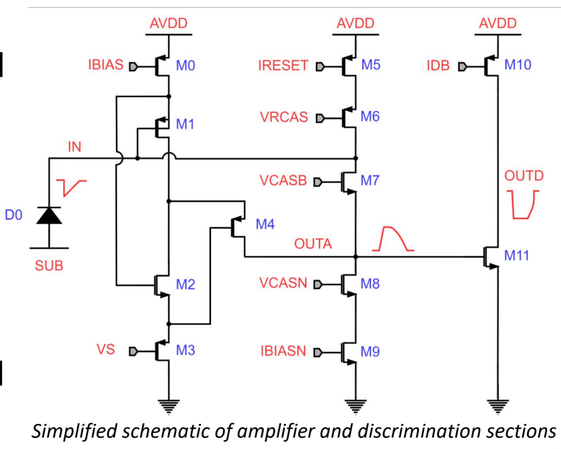
2. MLR1 and ER1 digital pixel architecture

- **50 µm thick** sensor
- Variable pixel pitch **O(20 µm)**
- Additional low dose n-type implant allows to deplete the epitaxial layer over the full width:
  - → Faster and more efficient charge collection
  - → Less charge sharing



The pixel architecture has evolved from ITS2 ALPIDE sensor [4].
Each pixel hosts:
- Sensing diode
- Front-end amplifier
- Discriminator
- Digital pixel section

Similar architecture will be ported to the final sensor design.

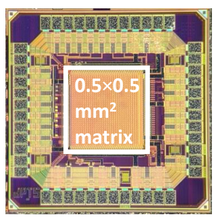


Simplified schematic of amplifier and discrimination sections

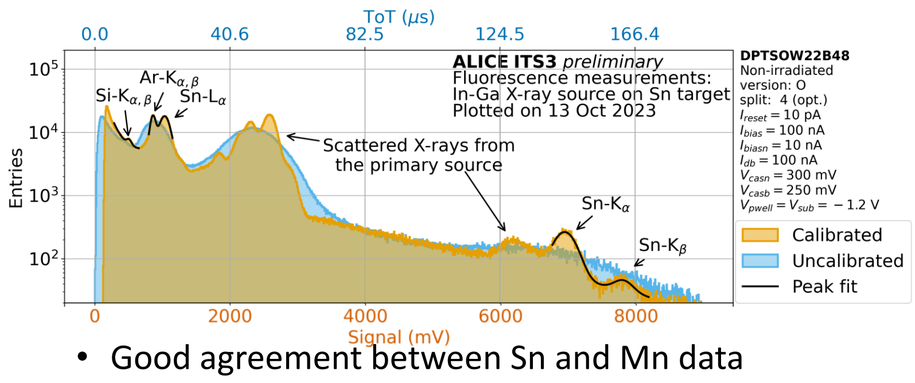
3. Energy loss measurements with DPTS

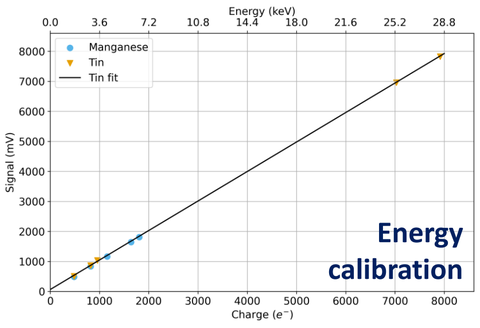
The DPTS is a 1.5×1.5 mm^2 MLR1 chip:
- 32×32 pixel matrix, **15 µm pitch**
- **Time-over-threshold** (ToT) measurements

The linearity of the front-end from 1.7 to 28.5 keV was evaluated with **fluorescence X-ray measurements**. A Mn foil and a Sn foil were used as targets.



DPTS Goal: study the in-pixel front-end





- Good agreement between Sn and Mn data
- Demonstrated **linearity** of the response **up to 28.5 keV**

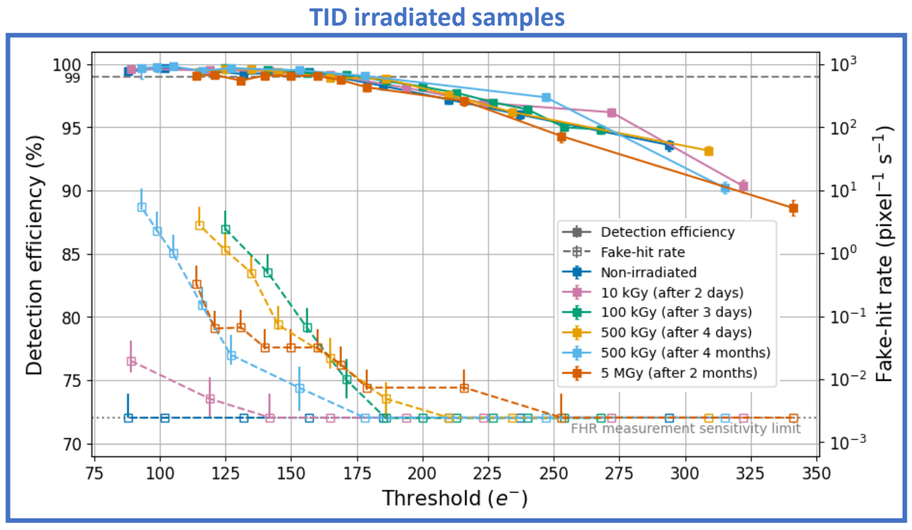
4. DPTS in-beam measurements

Measurements to assess [5]:
- Detection efficiency and spatial resolution

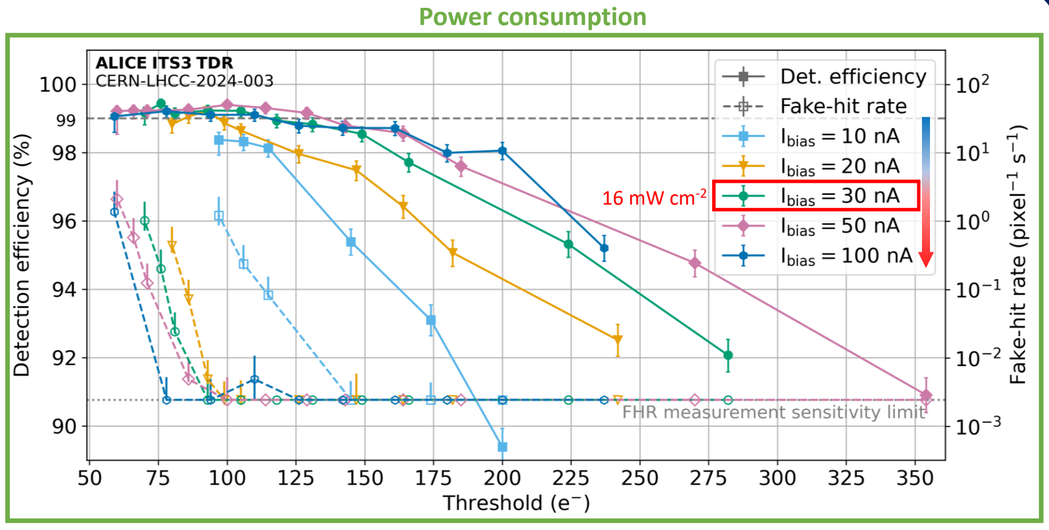
➢ **Irradiated samples** show excellent detection efficiency (99%)

➢ **DPTS power consumption** can be lowered to 16 mW cm^{-2}

TID irradiated samples



Power consumption

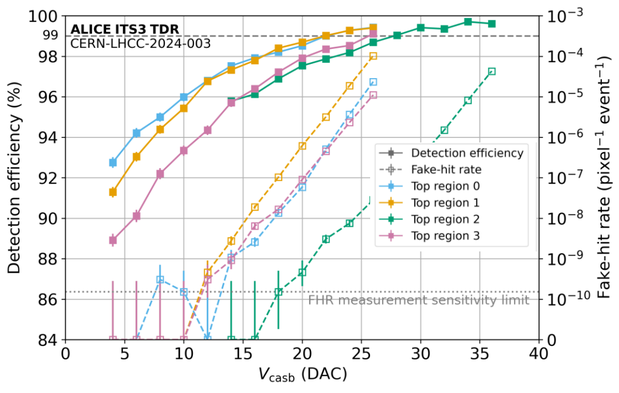


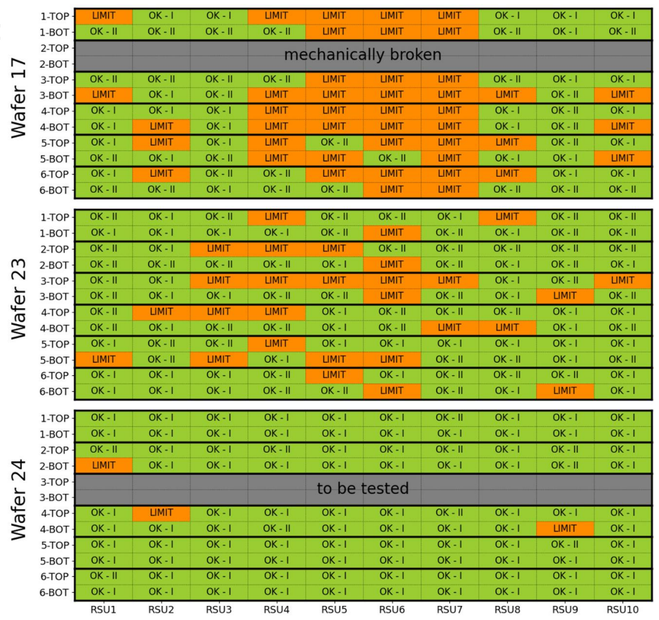
5. Large-area stitched sensor characterization

Extensive mass testing (120 chips from 20 wafers) to evaluate:
- Performance
- Production yield

First steps:
1. Measurements of power net impedances
2. Power ramp of the supplies

Detection efficiency and spatial resolution expected from MLR1 chips are confirmed.





Conclusions and outlook

➢ ITS3 will be installed during LS3 to be ready for LHC Run 4 (2029-2032)

➢ First large-area stitched sensor produced

➢ Demonstrated bent MAPS operability [6], not shown

➢ Sensor qualification is on track:
- Validated 65 nm CMOS process with MLR1 prototypes
- Stitching qualification is ongoing

References

[1] ALICE Collaboration, Letter of Intent for an ALICE ITS Upgrade in LS3, 10.17181/CERN-LHCC-2019-018
[2] Shreyasi Acharya et al., Upgrade of the ALICE Inner Tracking System during LS3: study of physics performance, http://cds.cern.ch/record/2868015
[3] Tower Semiconductor home page, https://towersemi.com/
[4] M. Šuljić, ALPIDE: the Monolithic Active Pixel Sensor for the ALICE ITS upgrade, https://iopscience.iop.org/article/10.1088/1748-0221/11/11/C11025
[5] G. Aglieri Rinella, et al., Digital pixel test structures implemented in a 65 nm CMOS process, https://doi.org/10.1016/j.nima.2023.168589
[6] ALICE ITS3 project, First demonstration of in-beam performance of bent Monolithic Active Pixel Sensors, https://doi.org/10.1016/j.nima.2021.166280