

# A 4D-Tracker Demonstrator based on the Timespot1, a CMOS 28-nm ASIC

Friday, 31 May 2024 08:55 (1 minute)

High luminosity upgrades to particle colliders imposes challenges to vertex detectors in terms of both radiation damage and event pile-up. For future tracking detectors, such as LHCb Upgrade II VERTex LOcator (VELO) detector, requirements are: a  $<50$  ps timing resolution; spatial resolution on the order of 10  $\mu\text{m}$ ; and radiation hardness up to  $6 \times 10^{16} \text{ neq cm}^{-2}$ . The TimeSPOT collaboration has already tested and proven that 3D silicon trench sensors are a potential candidate for such detectors, but the development of fast-timing front-end electronics remains an ongoing challenge.

To overcome these obstacles, 28 nm CMOS technology has been introduced to high energy physics to develop new fast-timing front-end electronics for sensors. The Timespot1 ASIC was developed with such technology and aimed to bridge the gap between currently available front-end ASICs and those required for high-luminosity collider applications. Each ASIC contained 1024 channels in a  $32 \times 32$  matrix, with each channel containing its own analog front-end and TDC. We present a collection of results on the Timespot1 hybrid: self-tests of the ASIC; a test beam at CERN SPS on a 5-layer demonstrator of Timespot1 hybrids; and a TCT scan of a 3D silicon trench sensor that has been bump-bonded to the Timespot1 ASIC. By combining results from these tests, it is possible to give a detailed characterization of pixel operation (ASIC and 3D-trench silicon sensor). The results will be presented in the present paper. Such results from the Timespot1 ASIC are highly valuable and will be used by the IGNITE collaboration in the development of new fast-timing ASICs.

## Collaboration

## Role of Submitter

I am the presenter

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**Session Classification:** Electronics and On-Detector Processing - Poster session

**Track Classification:** T7 - Electronics and On-Detector Processing