A 4D-Tracker Demonstrator Based on Timespot1: A CMOS 28-nm ASIC

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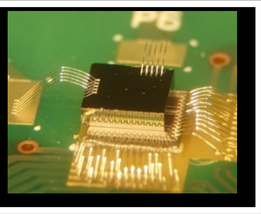
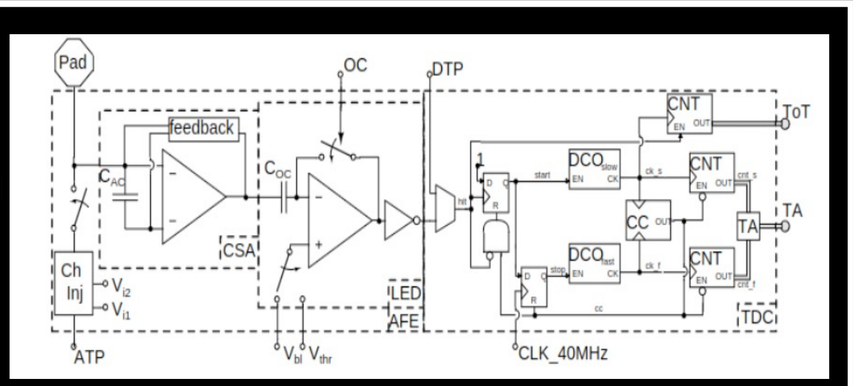
Introduction and Context

The Timespot1 ASIC was developed using 28 nm CMOS technology within the TimeSPOT/IGNITE collaborations and aimed to bridge the gap between available fast-timing ASICs and those required for high-luminosity applications. Presented in this poster are a collection of a results of the Timespot1 hybrid: self-tests of the ASIC; a CERN SPS test beam on a 5-layer demonstrator of Timespot1 hybrids; and a TCT scan of 3D trench electrode silicon sensors that have been bump-bonded to the Timespot1 ASIC.

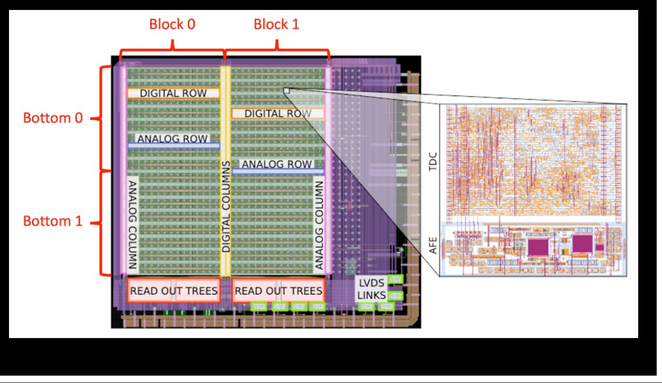


Channel Architecture

Each channel is comprised of an analog front-end (AFE) and a TDC. Each AFE has two stages: a charge-sensitive amplifier and a leading-edge discriminator. Each channel contained a charge-injection circuit for self-testing purposes.



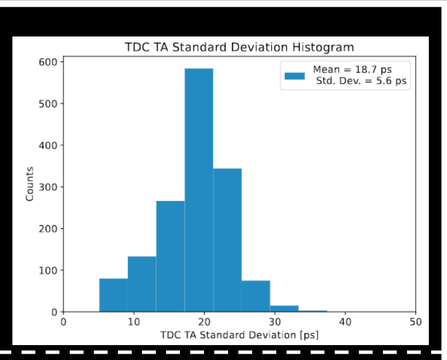
Channels were arranged in a 32x32 matrix and divided into four groups for read-out. 4 DACs controlled the chip threshold, baseline and the amount of charge injected for self-tests. It was also possible to control the power supply to the analog. Chip configuration and read-out from self-tests was performed via a slow I²C interface.



Electrical Self-Tests Summary

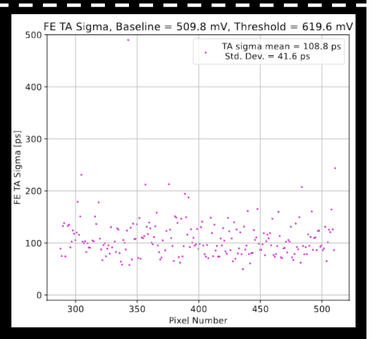
The TDC timing performance was determined by pulsing each TDC at 7 equally-spaced phases across its dynamic range. At each test point, the TDC was pulsed 50 times.

Mean TDC ToA Resolution: **18.7 ps**



The charge injection circuit of each channel was used to pulse each analog front-end with a charge equivalent to 1 MIP. Each channel was pulsed 50 times.

Mean AFE ToA Resolution: **108.8 ps**
AFE ToA Resolution Std.Dev.: **41.6 ps**

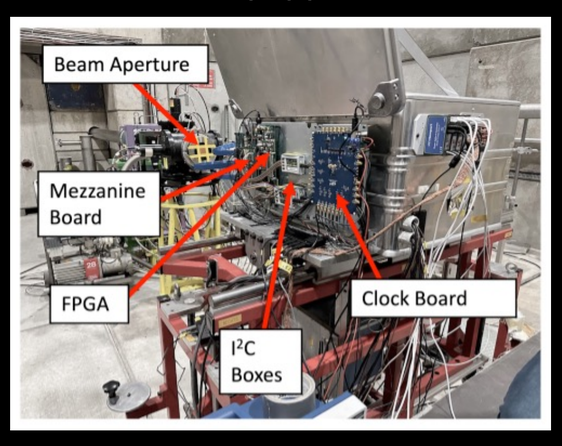


Dispersion is due to a known bug in the offset compensation (see https://doi.org/10.1088/1748-0221/17/03/C03022).

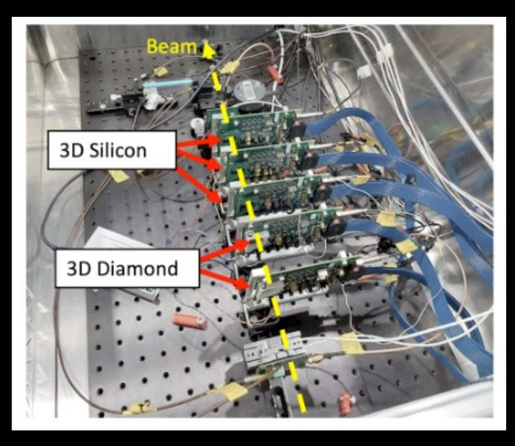
Test Beam at CERN SPS H8

A 5-layer demonstrator was set up and tested with a positively-charged 180 GeV/c pion beam at CERN SPS. Each layer had a sensitive area of ~0.25 mm². Three of the Timespot1 hybrids were equipped with **3D trench electrode silicon sensors**, whilst the other two were equipped with **3D columnar electrode diamond sensors**.

External Set-Up

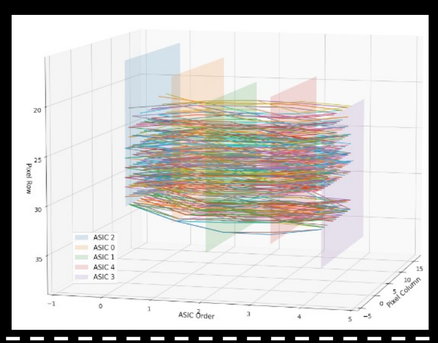


Telescope Set-Up

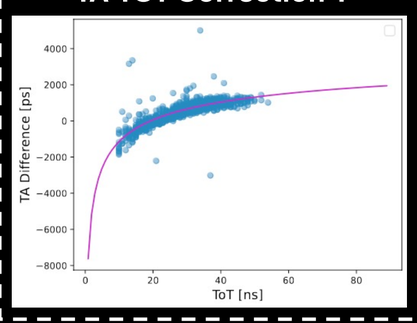


Output was performed using a KC705 Xilinx board. Tracks were found between the 5 layers, and the timing performance for individual pixels was determined.

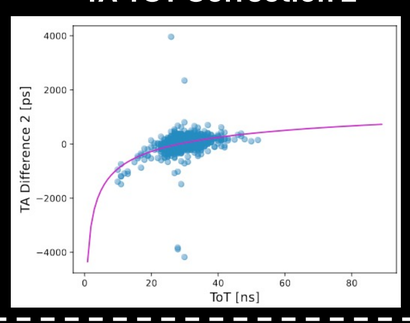
A two-stage TA-ToT correction was required for the timing performance between any two pixels.



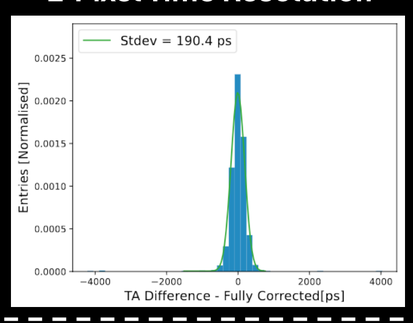
TA-TOT Correction 1



TA-TOT Correction 2



2-Pixel Time Resolution



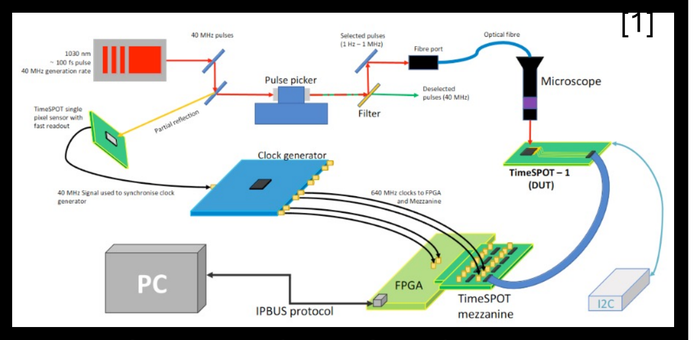
Best performing pixels (electronics + sensor): **Diamond: σ_{total} = 94.7 ps**
Silicon: σ_{total} = 237.1 ps

Why the difference in performance?

3D silicon trench sensors exhibited very high leakage current, meaning that the effective reverse bias was around -1 V. This was a consequence of an unsatisfactory bonding procedure. A properly biased 3D silicon trench sensor has an excellent timing performance of **~10 ps** (see https://doi.org/10.3389/fphy.2023.1117575). A laser scan was performed to assess the impact of this high leakage.

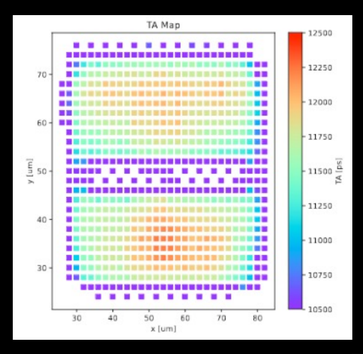
Laser Scan of Timespot1

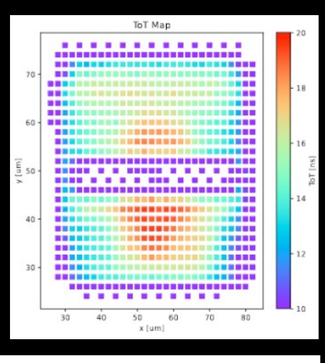
A Transient Current Technique was adopted to assess the non-uniformity of the weighting field in the Timespot1 hybrids equipped with 3D trench electrode silicon sensors.



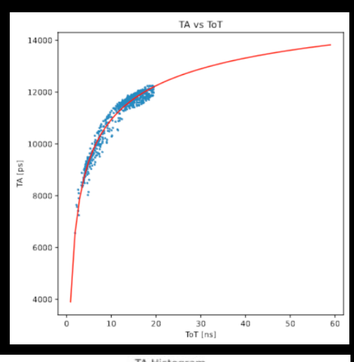
The Timespot1 hybrid was mounted on two piezo electric stages to allow *x*-*y* movement. A scan was performed over a 110 µm x 110 µm area with a 2 µm increment in both *x* and *y*. This was centred on a single pixel, and 600 events were recorded for each position. Energy was deposited equivalent to 1 MIP in each event. The Timespot1 hybrid was synchronised with the laser input to give the ToA measurements a reference. Read out was done via a KC705 Xilinx board.

Maps of both TA and ToT were produced, where each position gives the average TA and ToT over the 600 events recorded.



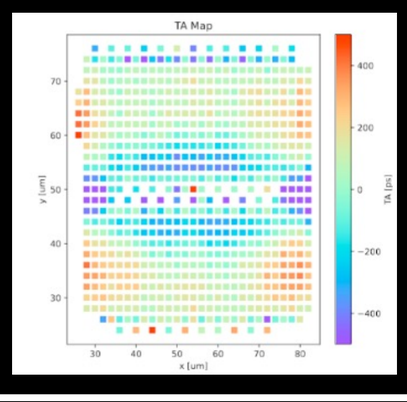


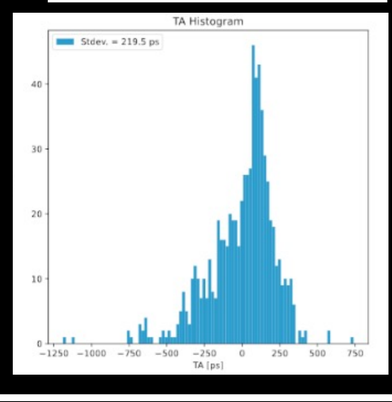
As was the case for the test beam analysis, a TA-ToT correction was required. This only required one stage as the reference for each ToA measurement was provided by the laser input. Following this, a new ToA map of the pixel was produced, with its associated ToA histogram.



For the measured pixel, the jitter due to the non-uniformity of the weighting field:

σ_w = 219.5 ps





Conclusions

σ_w = 219.5 ps and σ_w ≈ 80.0 ps [2] for the silicon and diamond sensors, respectively. Combining the results from the test beam and the laser scan, the timing resolution of individual channels of the Timespot1 ASIC have been shown to attain a performance below 100 ps. Although the performance of single channels show promise, there are non-uniformities in ASIC performance that require work for the next ASIC prototype. Under the umbrella of the IGNITE collaboration, ASIC development will continue with the aim of developing a full matrix with a timing performance below 50 ps whilst adhering to power consumption limits.

[1] A. Loi et al., *Test Results of the Timespot1 ASIC on 3D-Trench Sensors*, Trento Workshop, Feb. 2023. [2] L. Anderlini et al., *Recent results on 3D diamond pixel detectors for 4D-tracking*, FAST 2023.