

The FastRICH ASIC at the LHCb RICH enhancements

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Sub-100ps time information is a powerful tool to maintain the excellent particle ID performance of the LHCb RICH detectors during the high-multiplicity events at the HL-LHC Run 5. A cornerstone of the detector upgrade programme is the introduction of a novel opto-electronic readout chain with single-photon hit time information. The phased improvement, with new readout electronics during Long Shutdown 3 (LS3, 2026-2028), will be outlined. Central to the fast-timing readout electronics is a new ASIC called the FastRICH. This 65 nm CMOS ASIC is being designed by CERN and the University of Barcelona and the first chips will be available and tested by the end of 2024. The FastRICH packs a unique set of features targeting operation in HEP experiments and in particular the LHCb RICH detector: 25 ps time resolution, faster than 40 MHz operation, low power consumption in a 16-channel package, radiation hardness and a wide input signal dynamic range for coupling to multi-anode PMTs, SiPMs or MCP-based photon detectors. Special attention is paid to the reduction of data throughput in the ASIC, with constant-fraction discrimination, a configurable time gate to remove out-of-time hits at the front-end and a zero-suppressed output format. The direct interface with the CERN optical link chipset and the strategy for global detector calibration and operation in the time domain will be presented. An extensive test campaign at the SPS charged particle beam facility has been performed including the FastRICH predecessor, the FastIC ASIC, coupled to a TDC (time-to-digital converter) and the upgrade CERN optical link chipset. Overall, this contribution aims to introduce the future fast-timing components to the audience and outline how these will be integrated in a full detector design for the LHCb RICH at CERN.

Collaboration

LHCb RICH

Role of Submitter

I am the presenter

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