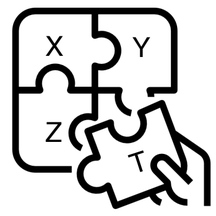
The FastRICH ASIC for the LHCb RICH enhancements



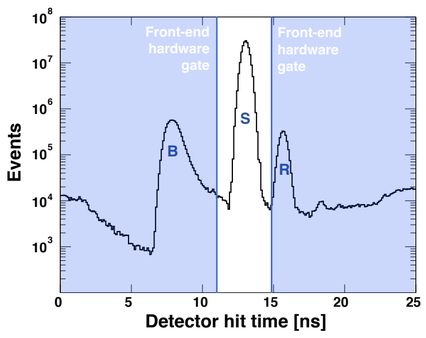
The Ring-Imaging Cherenkov (RICH) detectors at LHCb have an excellent intrinsic time resolution owing to the prompt Cherenkov radiation and focusing mirror optics. Novel RICH readout electronics, to be installed during the third Long Shutdown period (LS3), will introduce fast-timing information in the LHCb experiment. Central to the readout chain is a custom-developed ASIC, called the FastRICH, with a unique set of features targeting operation in HEP experiments and in particular the LHCb RICH detector. Here, an overview of its specifications and detector integration is given.

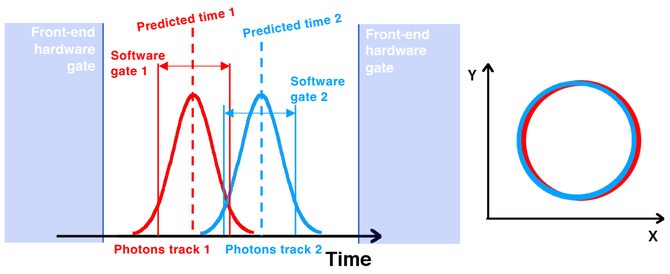
Floris Keizer (CERN) on behalf of the LHCb RICH Collaboration

1 The RICH detectors : fast timing by design

Studies demonstrated that for a given track the time-of-arrival of Cherenkov photons on the detector plane can be predicted to better than 10 ps [1]. This prediction in the RICH pattern recognition algorithms includes the LHCb tracking information, the reconstructed photon paths in the RICH and the Primary Vertex time. **Fast-timing information in the RICH detectors** is a powerful tool to mitigate pile-up and improve particle ID especially in the HL-LHC era.

Integrated over many simulated bunch-crossings, the detector hit times show a distinct signal peak (S) with one nanosecond width dominated by the Primary Vertex distribution. Similar to a camera shutter, a **hardware time gate** in the front-end electronics can be used at a fixed, configurable latency to the 40 MHz LHC clock. This reduces the hit detection window and eliminates out-of-time background (B, R) or noise from the photon sensor.

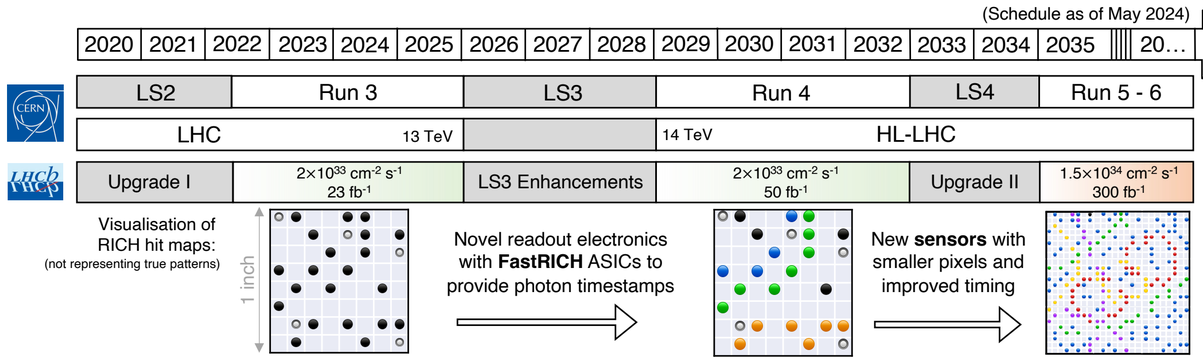




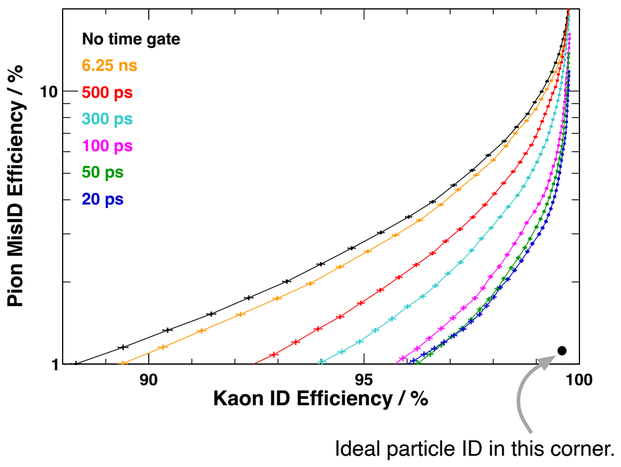
Within this time gate, a timestamp will be added for each detected hit. In the reconstruction algorithms, the hit times are compared against the predicted time-of-arrival. This novel '**software time gate**' reduces background from other particles and allows spatially overlapping events to be disentangled [2].

Simulation studies motivate that for **the single-photon detectors: faster = better**, up to the $\mathcal{O}$(10 ps) limit. A strategy was formed to first improve the readout electronics during LS3 enhancements followed by the photon sensor during LHCb Upgrade II [3].

Run 3	**Sensor** MAPMT	**FE ASIC** CLARO	**FPGA** Kintex 7	NDC	**Optical link** GBT Versatile Link	NDC	**Back-end** PCIe40	Sensor σ ~ 150 ps Electronics ~ 6000 ps
Run 4	**Sensor** MAPMT	**FastRICH**		DC	**Optical link** lpGBT / VL+	DC	**Back-end** PCIe40(0)	Sensor σ ~ 150 ps Electronics ~ 25 ps
Run 5	**Sensor** SiPM / MAPMT / MCP	**FastRICH**		DC	**Optical link** lpGBT / VL+	DC	**Back-end** PCIe400	Sensor σ ≤ 75 ps Electronics ~ 25 ps



2 LS3 Enhancements: performance



The **RICH particle ID** curves provide a standardised and sensitive probe of the RICH performance. The curves show the improvements as software time gates of smaller width are applied around the predicted hit time. During LS3, the detector enhancement will introduce fast-timing readout whilst maintaining the MAPMT sensors with σ~150 ps time resolution. For an optimal gate of $\pm 2\sigma_{\text{sensor}}$, this corresponds to a gate of about 600 ps. The **trend in particle ID performance motivates the pursuit of faster sensor technologies** (Upgrade II) to couple to the FastRICH readout.

3 Prototyping optoelectronic chain at the SPS testbeam

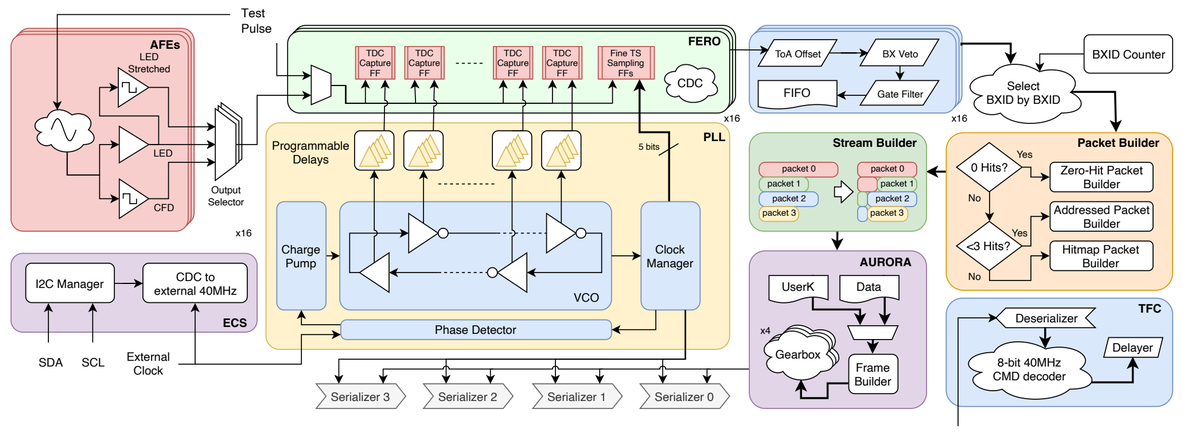
A prototype optoelectronic readout chain based on the **FastIC**, a predecessor of the FastRICH, was tested at the CERN SPS charged particle beam facility. The FastIC is connected to the **picoTDC**, which is used to timestamp the hits. The data are transmitted through an **lpGBT / VTRX+ optical link plugin** with a design close to the foreseen new modules. Nearly 500 channels across different photon sensors (MAPMT, SiPM and MCP-based) were read out during the testbeam.
The prototype is highly modular and designed to be compatible with a new FastRICH plugin to replace the FastIC + picoTDC combination for beam tests in 2025.

Conclusion

- During LS3, readout electronics with **25 ps** timing information will be introduced in the LHCb RICH.
- The new **FastRICH** ASIC will be coupled to MAPMTs (with 150 ps resolution) during Run 4.
- The FastRICH design allows **flexible coupling** to single photon sensors with **highly compressed** data.
- A **prototype chain** based on its FastIC predecessor has been extensively tested at the SPS facility.

4 The FastRICH ASIC

The FastRICH is an application-specific integrated circuit (ASIC) being designed in **65-nm CMOS technology by the CERN EP-ESE department and the University of Barcelona [4]** with strong input in the specifications from the LHCb RICH collaboration. The FastRICH is intended to meet the requirements for Run 4 (MAPMTs) as well as Run 5 and 6 with different types of photon sensor. The first FastRICH ASICs from a Multi-Project Wafer are foreseen at the end of 2024.



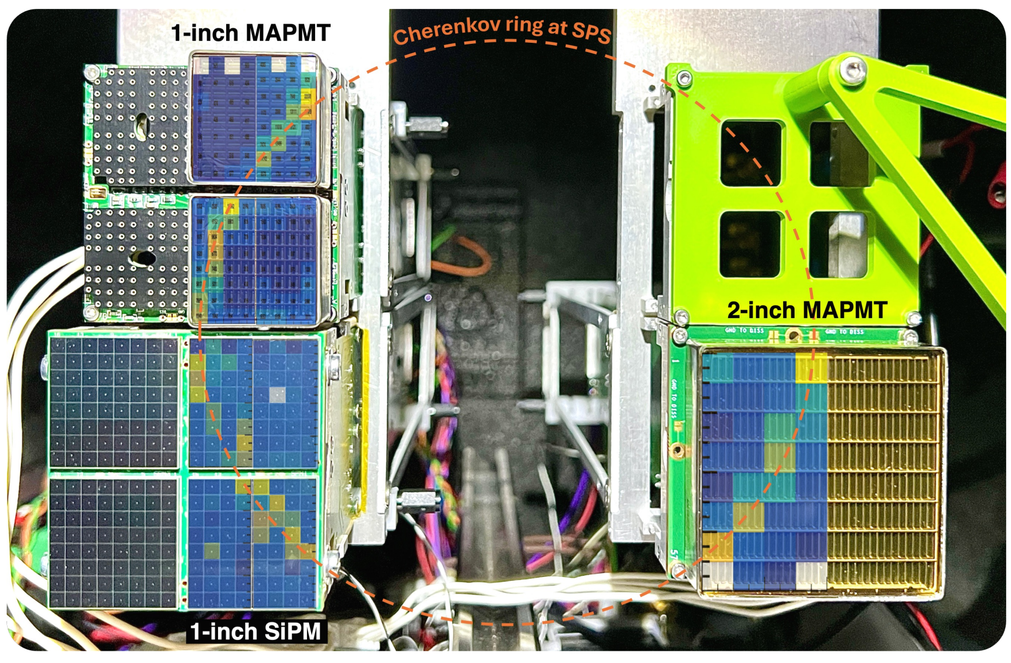
- **16-channel** design in QFN88 package of 10 mm size.
- Time resolution around **25 ps**.
- Front-end configurable between Constant Fraction Discrimination (**CFD**) or Leading-Edge Discrimination (**LED**) with 390 ps LSB Time-over-Threshold (**ToT**) measurement.
- Input **polarity** configurable, positive or negative, with 400 mV bias tuning range.
- Input signal dynamic range from **30 µA to 2 mA** for coupling MAPMT / SiPM / MCP-based sensors.
- Channel **recovery time** of less than ~ 8 ns (worst case of input saturation).
- Programmable **signal attenuation** by 25%, 50% or 75%.
- **Test pulse injection** into the analog circuit (through internal test capacitor) or TDC.
- Time-to-Digital Circuit (**TDC**) with per-channel **programmable offset** for time calibration.
- **Hardware time gate** of configurable width up to 6.25 ns (25 ps TDC) or up to 25 ns (100 ps TDC).
- Power consumption of about **200 mW (estimated) per chip** at 1.2 V bias.
- Radiation hardness using **triplication** up to ~ 2 x 10^{13} n_{eq}/cm^2 and ~ 12 kGy.
- Compressed data-driven format using a **packet-builder** at 40 MHz.
- **Aurora protocol** for serialiser link and back-end synchronisation in data-compressed format.
- **Configurable** number (1 to 4) and speed (320, 640 or 1280 Mbps) of **output serialisers**.
- Direct compatibility with next-generation **lpGBT** chipset for controls and data transmission.

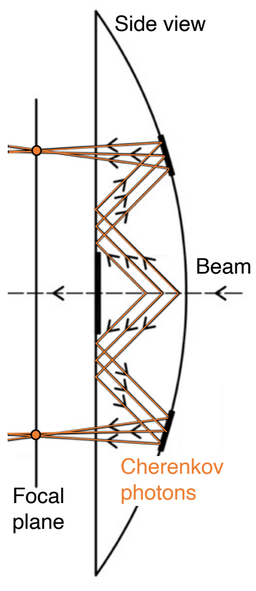
5 Data bandwidth considerations for FastRICH integration

The **photon hit occupancy varies significantly** across the RICH detector planes. To make best use of the available optical links, the number and speed of **FastRICH output serialisers are configurable**. This allows the front-end to be equipped with different densities of the optical link plugins. In high-occupancy regions, more links are used than in low occupancy regions, resulting overall in an optimised data-throughput per optical link.

The large amount of fast-timing data is challenging in view of the high-luminosity LHC environment. Therefore, the **FastRICH includes a unique set of features to reduce data throughput**. A configurable **time gate** reduces the TDC range to typically a few nanoseconds. Hits outside this gate are ignored and the reduced range requires fewer bits per hit timestamp. A **CFD** avoids the need to transmit ToT bits. Owing to the highly optimised **data-driven packet format**, typically 10 to 24 bits per hit (depending on the event) are sent off-detector.

During the 2024 testbeam at the SPS facility, MAPMT (multi-anode photomultiplier tubes) and SiPM (silicon photomultiplier) arrays were read out by prototype fast-timing readout electronics. A borosilicate lens acts as both the Cherenkov radiator and focusing optics. Hit maps from data are overlaid onto the active sensor area in the photograph, demonstrating the detected Cherenkov ring arcs.





Further information

These studies are published in [1] *Sub-nanosecond Cherenkov photon detection for LHCb particle identification in high-occupancy conditions and semiconductor tracking for muon scattering tomography,* F. Keizer (Doctoral thesis), January 2020, DOI:10.17863/CAM.45822 .
For full details on the LS3 Enhancements see [2] *LHCb Particle Identification Enhancement Technical Design Report,* LHCb Collaboration, 2023, CERN-LHCC-2023-005, cern-cds:2866493 .
More information on the Upgrade II can be found in the [3] *Physics case for an LHCb Upgrade II: Opportunities in flavour physics, and beyond, in the HL-LHC era,* LHCb collaboration, 2018, CERN-LHCC-2018-027, arxiv/1808.08865 .
The FastRICH ASIC documentation is available in [4] https://fastrich.docs.cern.ch , and more details on the FastIC are in: *FastIC, a fast integrated circuit for the readout of high-performance detectors,* S. Gomez *et al*, 2022, DOI:10.1088/1748-0221/17/05/C05027 .