Development of a MAPS Upstream Tracker for the LHCb Upgrade II

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Introduction

LHCb detector

- **LHCb detector** is dedicated to the flavor physics studies, serving as a forward general-purpose detector:
  - Forward **single-arm spectrometer** with a unique coverage in pseudo-rapidity(2<η<5)
  - Observing 40% of the **heavy quark** production cross-section in 4% of the solid angle
  - Precision measurement in the **beauty and charm** sectors
  - Study of QCD, EW, heavy ion collisions, etc.
- **Upstream Pixel detector (UP)** is located upstream of the LHCb bending magnet.
- LHCb operates at $\mathcal{L}_{max} = 2 \times 10^{33} cm^{-2} s^{-1}$ since 2022 with an upgraded detector. It will take data at $\mathbf{1.5 \times 10^{34} cm^{-2} s^{-1}}$ during Run 5 & 6, about **×7.5** times higher than Tun 3 & 4. The current UT (upstream tracker) cannot cope with the data rate and the high occupancy (up to ~10%).
- The Upgrade II UP detector will use **COMS Monolithic Active Pixel Sensors(MAPS)** technology.

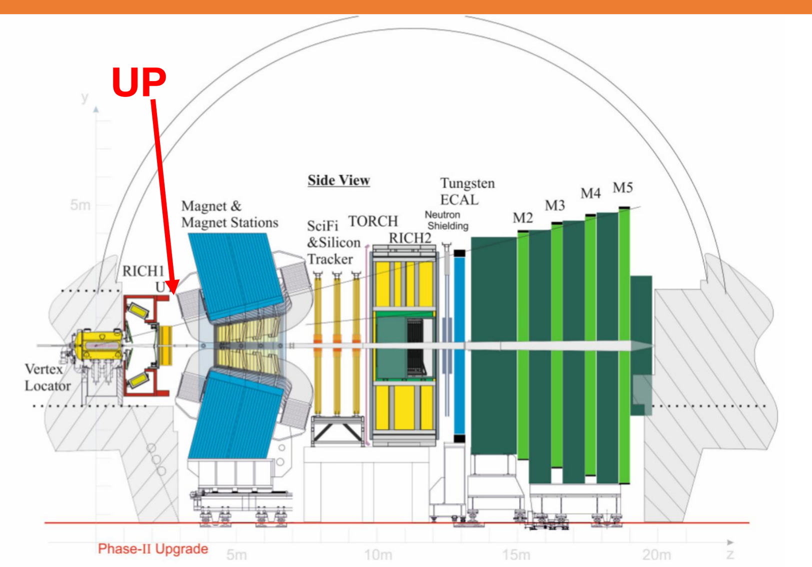

Fig1. LHCb detector at Upgrade II

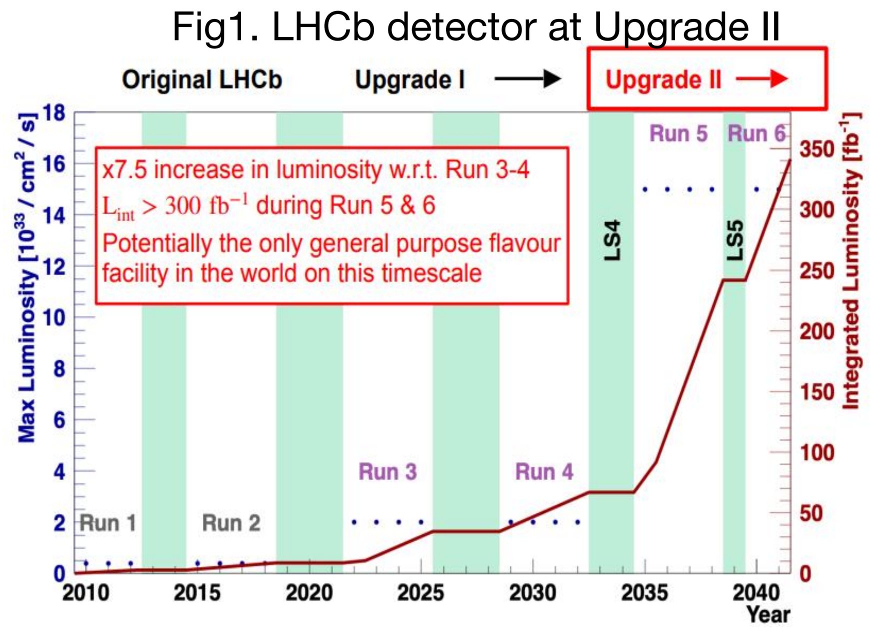

Fig2. LHCb luminosity by year

Detector design

CMOS sensor options

- The CMOS sensors should provide:
  - Good **spatial resolution** especially in horizontal
  - **High radiation hardness:** $3 \times 10^{15} n_{eq} \cdot cm^{-2}$
  - Frontend design provide good **timing resolution: 3-5ns**
- Two approaches are being pursued:
  - High-voltage CMOS (HV-CMOS)

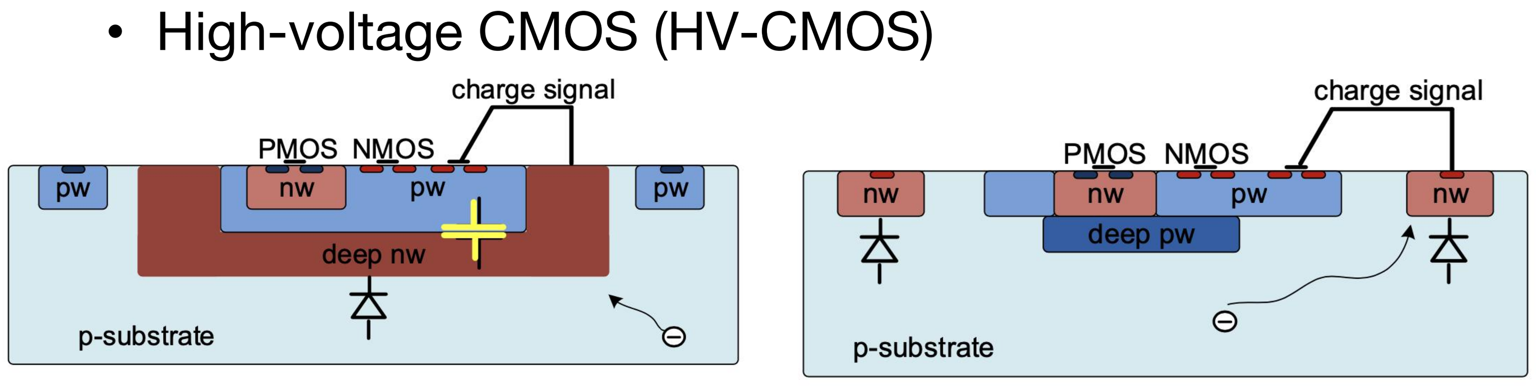

Fig3. The schematic of HV-CMOS (left) and LV-CMOS (right)

Detector design and layout

A potential detector layout is illustrated in Fig.4:

- **Fourteen chips in a 7 × 2 array** are interconnected to a flex circuit to form a module.
- The common HL-LHC radiation tolerant ASIC for data, timing, trigger and control, known as the lpGBT, will be utilized for data acquisition.
- **A total of 32 modules** are mounted alternately on both sides of a supporting bare stave, **in total 10 staves per plane.**
- **A four-plane detector based on HVCMOS is proposed.** Layout using other MAPS technology like LVCMOS is similar.

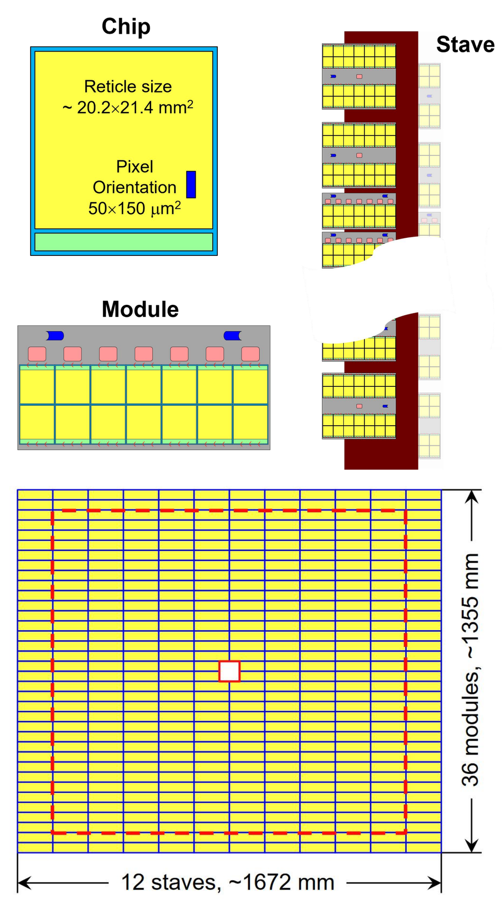

Fig. 4 Geometry construction

HVCMOS sensor COFFEE development

- Two designs of HVCMOS have been produced:
  - COFFEE1: deep N well with **55nm low leakage** process
  - COFFEE2: HVCMOS sensor with **1kΩ·cm wafer**
- IV-test of COFFEE2:
  - Low leakage: ~**10pA**
  - Breakdown: ~**70V**

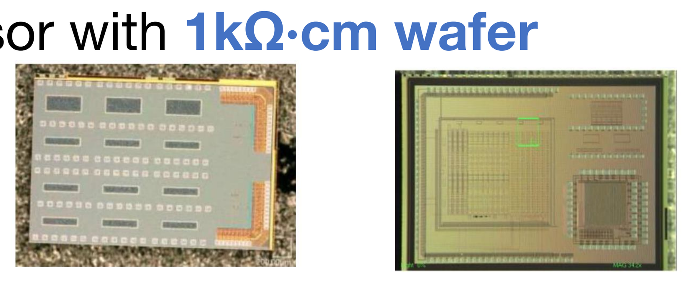

Fig.5 COFFEE1 (left) and COFFEE2 (right) chips

- Beam test at **CSNS Dong guan**
  - 2024 April
  - **10-80 MeV proton**
  - $-28℃ @ 7 \times 10^{14} n_{eq} \cdot cm^{-2}$
  - Room temperature@ $2 \times 10^{11} \sim 1 \times 10^{14} n_{eq} \cdot cm^{-2}$

CMOS SENSOR IN FIFTY-FIVE NM PROCESS

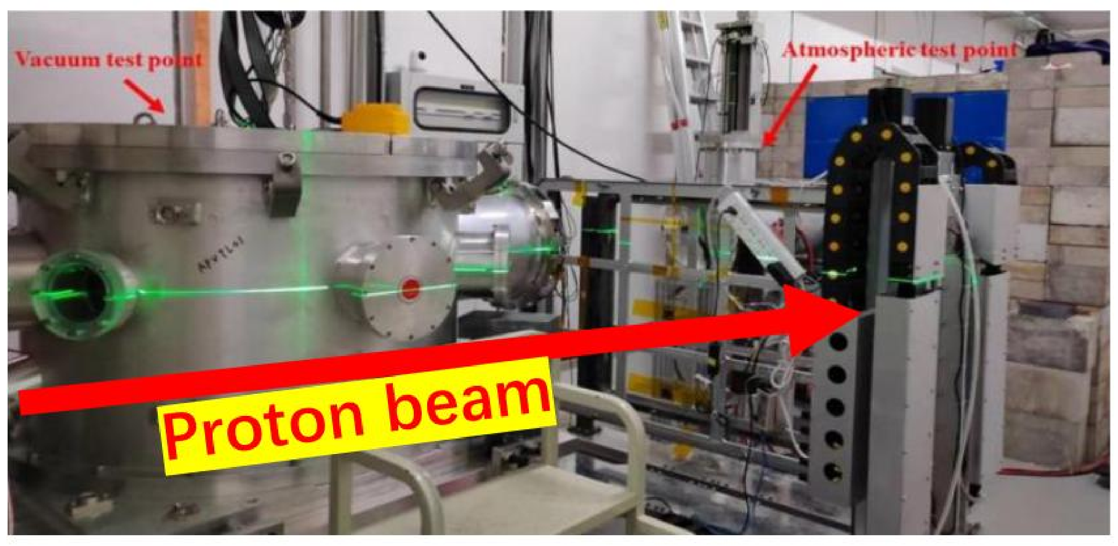

Fig. 6 Beam test setup at CSNS

Simulation

Luminosity simulation

- The performance studies of the **UP detector** are based on simulation samples generated in Upgrade II conditions.
- Detector is described using the **DD4hep** in Gauss/Gaussino framework.
- The center-of-mass energy of p-p collision is $\sqrt{s} = 14TeV$ and the instantaneous luminosity is set to be $\mathbf{1.5 \times 10^{34} cm^{-2} s^{-1}}$, $1.3 \times 10^{34} cm^{-2} s^{-1}$, and $1.0 \times 10^{34} cm^{-2} s^{-1}$
- Fig. 7 shows the hit densities per bunch crossings in p-p collisions with the instantaneous luminosity at $1.5 \times 10^{34} cm^{-2} s^{-1}$.

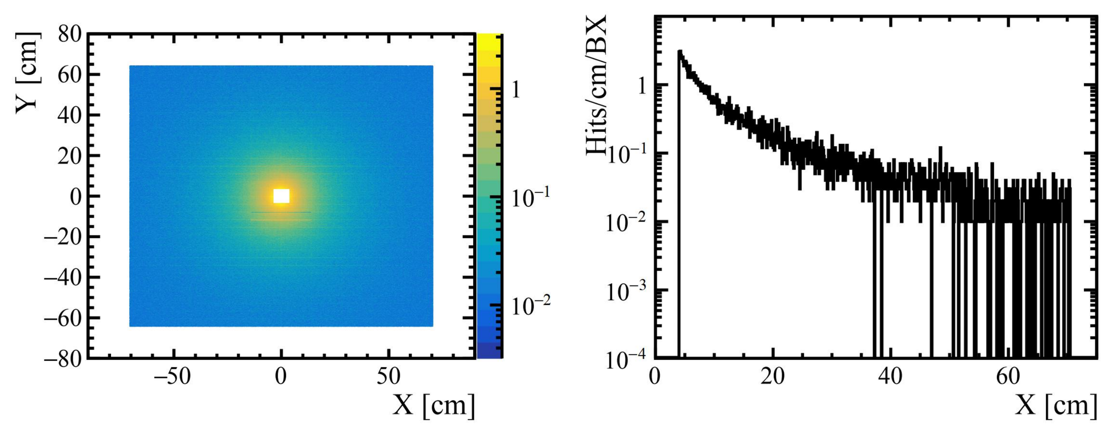

Fig. 7 The UP hit density per PX per cm

Material budget simulation

- **Detector description** has been developed both in DetDesc and DD4hep framework. “Fake digitization” study was based on MCTruth level. The **material budget** scan was performed in two frameworks with consistent results.
- Fig. 8 shows the radiation length of the first layer of UP plane in η/φ view. The last plot shows the projection map on the η axis.

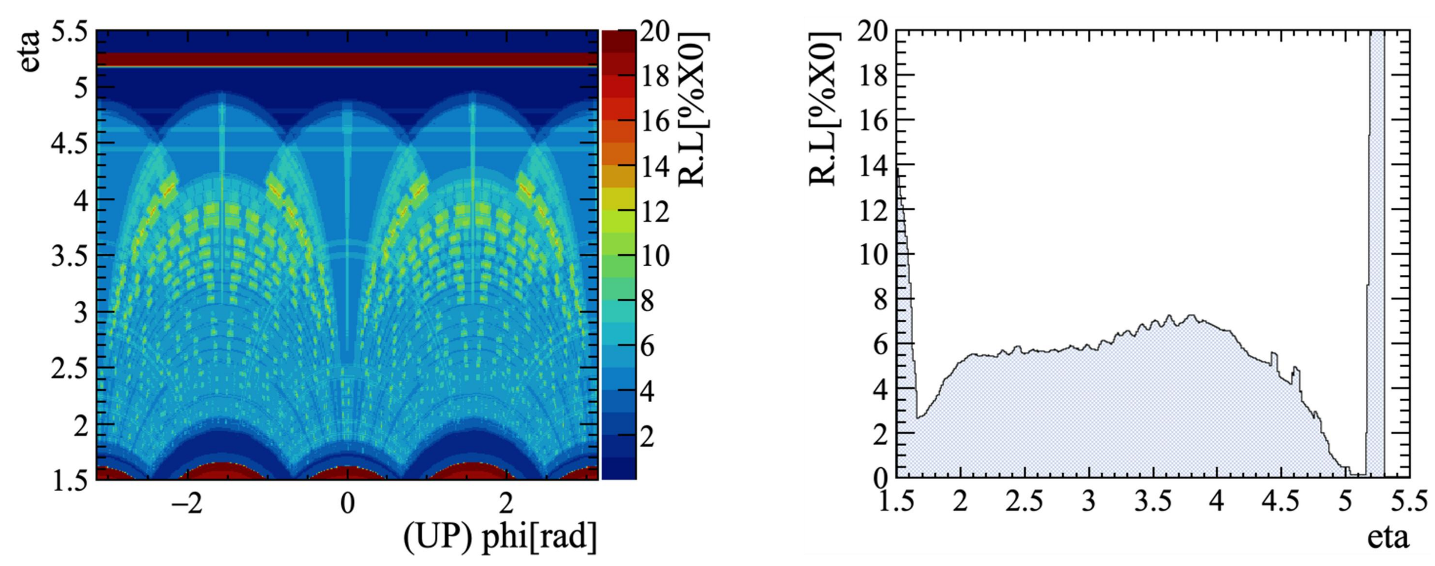

Fig. 8 Radiation length in DD4hep