16th Pisa Meeting on Advanced Detectors

Performance and Test of the New CMS ECAL Barrel Front-end Electronics for HL-LHC

26 May – 1 June 2024, La Biodola – Isola d'Elba (Italy)

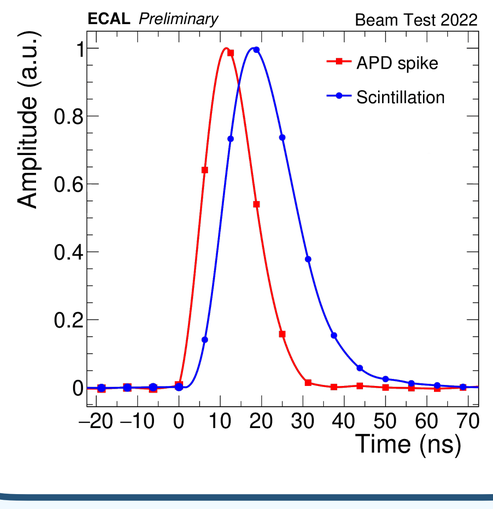
HL-LHC challenges for the CMS ECAL Barrel

- **Increased pile-up:** from 40–60 in LHC Run 3 up to 200 at HL-LHC
- **Detector ageing effects:**
  - Crystal **transparency loss**
  - Increased noise due to **APD leakage current**

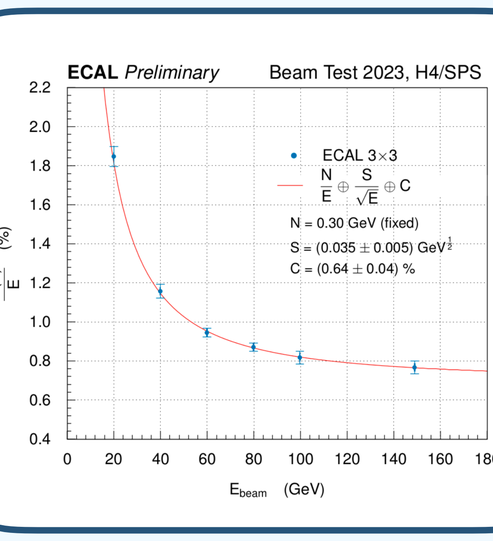
A new faster front-end electronics

- Will **improve time resolution** for better primary vertex reconstruction
  - Target: **<30 ps for E>50 GeV**
  - Higher sampling rate: 40 -> 160 MS/s
  - Faster analog shaping: ~100 -> ~20 ns
- Will **enable the discrimination of scintillation signals from APD spikes** – signals from direct ionisation of the APDs – using pulse shapes

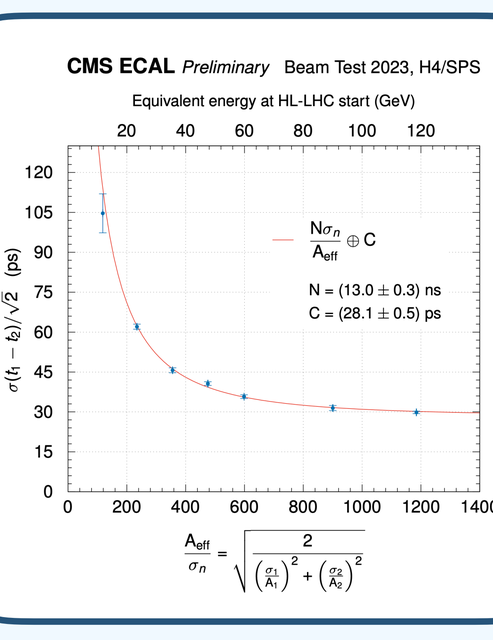
Highlights from beam tests @H4/CERN SPS



Spike discrimination
With the new electronics, a clear difference in the pulse shape between signals and spikes, which have different rising times, can be seen



Energy resolution
Compatible with current electronics: <1% for electrons and photons above 50 GeV



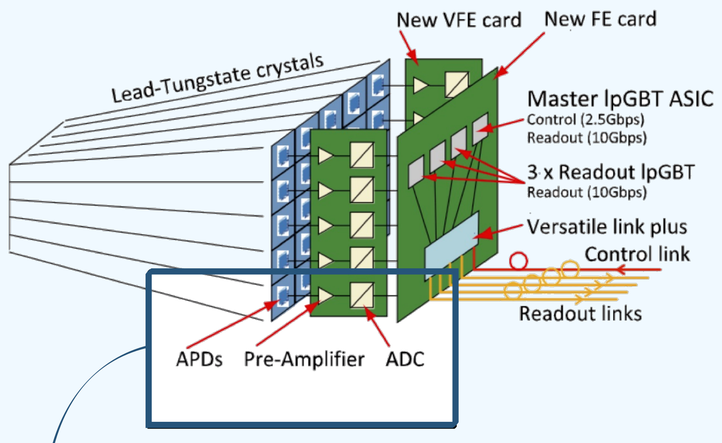
Time resolution
- Compatible with the target of 30 ps above 50 GeV
- The measure is done targeting with the beam a region between two crystals (in two different readout units, read by two different back-end boards) and computing the difference in time between the two

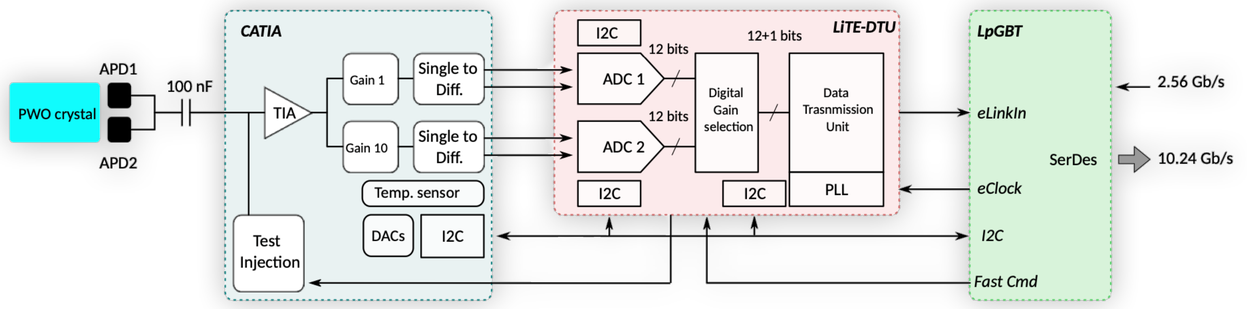
In the **new Readout Unit** — that covers a 5x5 crystal matrix — the geometry, the crystals and the APDs will be unchanged

New electronics cards
- **VFE:** very-front-end card, with 5 readout channels each
- **FE**: front-end card that serializes data from 25 channels
- **LVR**: low voltage regulator card

New back-end card
The **BCP** (Barrel Calorimeter Processor) will take care of readout and trigger operations

New Readout Unit





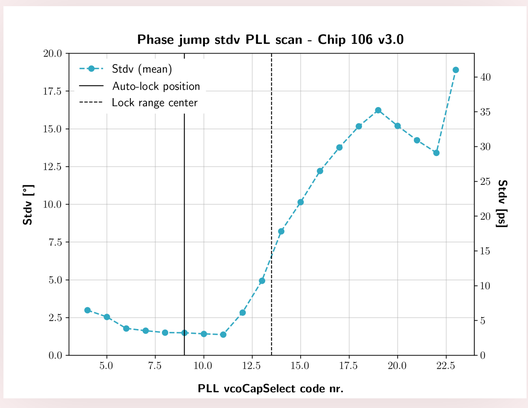
Two new ASICs

CATIA: Calorimeter Trans-Impedance Amplifier
- TMSC 130 nm
- Two gain stages x1 and x10
- Range of G10: 200 GeV
- Range of G1: 2 TeV

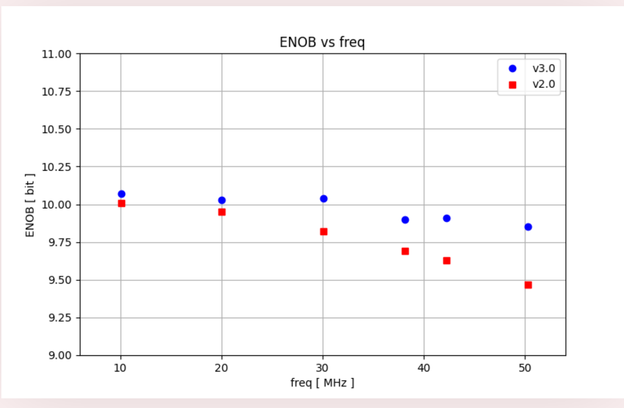
LiTE-DTU: Lisbon Turin ECAL Data Transmission Unit
- TMSC 65 nm
- Two 12-bit 160 MS/s SAR ADCs
- Gain selection mechanism
- Loss-less data compression with simplified Huffman encoding
- 1.28 Gbps serializer unit
- PLL (Phase-Locked Loop) circuit from CERN lpGBT design

Improved performance in the production version of the LiTE-DTU

Changes from v2.0 to v3.0
- PLL power connection improved
- PLL auto-lock feature implemented
- Separate resets for PLL and digital logic
- Other minor improvements and bug fix



The **PLL performance improved**, and the auto-lock feature showed to be able to select an optimal value in order to minimise the jitter; the **phase relation with the input clock is constant** after multiple reconfigurations



The **Effective Number of Bits** (ENOB) increased in v3.0.
This is the result of a **lower jitter**, achieved by improving the PLL power connection, and thanks to the auto-lock feature

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