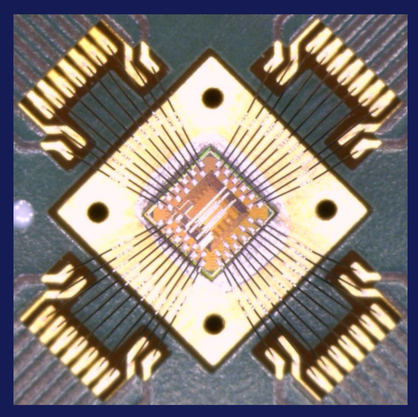
First Experimental Results on Ignite0: a prototype Pixel Front-End ASIC with Timing in 28 nm



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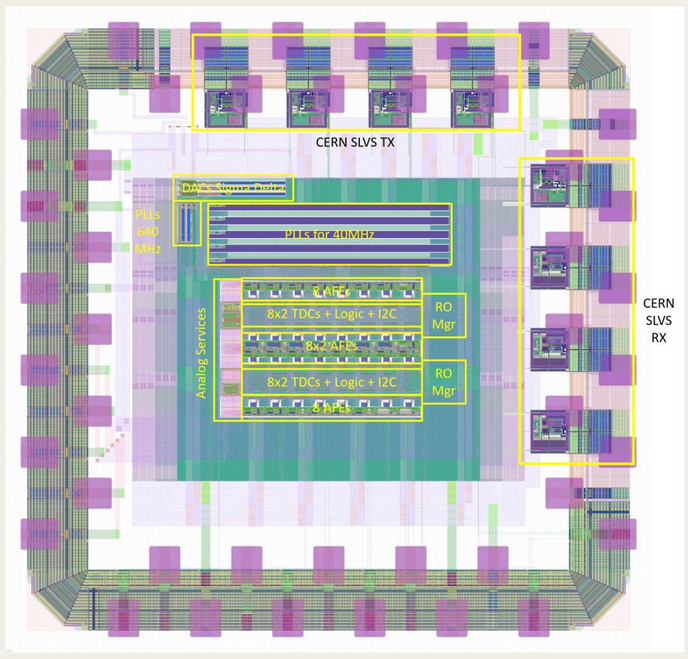
Abstract

This poster presents the results of the first test activity on the *Ignite-0* ASIC. The main challenge of this microelectronics development is to reach an overall time resolution of at least 50ps, on a pixel-front end ASIC within the constraints defined by high-luminosity HEP experiments.
Ignite-0 has been developed during 2023 in order to test individually the building blocks for the future developments on the front-end ASIC. It contains mainly the pixel front-end electronics such as the Analog Front-End (AFE) and the Time to Digital Converter (TDC), but it also integrates various service blocks such as a $\Sigma\Delta$ DAC and two different PLL architectures. All the integrated blocks have been designed to satisfy the desired requirements and constraints both in terms of power, performance and form-factor.
Both in terms of the AFE and the TDC, the implemented architectures were developed on the basis of the ones of the Timespot1 front-end ASIC [2] [4] in order to improve their performance and reliability. Moreover, six different AFE architectures were investigated in order to test different combinations of the preamplifier and discriminator.

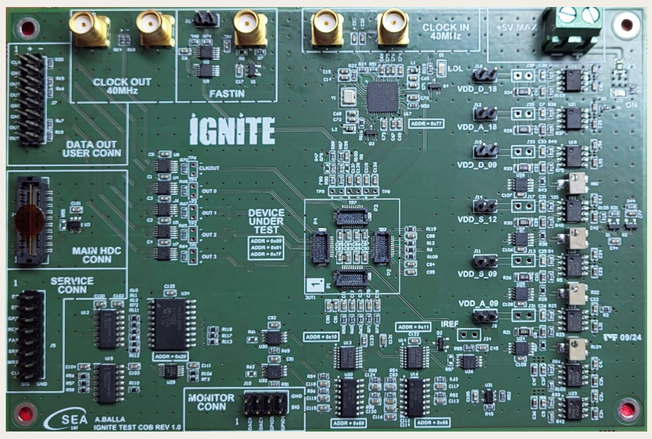
Ignite0 ASIC Layout



1 mm x 1 mm

Ignite0 features a small pixel matrix of 8 × 4 channels. Each AFE and TDC can be tested independently or chained together. The AFE is not connectable to and actual sensor, but a sensor emulator is present in the chip. The channels can be pulsed via a fast asynchronous differential digital input signal. The performance of the PLLs and DACs can also be tested independently. A combination of outputs can be directly measured outside the ASIC via two fast digital outputs. This setup is able to measure the DUT jitter with a precision of 5 ps rms.

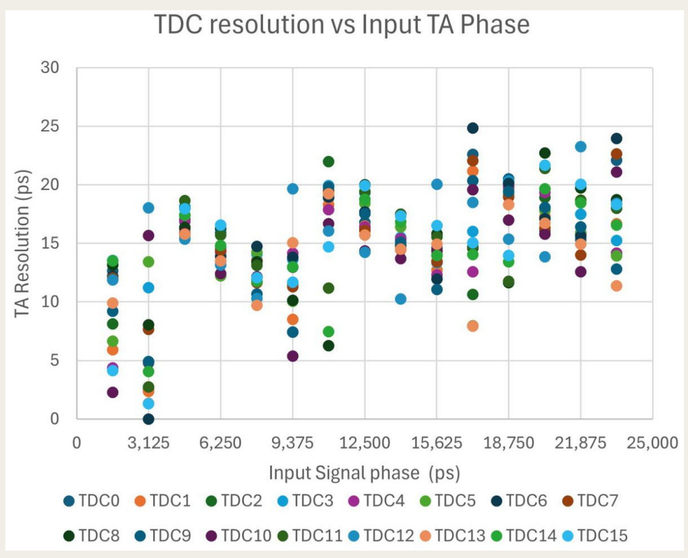
The Ignite0 Test Board

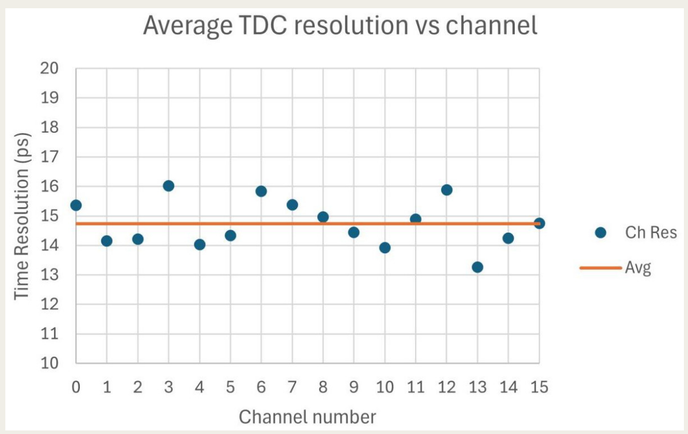


15 cm x 10 cm

The test board is divided in two modules: the mother board containing all the discrete components, and a DUT-board which only contains the Ignite0 ASIC. This configuration allows to quickly swap the DUT. The whole system, including the ASIC, can be configured and read via an I^2C interface. A clean system clock is generated on board via a dedicated component.

First Test Results



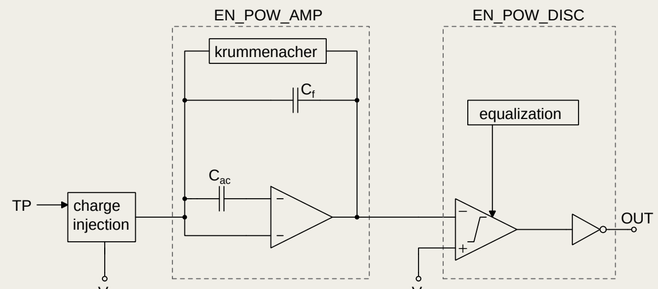


The TDC resolution has been evaluated using an internal pulsing scheme. This allows to inject a signal with 15 difference phases in regard to the reference clock. The resolution has been evaluated as the rms error between the measurement and the expected result on sets of 500 measures. In this architecture, the main sources of resolution variability are the per-channel variations and the input signal phase. The TDC shows an average resolution of 15 ps rms, well in accordance with what it is expected based on simulations. The reference clock period jitter has been measured to be under 5 ps rms. Further tests on the ASIC are ongoing, and will be presented soon.

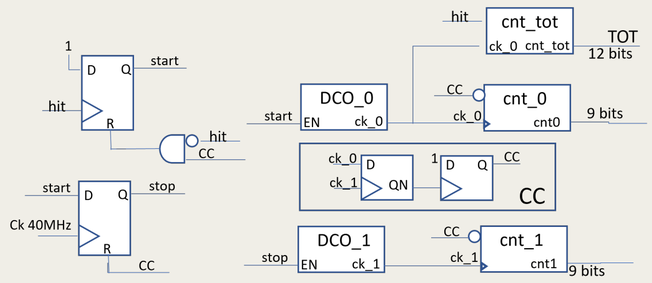
The IGNITE Project

The IGNITE project (INFN Ground-up INITiative-on micro-Electronics developments) [1] aims to develop integrated micro-systems suitable for particle tracking in the next generation of high-luminosity experiment at the LHC. This objective involves the following system level requirements: a pixel pitch of $\sim$ 50 µm, a time resolution of at least 50 ps and a sustainable event rate up to 10 GHz/cm^2. These specifications must be met within specific constraints: a $\sim$ 1.5 W/cm^2 power consumption, a radiation tolerance to TID up to 1 Grad, and a material budget of 0.5 % Xo at most. The investigated system-level technological solutions include: a 28 nm CMOS front-end chip coupled with a silicon 3D sensor [3], a system assembly leveraging 3D integration technologies and an integrated optical read-out.

Pixel Architecture



The ASICs implements different architectures for both the amplifier and the discriminator equalization. The Amplifiers are all inverter based, both in with and without a cascode configuration. One equalization scheme is based on a discrete-time offset-compensation circuit, the other is based on a local fine-tune DAC. Both solutions require only two global reference voltages and digital controls. The AFE can be configured to consume between 4 µW and 20 µW of power.



The TDC is implemented with a Vernier scheme, in which the time is measured by counting the number of oscillations of two slightly de-tuned Digital Controlled Oscillators (DCO). Both the DCO are calibrated automatically with an internal procedure. The main advantage of this scheme is its low inactive power consumption.

Expected Performance

- TDC: average Time over Arrival (TA) resolution of 15 ps rms, using a 40 MHz reference clock with a period jitter of 6 ps. The Time over Threshold (ToT) resolution is 260 ps, with a range of 4 µs. The average power consumption is 2.5 µW at 200 kHz signal rate.
- AFE: 25 ps TA resolution and 200 ps ToT resolution in nominal conditions: 1 fC input charge, 100 fF input capacitance, 10 µW of per-channel power consumption, 1000 e^- discriminator threshold. In this condition, the expected TA is 0.5 ns and the ToT is 10 ns.
- PLL: output clock period jitter of 5 ps rms, with an input clock with 25 ps rsm.

References

[1] Sandro Cadeddu, Gian Matteo Cossu, Luca Frontini, Adriano Lai, Valentino Liberali, Lorenzo Piccolo, and Alberto Stabile. "Recent developments in the IGNITE project on front-end design in CMOS 28-nm technology". In: *JINST* 19.01 (2024), p. C01040. DOI: 10.1088/1748-0221/19/01/C01040.

[2] Sandro Cadeddu, Luca Frontini, Adriano Lai, Valentino Liberali, Lorenzo Piccolo, Angelo Rivetti, Jafar Shojaii, and Alberto Stabile. "Timespot1: a 28 nm CMOS Pixel Read-Out ASIC for 4D Tracking at High Rates". In: *JINST* 18.03 (2023), P03034. DOI: 10.1088/1748-0221/18/03/P03034. arXiv: 2209.13242 [physics.ins-det].

[3] A. Lampis et al. "Characterisation of highly irradiated 3D trench silicon pixel sensors for 4D tracking with 10 ps timing accuracy". In: *Front. in Phys.* 12 (2024), p. 1393019. DOI: 10.3389/fphy.2024.1393019.

[4] A. Loi et al. "A prototype 4D-tracking demonstrator based on the TimeSPOT developments". In: *JINST* 19.02 (2024), p. C02069. DOI: 10.1088/1748-0221/19/02/C02069.