The OBELIX Chip for the Belle II VTX Upgrade

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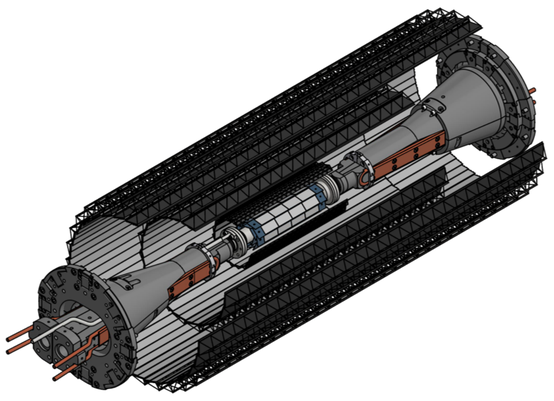
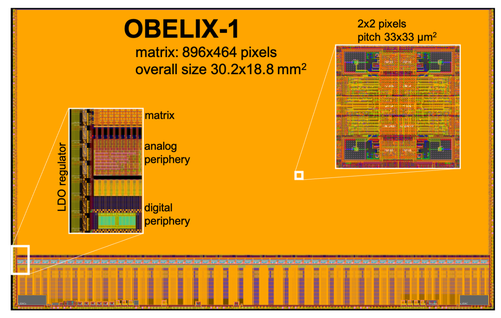
The VTX Upgrade

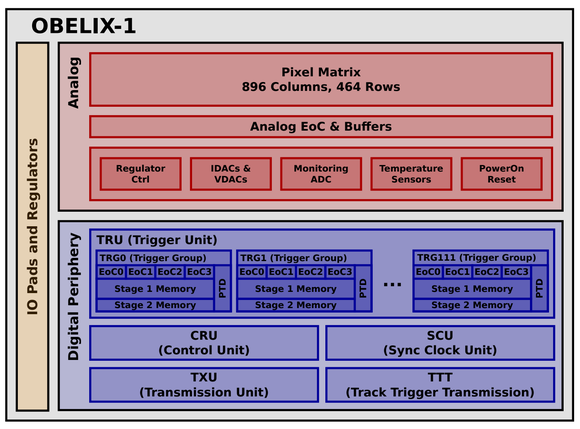
- Opportunity to upgrade the Belle II Vertex Detector during Long Shutdown 2 (Around 2028)
- Interaction region is likely upgraded: Rework of the Vertex Detector necessary
- Improves tracking performance at increased beam background due to luminosity increase
- Five layers with the same DMAPS sensor: The OBELIX (**O**ptimized **BEL**le II p**IX**el) Chip
- Fully pixelated design for low occupancy and fake-rate at high hitrates
- iVTX (2 inner layers): Self supported, air cooled, all silicon ladders, with redistribution layer
- oVTX (3 outer layers): Carbon fiber support, liquid cooled
- See Talk from G. Rizzo on Tuesday





The OBELIX Chip

- Matrix inherited from TJ-Monopix2
- 464 rows and 896 columns
- Timestamp period: 47 ns
- Up to 10 µs trigger latency
- Power: $< 200\,\mathrm{mW/cm^2}$
- TID tolerance: 1 MGy
- NIEL tolerance: $5 \times 10^{14}\,\mathrm{n_{eq}/cm^2}$
- Hitrates up to $120\,\mathrm{MHz/cm^2}$
- Supply: 2 to 3 V

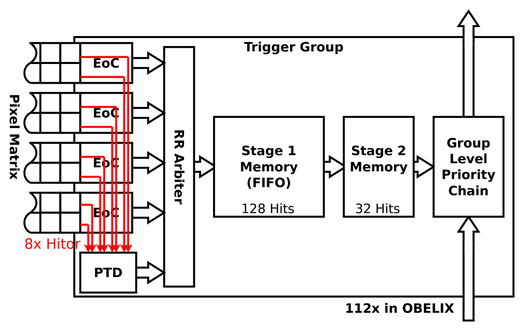


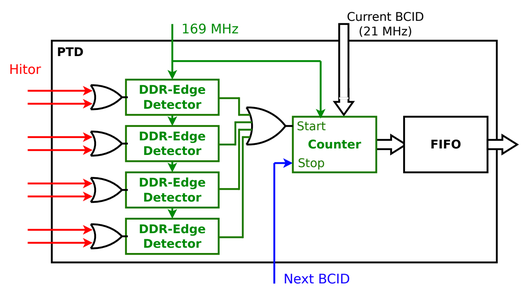
New On-chip features

- Trigger memory
- Precision timing measurement (PTD)
- Transmission for trigger contribution (TTT)
- LDOs for wide supply voltage range
- Several temperature sensors across the chip
- Monitoring ADC for power and temperature

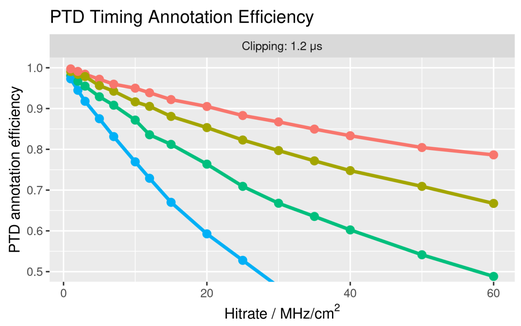
Peripheral Time to Digital Converter (PTD)

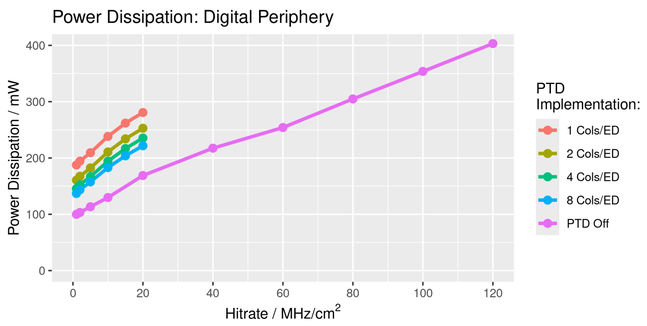
- Precision timing feature (enabled via configuration)
- Uses the HitOr lines to measure timing
- HitOr: Discriminator outputs chained via OR-gates along each column
- Timing resolution < 2 ns after calibration from measurements with TJ-Monopix2
- After irradiation (with VTX total design fluence): < 3 ns
- OBELIX: Sampling in the periphery with 3 ns period (196 MHz and DDR)
- Result is injected into datastream
- Association of hit-data with PTD-data (offline)
- Dead-time and not always possible without ambiguities





- Design decision: Number of columns per ED
- Impacts performance and power consumption
- Decision depends on power budget consideration of other modules
- Evaluation and decision is still ongoing

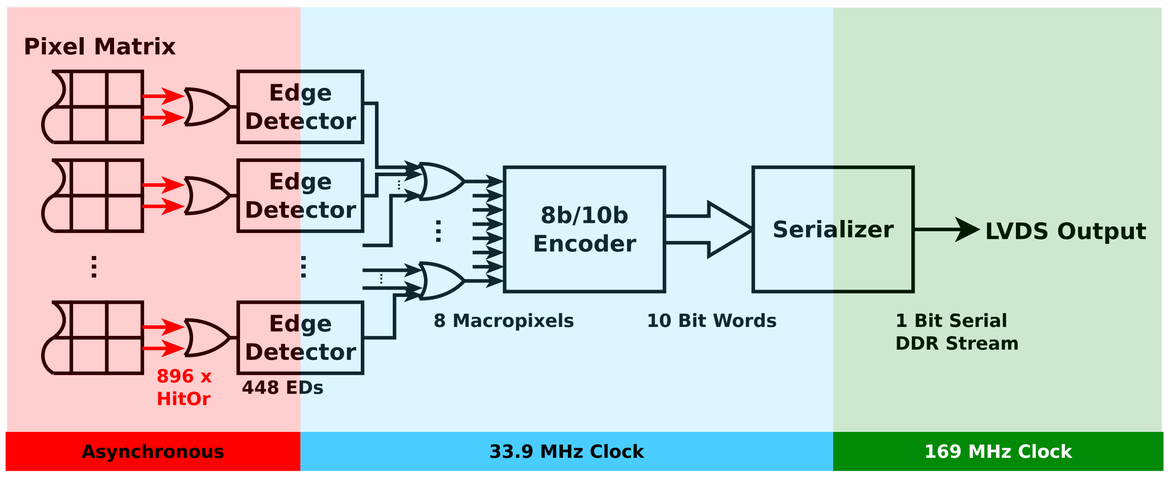




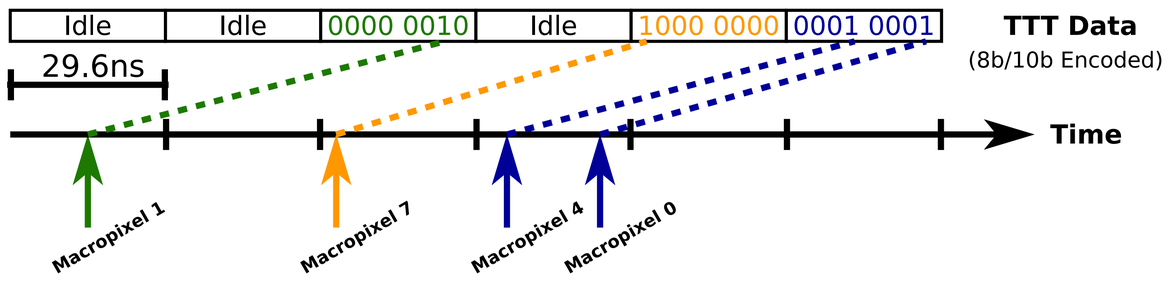
- Lower hitrate ($< 10\,\mathrm{MHz/cm^2}$) in oVTX
- Power consuming feature: PTD enabled in oVTX
- Extensive calibration for timewalk and gate-delays necessary

Track Trigger Transmission (TTT)

- OBELIX can contribute to the trigger decision
- This can be used to build a VTX track trigger
- Datapath independent from normal readout (extra LVDS line)
- Chip is divided into small number of macropixels (2 to 8 depending on wiring)
- Any hit inside a macropixel region activates the macropixel
- Time binning: 29.5 ns, 8b/10b encoded stream, one bit per macropixel
- Only enabled in oVTX

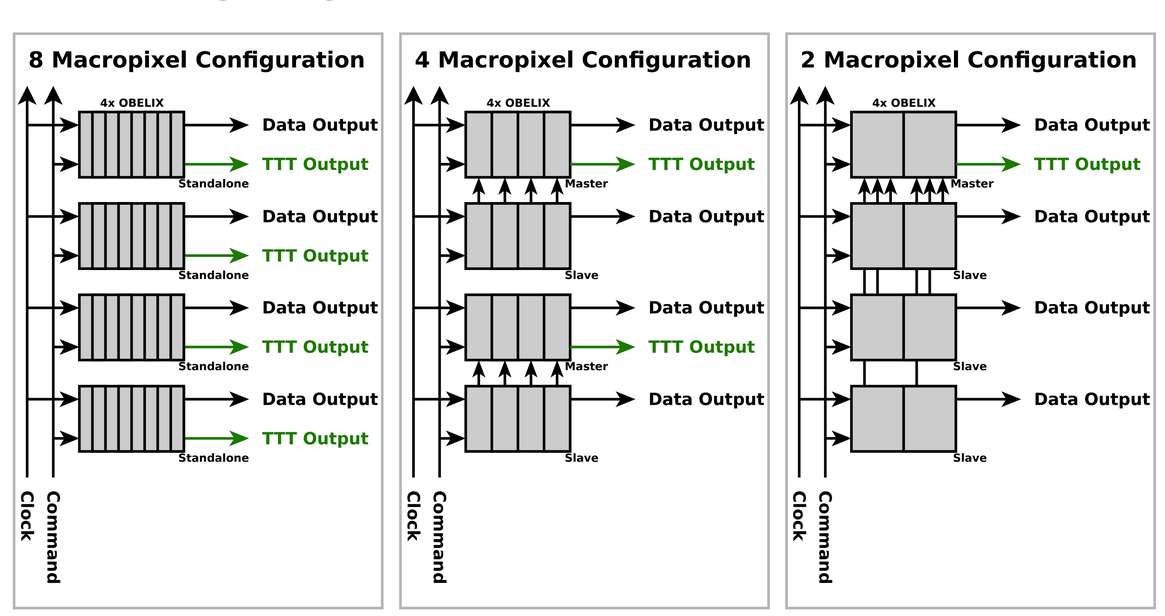


TTT Data Format and Flow



- No frame structure, each byte corresponds to one time-bin
- Each bit in byte corresponds to one macropixel
- Fixed latency (100 ns), high bandwidth
- Synchronization via command input

Possible Wiring Configurations



- In standalone mode, one additional LVDS line per chip
- For 4 macropixel per chip operation, two chips can share this transmission line
- With only two macropixels, four chips can share one line
- The operation mode can be configured by different wiring with the same chip