Design and performance of the readout chip in the Si(Li) tracker module of the GAPS experiment

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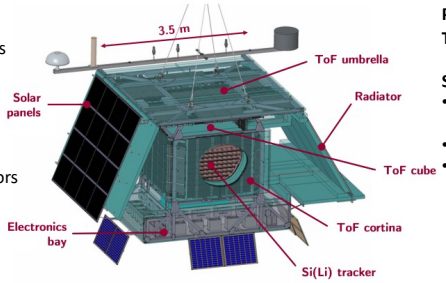
Introduction

This work reports the experimental results from the characterization of a semiconductor detector module, that is the basic unit of the tracker for the General AntiParticle Spectrometer (GAPS) balloon mission. In the austral summer of 2024, GAPS will search for an indirect signature of dark matter through the detection of low-energy (< 0.25 GeV/n) cosmic-ray antiprotons, antideuterons, and antihelium.

The GAPS instrument

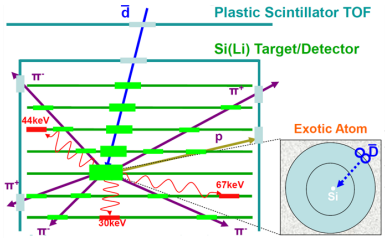
Time-of-Flight System (TOF)
- 160 plastic scintillator paddles with Si-PM readout

Si(Li) Tracker
- ~1000 Si(Li) detectors
- 10 layers with 10 cm spacing
  - 7 with Si(Li) detectors
  - 1 with both Si(Li) detectors and dummy modules
  - 2 with dummy modules



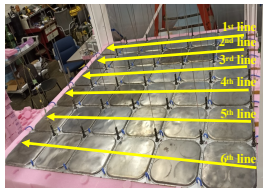
Particle identification:
TOF system measures velocity and dE/dx

Si(Li) Tracker functions as
- Target to slow an incoming antiparticle and capture it into an exotic atom in an excited state
- Spectrometer for de-excitation X-rays
- Tracker to measure antinucleus dE/dx and stopping depth, and annihilation products from nuclear decay

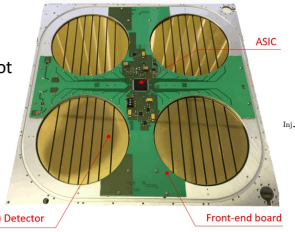


The GAPS Tracker

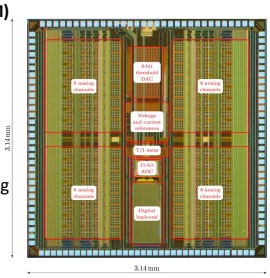
- Tracker composed by 10 layers of 6x6 modules
- Each layer with modules arranged in 6 lines (every line shares the same low power supply voltage)



Module:
- 4 sensors (8 strips per sensor)
- 1 readout ASIC
- 1 front-end board
- Mechanical support
- Top and bottom windows (not shown)



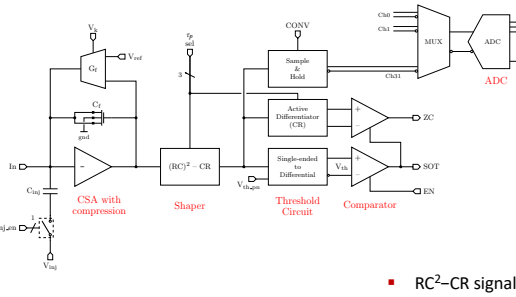
Front-end electronics requirements
- Channels per ASIC: 32
- Operating temperature: **-40 ° C**
- Power dissipation: < 10 mW/ch
- Signal polarity: electrons
- Dynamic range: 10 keV-100 MeV
- Analog Resolution: **4 keV (FWHM) detector capacitance 40 pF**
- Detector leakage current: **5-10 nA**
- Event rate: 100 Hz

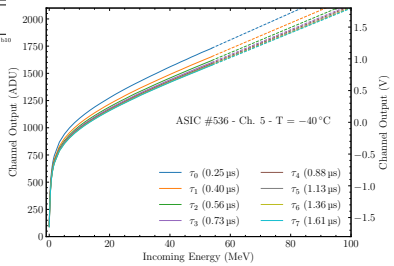


- 11-bits ADC
- Digital Back End (registers control, SPI, ...)
- 8-bit DAC for global threshold setting
- 3-bit DAC for threshold fine trimming
- Detector leakage current readout
- Temperature sensor readout

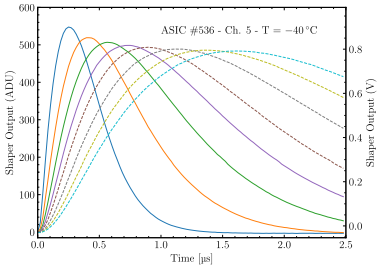
The SLIDER 32 Front-End ASIC

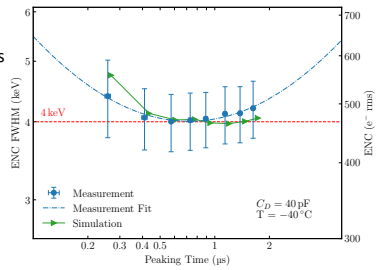
- 180 nm CMOS technology
- **Low-noise analog front-end with dynamic signal compression** for high dynamic range (from low-energy X-rays to high energy proton and pion annihilation products)



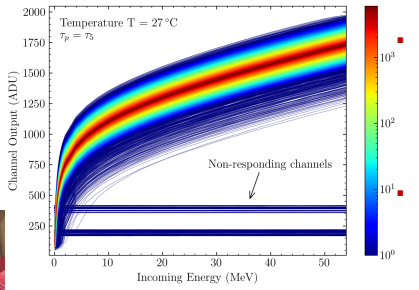


- RC²–CR signal shaping with peaking time 0.25 µs – 1.6 µs
- 4 keV energy resolution at peaking times 0.5 – 1 µs

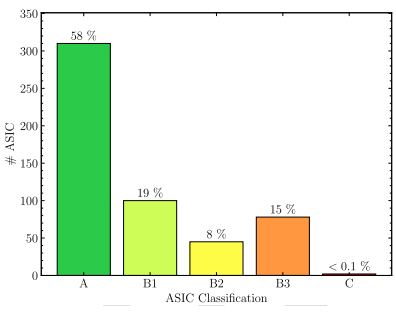




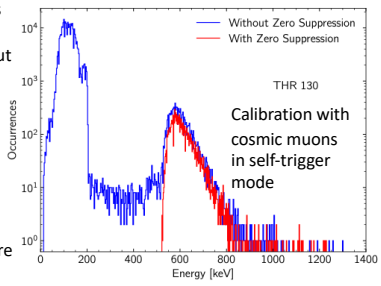
ASIC selection and testing



- Test results for 535 ASICs, about 17000 channels
- 58% fully functional ASICs at room temperature



Muon detection



Calibration with cosmic muons in self-trigger mode

GAPS timeline

- ❖ Fall 2021/Winter 2022: GAPS Functional Prototype built at MIT Bates Laboratory
- ❖ Fall 2022/Winter 2023: GAPS integration at Berkeley Space Sciences Lab
- ❖ June 2023: TVAC testing at NTS Lab in El Segundo, CA
- ❖ Fall 2023: Rebuild at Columbia Nevis Lab, NY
- ❖ June/July 2024: Hang test at NASA facilities in Palestine, TX
- ❖ Fall 2024: Ship to Antarctica for launch during 24-25 season

References

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