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A Time-over-Threshold based analog front-end in 28 nm CMOS for pixel detectors in future colliders

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This work is concerned with the design of an analog front-end processor for the readout of pixel detectors in future high energy physics experiments. The front-end circuit is being developed, in a 28 nm CMOS technology, in the framework of the INFN Falaphel project, whose ultimate goal is the integration of silicon photonic devices with rad-hard electronics in the 28 nm node, and which targets the requirements for optical data readout in future trackers such as the one at the hadronic Future Circular Collider experiments.
The front-end circuit being developed consists of a shaper-less architecture which leverages the Time-Over-Threshold (ToT) technique for the analog-to-digital conversion of the signal from the detector. It includes a charge sensitive amplifier (CSA), designed to cope with large (of the order of tens of nanoamps) detector leakage currents, connected to a pre-comparator stage converting the single-ended signal at the CSA output to a differential one. The pre-comparator output is fed to a discriminator stage, implemented by means of a straight differential pair with active load. A 5-bit threshold tuning DAC is implemented at the pre-comparator level in the analog processor chain.
Post-layout simulation results show that the circuit, operated with a nominal current close to 4.5 uA and a supply voltage of 0.9 V, is able to operate at threshold levels well below 1000 electrons. A prototype chip including a matrix of 8x32 readout channels will be submitted in a mini@sic run in April 2024.
The full description of the analog front-end and of the prototype chip being designed will be provided in the conference paper, together with the main simulation results.

Collaboration

Role of Submitter

I am the presenter

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