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A Time-over-Threshold based analog front-end in 28 nm CMOS for pixel detectors in future colliders

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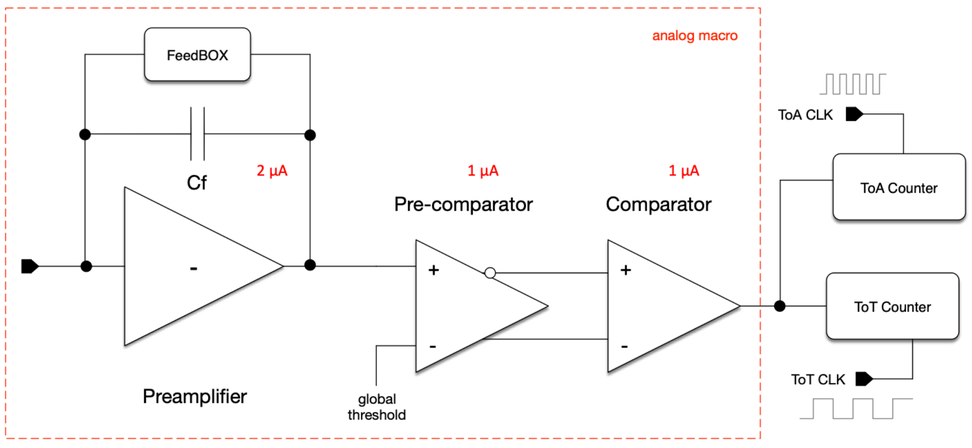
PRIN PiHEX project

Introduction

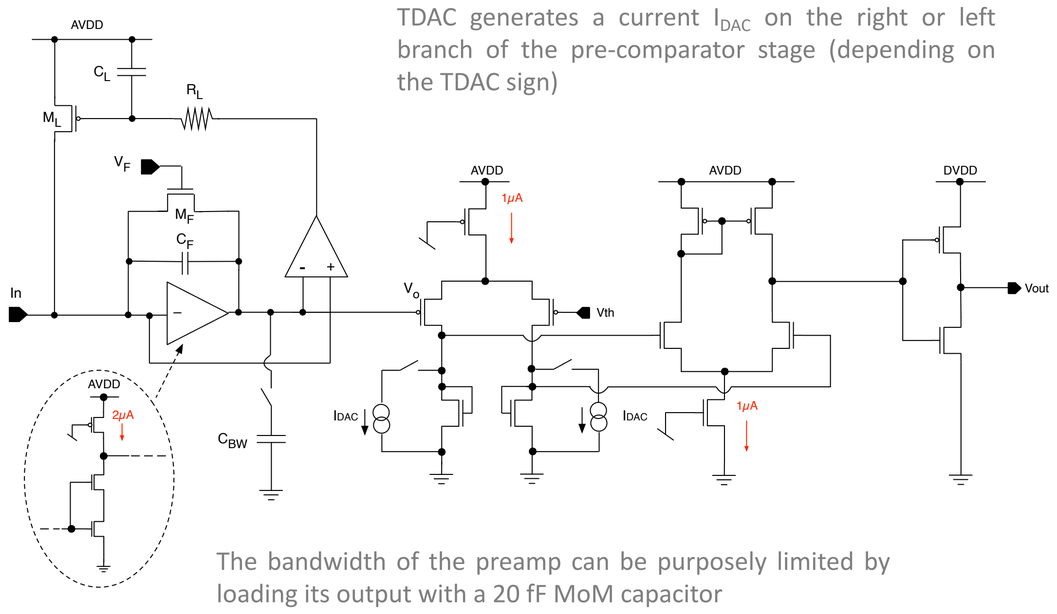
State-of-the-art pixel front-end electronics has been developed by the CERN **RD53** collaboration in a **65 nm CMOS** technology. The chips designed by the collaboration have successfully met the requirements of ATLAS and CMS pixels at the **High-Luminosity Large Hadron Collider** (HL-LHC). Looking ahead, the HEP microelectronics community is now focusing on the **28 nm CMOS** technology for future developments. The work presented here is concerned with the design of **analog front-end circuits** for future, high-rate pixel detectors in 28 nm. Specifically, the work is part of the PRIN project called **PiHEX**, funded by Italian Ministry of University and Research, which aims at improving the state-of-the-art of pixel readout chip technology at high luminosity colliders and for X-ray imagers at the next generation free electron lasers by developing the fundamental microelectronic building blocks for pixel readout ASICs. The project is synergic with the INFN **Falaphel** project, aiming at the integration of silicon photonics modulators with high-speed, radiation-hard. electronics in 28 nm. This technology could potentially be exploited for the replacement of the inner pixel systems of the HL-LHC experiments after 2030.

The analog front-end



Time-over-Threshold (ToT) based front-end

- **preamplifier** with detector leakage compensation circuit
- differential **comparator** (to improve the immunity to interferences)
- 5-bit (+ 1 bit sign) threshold **tuning DAC (TDAC)**
- **ToT** counter for A/D conversion of the signal
- **ToA** counter for time-walk measurements (in the prototype chip)

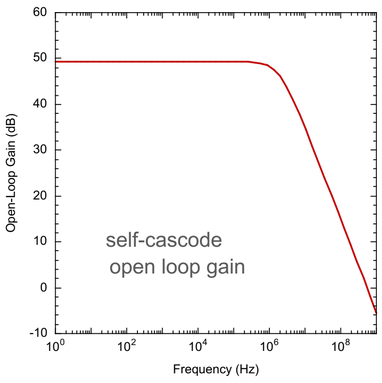


TDAC generates a current I_{DAC} on the right or left branch of the pre-comparator stage (depending on the TDAC sign)

The bandwidth of the preamp can be purposely limited by loading its output with a 20 fF MoM capacitor

Preamplifier

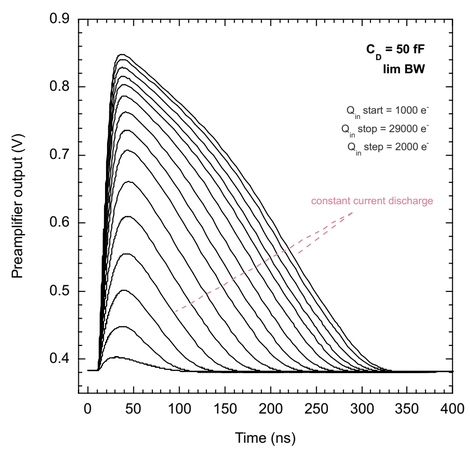
- self-cascode gain stage
- two independent feedbacks, one for signal processing and the other for detector leakage compensation

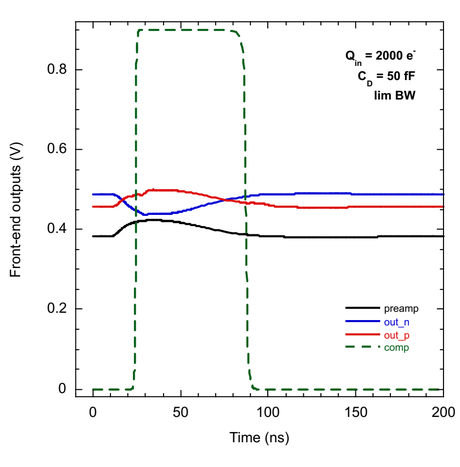


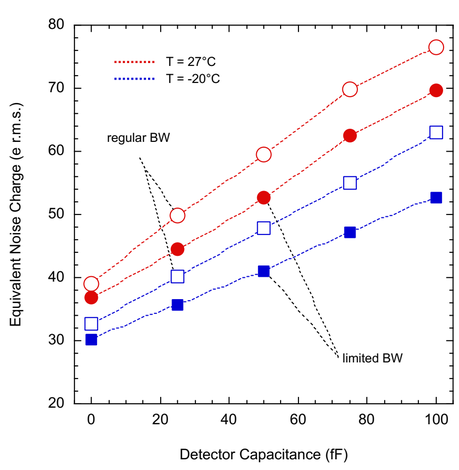
Comparator

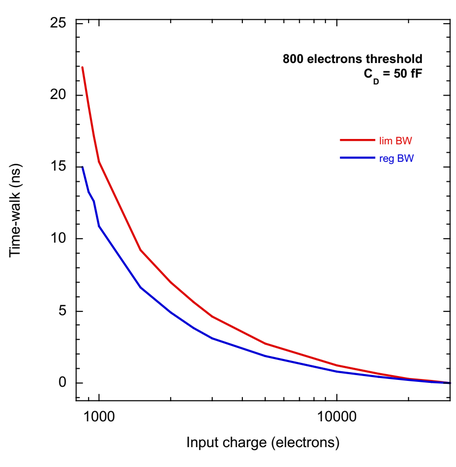
- pre-comparator stage featuring differential input pair loaded with diode connected transistors → single-ended to differential signal conversion
- standard differential pair with active load + output inverter

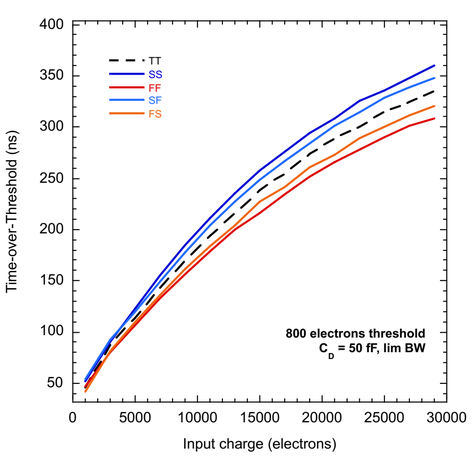
Simulation results





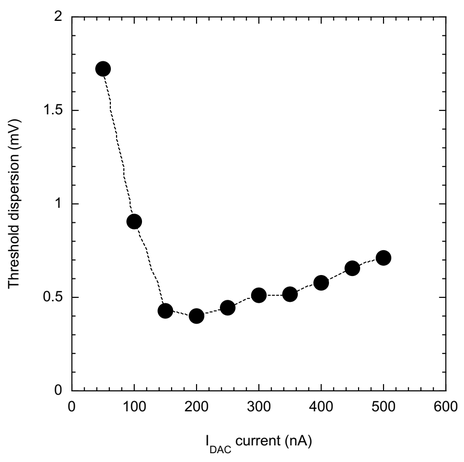


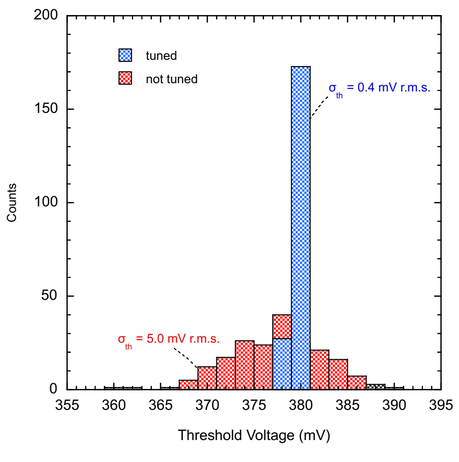


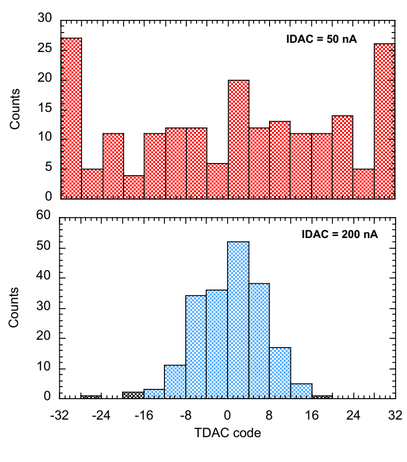


- **Preamplifier output** for an input charge from 1 to 29 ke$^-$ → charge sensitivity of **25 mV/ke$^-$**
- Preamplifier, pre-comparator and inverter output in response to a **2 ke$^-$ signal**
- **ENC** as a function of detector cap for regular and limited preamp BW (room T and -20°C)

- **Time walk** vs input charge for limited and regular BW preamp
  - Time walk < 15 ns for the regular BW version
- **ToT** as a function of the input charge (~linear up to 12 ke$^-$) in a four corners simulation

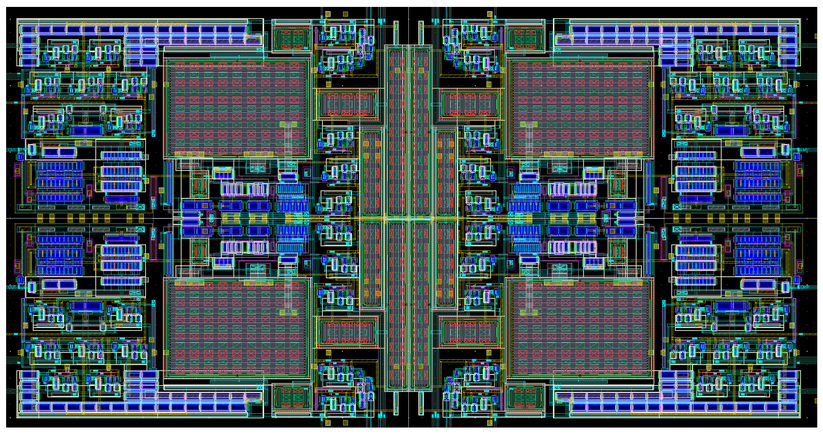






- **Threshold dispersion** (pre-comparator input, in mV) as a function of TDAC current
  - Optimum @ I_{DAC} = 200 nA → threshold dispersion of 0.4 mV (~**16 e r.m.s.**)
- **Threshold distribution** before and after TDAC tuning (dispersion is reduced by a factor ~12)
- **TDAC codes distribution** in the optimum condition (I_{DAC}= 200 nA) and in the case of a too small TDAC range

Analog macro layout



- **Analog island** arrangement (2x2 pixels)
- Analog macro size → **30 x 17 µm^2**
- To be integrated in an **8x32 matrix** of readout channels