# The ATLAS RPC Phase-II Upgrade for High Luminosity LHC era



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RPC detectors play a crucial role in triggering events containing muons in the central region of ATLAS [1]. In view of the HL-LHC program, the existing RPC system, consisting of six independent concentric cylindrical detector layers each providing a full space time localization of hits, is currently facing a significant upgrade. In the next few years, 306 triplets of new generation RPCs will be installed in the innermost region of the ATLAS Muon Barrel Spectrometer [2], increasing from 6 to 9 the number of tracking layers, doubling the trigger lever arm. This allows a substantial enhancement of the present trigger redundancy, increasing the coverage from 76% to 96% approximately. The new chamber design is based on a very efficient integration of an innovative frontend electronics within the detector Faraday cage, allowing to operate the RPCs with an order of magnitude less of average charge per count, correspondingly increasing rate capability and longevity. Fitting new chambers in the narrow space left in ATLAS inner barrel was a challenge, achieved by optimizing RPC materials and thickness, featuring a 1 mm gas gap (instead of 2 mm), and 1.4 mm resistive electrodes (instead of 1.8 mm). Both sides of RPCs are readout by strip panels oriented to measure the bending coordinate of the muon spectrometer, while the second coordinate is reconstructed from the time difference of signal drift at opposite detector's ends. To achieve such results, a 100 ps precise TDC has been integrated in the front-end electronics ASIC. The expected time resolution of a single 1 mm RPC gas gap is approximately 300 ps, and the possibility of a stand-alone Time of Flight measurement will have a huge impact on ATLAS searches for massive long-lived particles. An overview and the present status of the ATLAS RPC Phase II project will be presented.

## MUON SPECTROMETER PHASE-II

Installation of new layer of triplet Resistive Plate Chambers (RPC) and replacement of Monitored Drift Tubes (MDT) with Small MDT (sMDT).



### **RPC-BI CHAMBERS UPGRADE**

- Present RPC chambers face operational challenges at HL-LHC due to reduced performance requirements, necessitating operation at lower efficiency by reducing gas gain through voltage adjustments.
- New RPC chambers with increased rate capability will be installed on top of the inner (BI) MDT chambers

On-detector electronics of MDT, RPC and Thin Gap Chambers (TGC) will be replaced. Electronics upgrades are necessary to:

- Improve muon triggers, maintaining low trigger thresholds.
- Manage trigger rates effectively in the high- BIS RPC+SMDT rate, high-luminosity HL-LHC environment.
- Ensure compatibility with the new ATLAS trigger and readout scheme.

Upgrade and replacement of the Power System to cope with aging.

ATLAS Muon Spectrometer. In blue the RPC and MDT chambers while in grey the toroidal solenoid and the mechanical structure of the experiment

# TRIGGER LOGIC

- All hits from RPC detectors contribute to generating barrel trigger candidates.
- New BI RPCs enhance the geometrical acceptance and robustness of the barrel muon trigger, compensating for inefficiencies in old BM and BO RPCs.
- The new RPC trigger will utilize nine measurement planes (instead of six) from four layers of RPC chambers: one BI triplet (RPCO), two BM doublets (RPC1 and RPC2) and one BO doublet (RPC3).
- A trigger algorithm leveraging detector plane redundancy without a fixed pivot plane has been developed with different trigger coincidence logic schemes based on requirements across the four RPC chamber layers:
- 3/3 chambers: Hits in at least three out of four planes of RPC1+RPC2 chambers and in at least one out of two planes of RPC3, equivalent to the present high- $p_T$  trigger.
- 3/4 chambers: Previous requirement combined with hits in at least two planes out of three in RPCO and at least three planes out of six in RPC1+RPC2+RPC3, accepting all combinations of three-chamber

- of the barrel to maintain high trigger efficiency.
- 130 RPC Barrel Inner Large (BIL), 96 Barrel Inner Small (BIS) will be installed
- Despite reduced single-hit efficiencies, maintaining high trigger efficiency and purity is feasible by relaxing hit coincidence requirements in old chambers while introducing coincidences with new BI RPC chambers.
- Adding new RPC chambers in the barrel poses challenges in terms of space and installation logistics.
- In small sectors, installation of BI RPC chambers requires replacement of outermost BI MDT chambers with new sMDT chambers of reduced thickness.
- In large sectors, additional space exists for new RPC chambers without MDT replacement, contingent on

rearrangement of on-detector services.

In sectors 11-15, because of ATLAS feet the space is lacking, and the installation of 80 BOM/BOR special triplets is planned in the outer region.



Schematics of the new RPC-BI layout: large sector layout in the middle while on the edges there are the small sectors with new RPC-BI and sMDT chambers

# TRIGGER UPGRADE

The ATLAS TDAQ system [3] will undergo upgrades to have increased trigger latency required by the HL-LHC program. The upgraded system will feature a two-level trigger system:

• First-Level Trigger (L0): A hardware-based trigger utilizing muon and calorimeter data. L0 muon trigger candidates will be sent to the ATLAS LO global trigger within a latency of approximately 5 μs, with readout buffers accommodating a maximum latency of 10 µs. This extended latency allows for more complex trigger algorithms compared to the current Run 2 setup. • High-Level Trigger (HLT): A software-based trigger receiving events selected by the L0 trigger at a rate of 1 MHz. This tenfold increase in bandwidth enables maintaining low  $p_T$  thresholds despite increased luminosity, ensuring good acceptance for key physics channels.



#### coincidences.

• 3/4 chambers + BI-BO: Previous requirement combined with at least two hits in RPCO and at least one hit in RPC3, enhancing trigger coverage in regions without BM RPCs.

ATLAS Simulation



2 -0.5

ATLAS section with three possible muon trajectory: the first has 4 hits (one hit per RPC layer), the second has 3 hits and the last has two hits Trigger efficiency in function of the pseudorapidity for the three possible schemes

3/4 chambers

3/3 chambers

0.5

## **READOUT ELECTRONICS**

- The Data Collector and Transmitter (DCT) board interfaces with RPC Front-End boards and is based on FPGA.
- It receives trigger, timing, and control signals from barrel Sector Logic board through optical fiber and transmits zero-suppressed detector hit data to Sector Logic via a different optical fiber.
- Data transmission is handled by a GBTx chip.
- A total of 1096 DCT boards will be installed in the barrel as follows: 272 for BI, 424 for BM and 400 for BO connected to 32 off-detector Sector Logic boards. There will be two types of DCT:

#### DCT-BM/BO

• Front-End electronics boards in present BM and BO chambers, located within detector Faraday cages, perform amplifier, shaper, and discriminator (ASD) logic. These Front-End boards are compatible with Phase-II requirements and do not require replacement.

Section of ATLAS Muon Spectrometer: On top the section for the small sectors and on the bottom the section for large sectors

#### **POWER SYSTEM**

- MDT, RPC, and TGC detectors equipped with lowvoltage (LV) and high-voltage (HV) power systems from the EASY 3000 family by CAEN. These systems include power supply modules as well as modules for monitoring and control. They were tested up to accumulated radiation doses equivalent to 1500  $fb^{-1}$ approximately half the expected total dose at the HL-LHC. Combination of ageing, irradiation, and component obsolescence will pose significant challenges for maintenance up to 2035–2040, making it both problematic and costly.
- The replacement schemes for power system components of the muon system foresees a complete replacement during Long Shutdown 3 (LS3).



Scheme of the Power System: the detectors are connected to the racks or

- Present on-detector trigger and readout electronics (Pad and Splitter boxes) are incompatible with Phase-II and will be substituted by new DCT boards.
- Each DCT board replaces one pair of Pad and Splitter boxes.

#### DCT-BI

- BI DCT FPGA decodes TDC input data before performing zero-suppression logic.
- Output data format remains consistent with BM/BO.
- New BI front-end electronics feature internal Time-to-Digital Converter (TDC) embedded in Front-End ASIC with 100 ps time resolution.



balconies which is interfaced to the Mainframes outside the cavern



- Upgrades to the Muon Spectrometer are crucial for maintaining performance under the high-rate, highluminosity conditions of the HL-LHC. Trigger systems are being upgraded to cope with increased luminosity and maintain low trigger thresholds.
- Evolutionary schemes involve transitioning from single-level to two-level triggers for improved performance and adaptability.
- Replacement of on-detector trigger and readout electronics is essential for compatibility with Phase-II requirements.
- Ageing, irradiation, and component obsolescence pose significant challenges for maintaining the original power systems.

### REFERENCE

- ATLAS Collaboration, CERN-LHCC-97-022, ATLAS muon spectrometer : Technical Design Report
- ATLAS Collaboration, CERN-LHCC-2017-017, Technical Design Report for the Phase-II Upgrade of the ATLAS Muon Spectrometer
- 3. ATLAS Collaboration, CERN-LHCC-2022-004, Technical Design Report for the Phase-II Upgrade of the ATLAS Trigger and Data Acquisition System - Event Filter Tracking Amendment