A versatile and fast pixel matrix read-out architecture for MAPS

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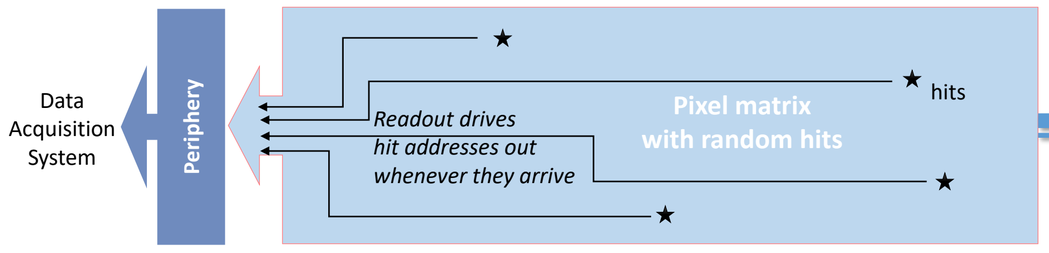
Goals:
- Implementation of an asynchronous architecture for monolithic pixel matrix readout
- Initial step to improve consumption and reading speed
- Timestamping at the end of column with a nano second resolution

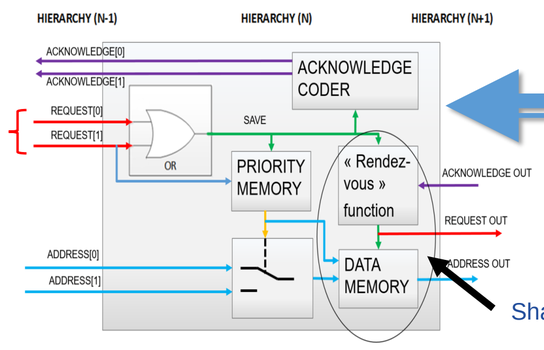
Asynchronous readout

Matrix readout within MAPS



Asynchronous arbiter principle (2 to 1)

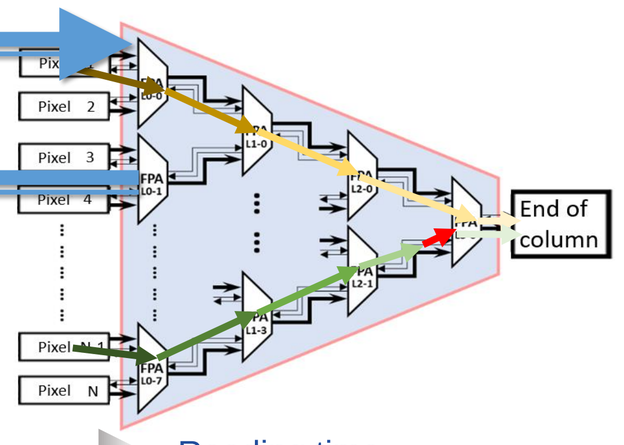
Fixed Priority Arbiter (FPA)
Between 2 pixel inputs



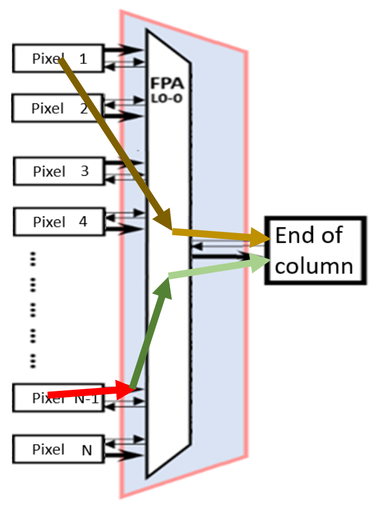
Shareable part

Architecture made of cascade of arbiters

2 to 1 arbiters (bandwidth optimized)



N to 1 arbiters (area optimized)



Reading time
Arbitration collision (pending signal)

Fixed Priority Arbiter (FPA) implementation

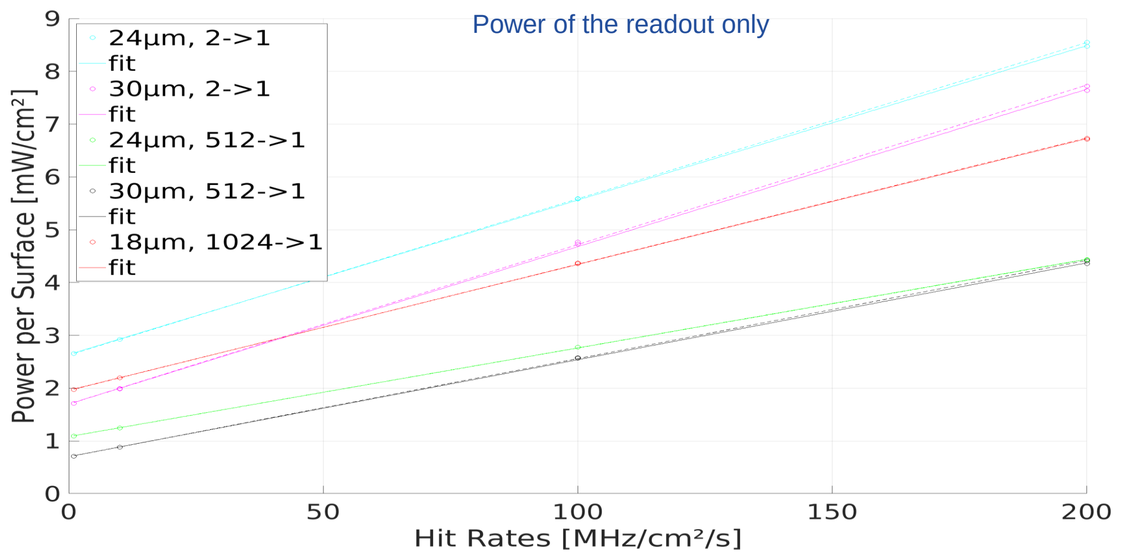
Various complete designs
(only redaout for a double-column)

Results from post-layout implementation

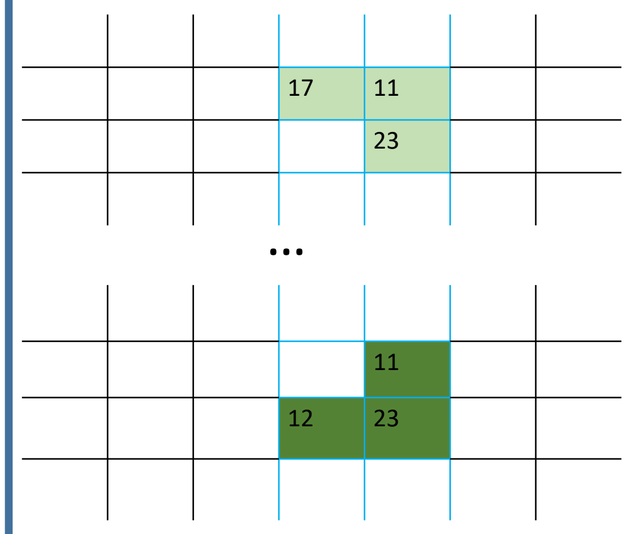
Ctrl size	Pitch µm	Nb of pixels	Cell	Vert. Metal
1024 -> 1	18	1024	35%	18%
2 -> 1	24	512	25%	7%
512 -> 1	24	512	12%	7%
2 -> 1	30	512	14%	5%
512 -> 1	30	512	6%	5%

Percentage used by the circuit in the given pitch

Linear power density over hit-rates



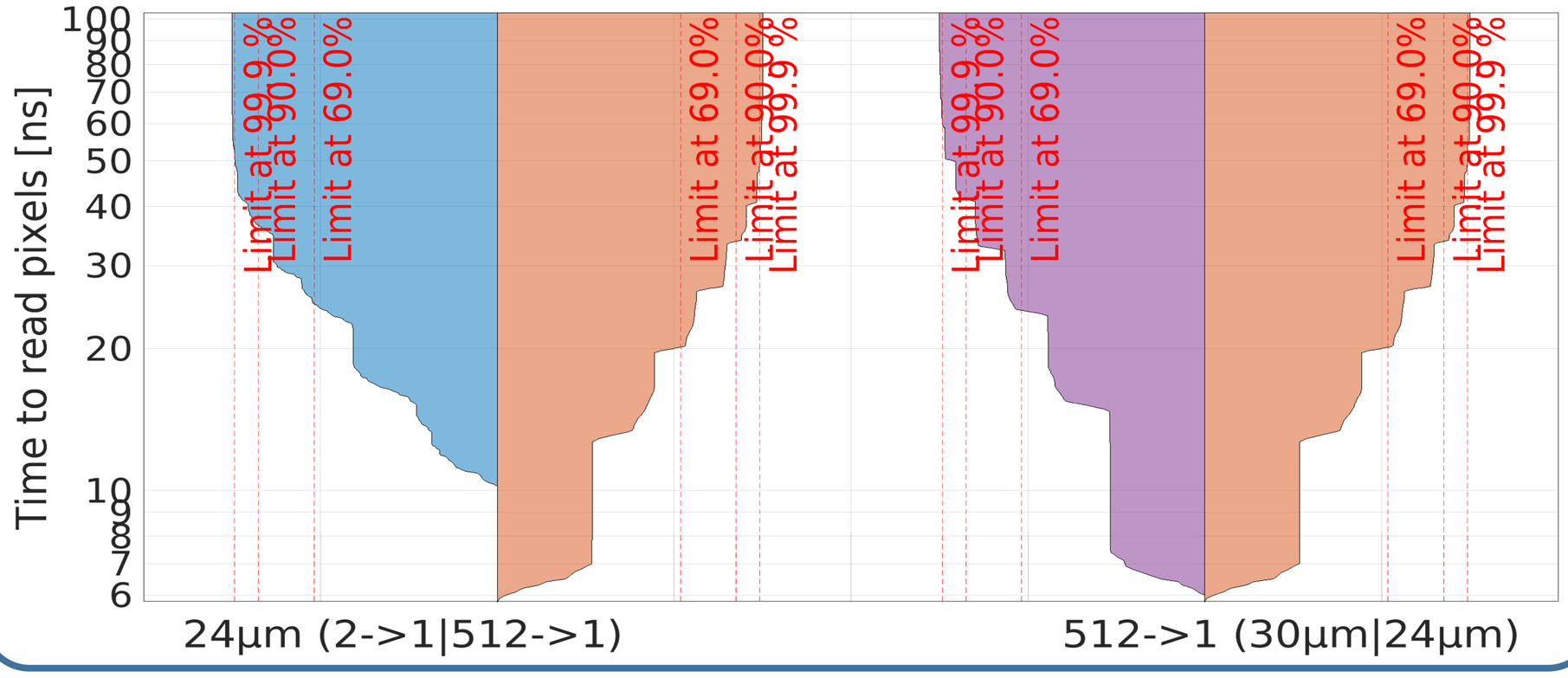
Time-stamping
(consecutive hit clusters)



Matrix of pixels with readout time (ns)
- Bunch crossing 1 (0-25ns)
- Bunch crossing 2 (25-50ns)

Readout time performance

Matrix stimulated with random hits (with physical shapes) at 100 MHz/cm²



Summary

- **Reading speed:**
  - Mean time per pixel around 20ns at 100MHz/cm²
  - 99,9% of pixels read within 100ns
  - Rates close to 5 Gparticles/cm²/s accessible
- **Power consumption:**
  - Below 10mW/cm²
  - Linear peer hit (asynchronous behaviour)
- **Time stamping:**
  - Possibility to timestamp hit at 2ns, assuming:
    - Fast clock only at periphery
    - Time-walk corrected

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