The description of the steps of the Q&A test and detector module assembly of the CBM-STS

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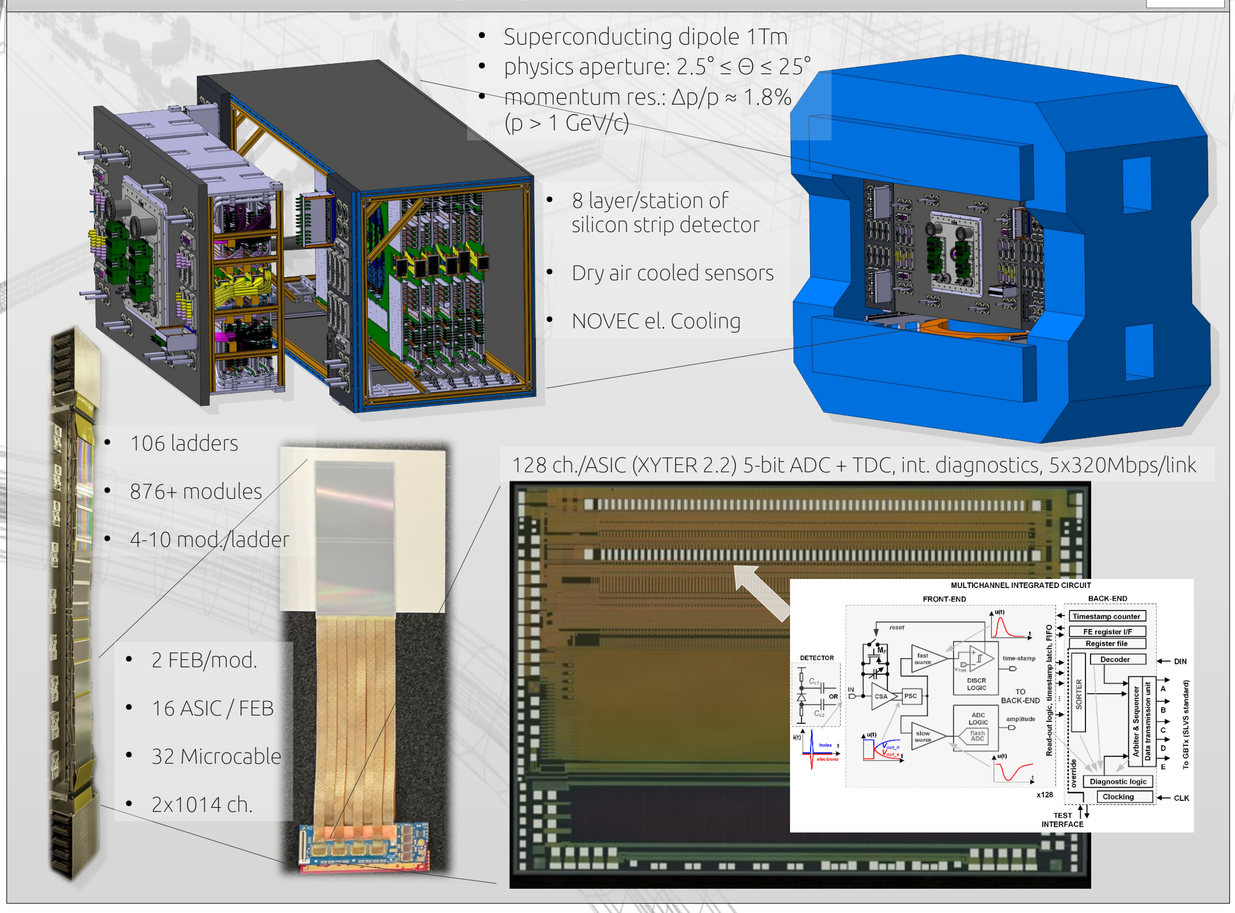
Introduction

CBM Bhsics Book

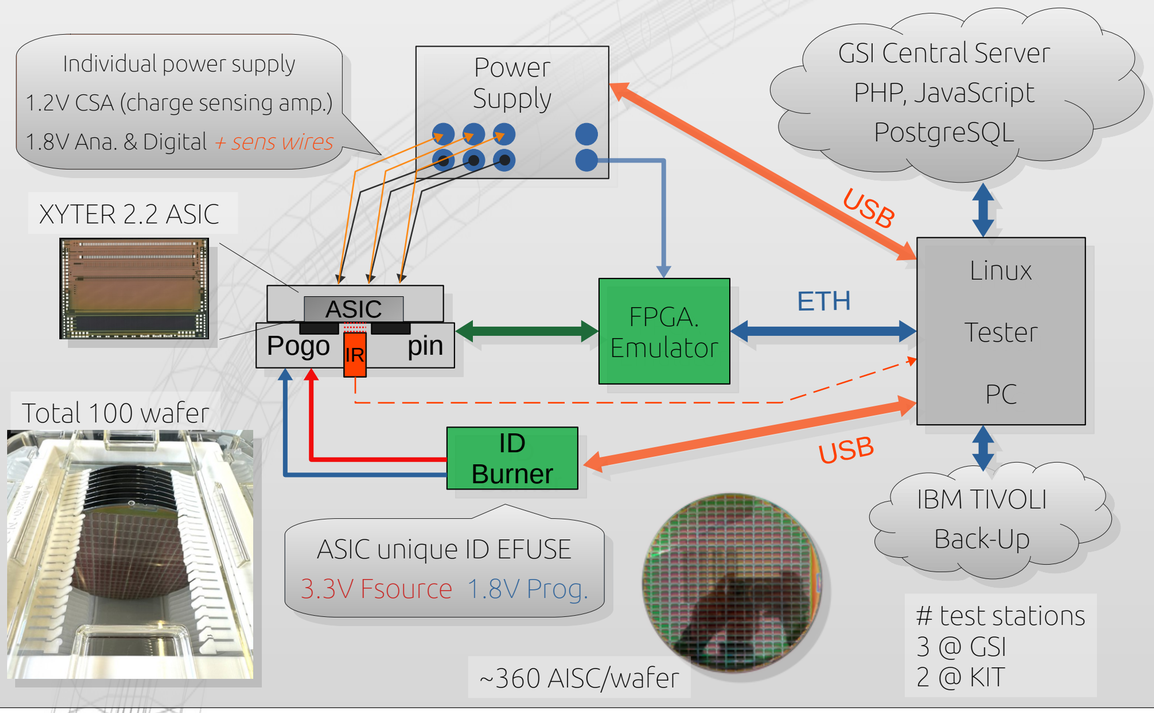
Abstract – The Silicon Tracking System (STS) is the core detector system of the Compressed Baryonic Matter (CBM) experiment at the Facility for Antiproton and Ion Research (FAIR) in Darmstadt, Germany. CBM will study matter at the highest baryonic densities in collisions of nuclear beams with a stationary target. The expected long latency for identification and the changing signature of the events drive us to use self-triggered streaming readout. CBM data collection will be based on time-stamped detector data into a compute farm. Event reconstruction and physics analysis are performed online at collision rates up to 10 MHz. In the presented work, we will discuss step by step how the CBM-STS detector components are rigorously selected and prepared for assembly. It all starts with carefully testing the readout ASICs manually or at the wafer level. The various parameters are recorded to select the chip. The next step is to test the tap-bonding to the micro cables and, later, the 16-chip cables that are bonded to the silicon strip sensor. All test results are stored and available for later use in a specially designed database using custom software that is applied to each step in the assembly process. More than ten percent of the modules will be produced by the time of the presentation so that an overview of the production can be presented.

The Silicon Tracking System (STS)

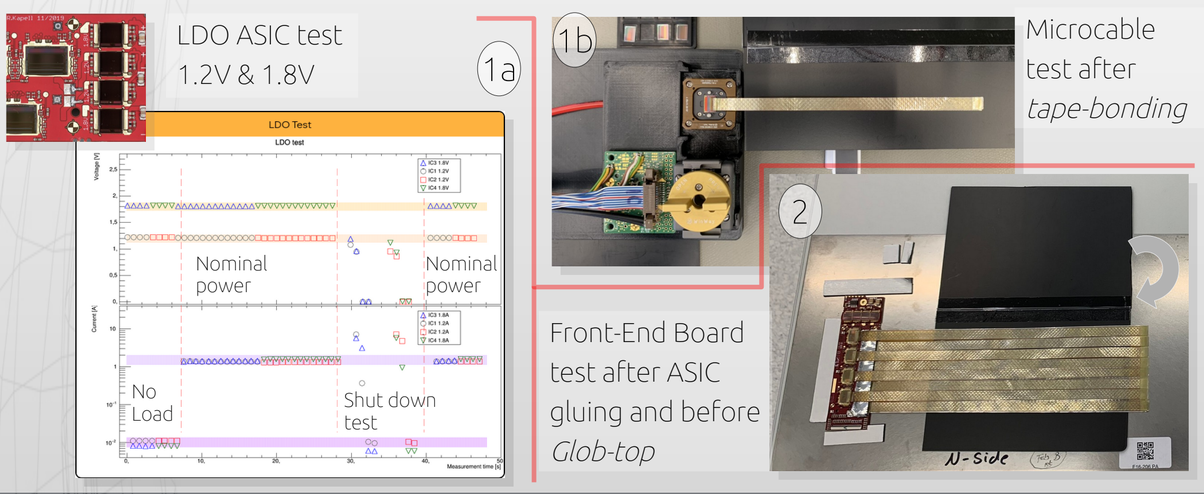
Poster - Johann M. Heuser



ASIC Test Procedure

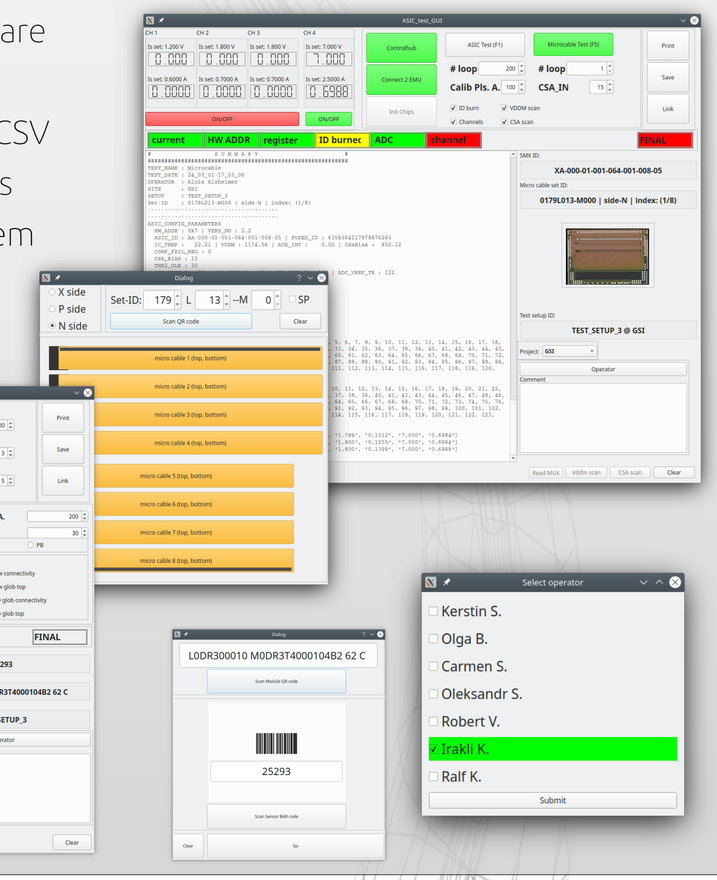


LDO and FEB (Front-End Board) test



Test and Calibration during the assembly

- Custom developed test software
- Adaptive test procedures
- Configurations via YAML and CSV
- Python, PyQT5, PyROOT, Ipbus
- Fully integrated modular system
- *Software more than **10k** lines of code*

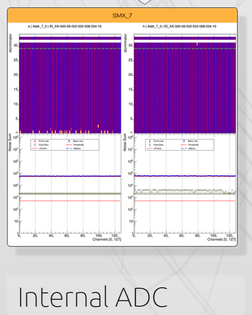


Data Base + Web Interface

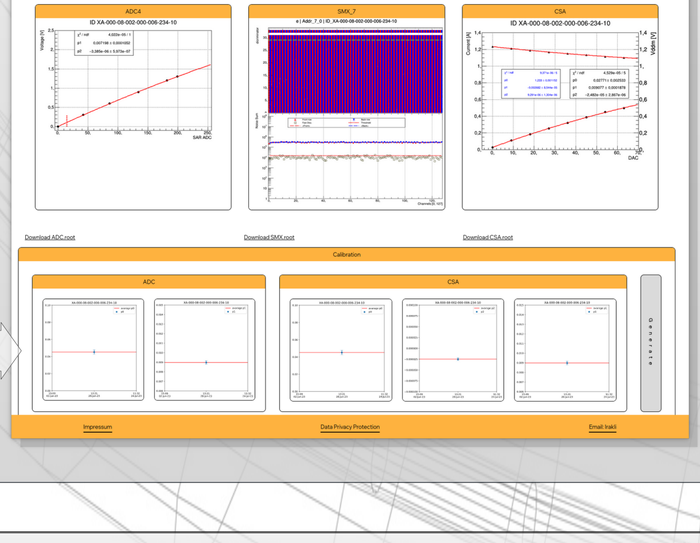
http://web-docs.gsi.de/~dtl-sts/

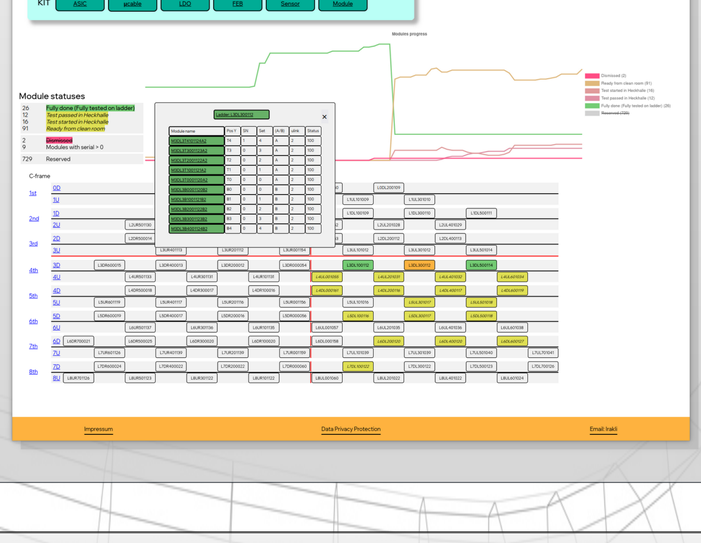
Custom developed PHP, Python, and PostgreSQL-based data monitoring system in collaboration with Jagiellonian University, Krakow. *front&back**10K** lines of code.*

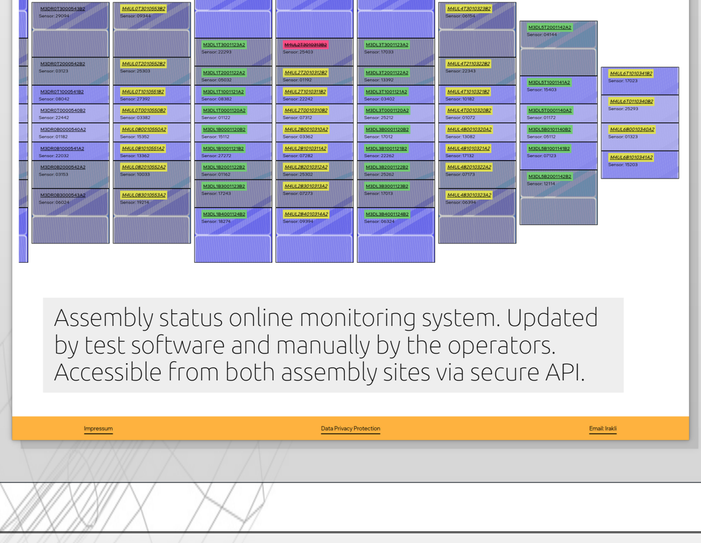
ASIC internally generated charge for both polarity



Internal ADC diagnostic and charge-sensing amplifier CSA circuit calibration







Assembly status online monitoring system. Updated by test software and manually by the operators. Accessible from both assembly sites via secure API.

Summary

- The assembly of the modules has been started in 2023 at two assembly sites, GSI and KIT. The procedures are identical and always interchangeable.
- To date, more than 140 modules have been produced out of almost 900 (876++) planned. All modules are tested step by step during the assembly and later characterized.
- Each module proceeds the so-called burn-in procedure, where the modules are cooled down and warmed up five times and monitored for failures.
- After the whole ladder is assembled, it will be tested simultaneously in realistic conditions. Each station (layer) will also undergo rigorous tests before being installed in the STS box.
- The appropriate lab environment, including the final cooling system, power, high-voltage supplies, and a fast readout and control system, is under development for the final test.

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