Contribution ID: **93** Type: **Poster**

R&D of a timing measurement ASIC for possible HL-LHC upgrade

Friday, 31 May 2024 08:40 (1 minute)

The Compact Muon Solenoid (CMS) experiment at the Large Hadron Collider (LHC) at CERN will undergo a major upgrade for the high-luminosity phase of the LHC (HL-LHC), which is expected to start in 2029. In addition to improving the detector rate capabilities and performance at increased higher luminosities, precision timing measurements are added to mitigate pile-up effects. The timing detector currently under construction cover pseudorapidity up to $\eta = 3$. A possible pathway for further improvements is the extension of timing capabilities to cover the full tracker acceptance up to $\eta = 4$. Low Gain Avalanche Detectors (LGAD) pixels have been shown to be a suitable candidate for replacing a part of the pixel detector end-caps during a future Long Shutdown or Year-End Technical Stop of the LHC.

Here, we present design efforts towards a readout Application-specific integrated circuit (ASIC) capable of operating with LGAD pixel detectors in the environment of the pixel end-caps at the HL-LHC. It is designed in a 28 nm CMOS technology, to process the signals from LGADs that will be used as the sensors for this timing layer.

LGADs are a class of silicon sensors that feature an internal moderate gain, enabling fast and precise timing measurements. The targeted ASIC should feature a low jitter preamplifier, a discriminator with time walk correction, and a Time-to-Digital Converter (TDC) targeting a final resolution of 30 ps. It also provides a digital interface system for configuration and readout, designed to balance between power efficiency, integration and performance.

We report on the results of the modeling and simulations of the analog part at transistor level. We explain the challenges and the different concepts to meet the requirements of the possible CMS timing upgrade in terms of noise, gain, linearity, time resolution, power consumption, and different implementations of the LGADs.

Collaboration

Role of Submitter

I am the presenter

Primary author: Dr GHIMOUZ, Abderrahmane (Paul Scherrer Institut)

Presenter: Dr GHIMOUZ, Abderrahmane (Paul Scherrer Institut)

Session Classification: Electronics and On-Detector Processing - Poster session

Track Classification: T7 - Electronics and On-Detector Processing