R&D of a timing measurement ASIC for possible HL-LHC upgrade

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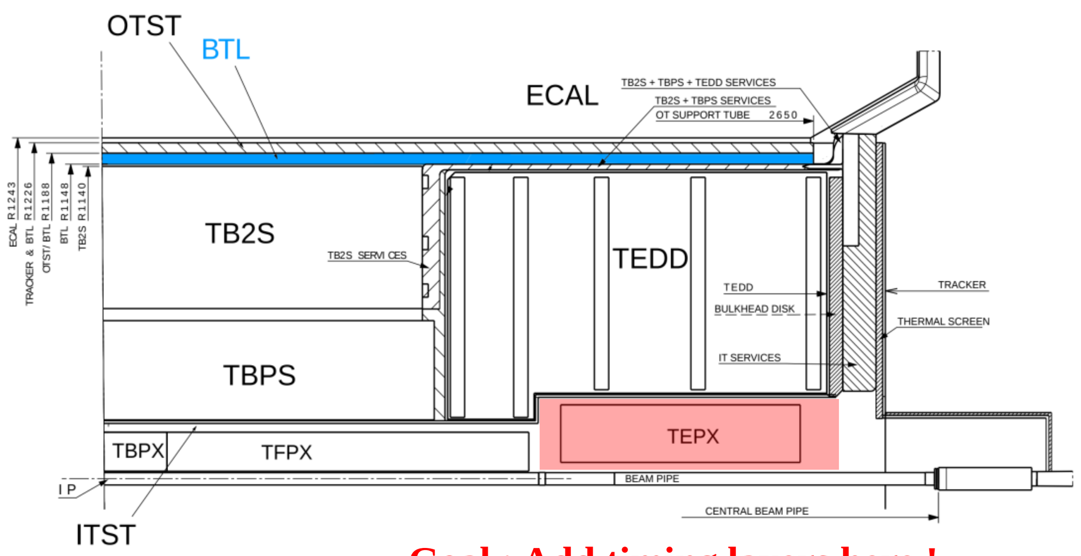
Introduction

The Compact Muon Solenoid (CMS) experiment at the Large Hadron Collider (LHC) will undergo a major upgrade for the high-luminosity phase (HL-LHC) starting in 2029. The goal is enhancing the detector rate capabilities and adding precision timing measurements to mitigate pile-up effects. With potential future improvements extending the timing coverage to $\eta = 4$, Low Gain Avalanche Detectors (LGAD) based pixels are being considered to replace part of the pixel detector end-caps.



Goal : Add timing layers here !

Challenge

In this context, we aim to design a readout Application-specific integrated circuit (ASIC) capable of operating with LGAD pixel detectors in the environment of the pixel detector end-caps at the HL-LHC for CMS. It is designed in a 28 nm CMOS technology, to process the signals from LGADs that will be used as the sensors for this timing layer.

$$\sigma_t^2 = \sigma^2_{\text{Landau}} + \sigma^2_{\text{Distortion}} + \sigma^2_{\text{Timewalk}} + \sigma^2_{\text{TDC}} + \sigma^2_{\text{Jitter}}$$

Sensor (characterization) — To model and optimize (FEE architecture)

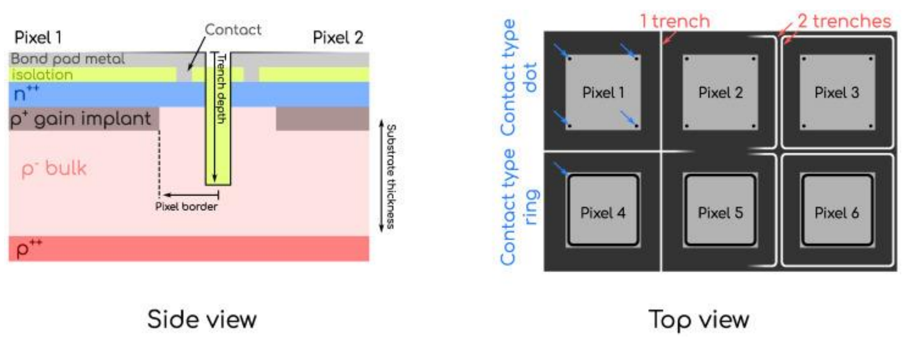
Property	Value
Pitch	100 x 100u / 200 x 200u
Input capacitance	~ 1 pF (including parasitic)
Time res RMS	30 ps
Max latency	500 KHz to 1 MHZ per pixel
Max dead time	< 250 ns
Total power density	1 W/cm2
Threshold Level	1000 e^-
Dynamic range (Q)	Equivalent 1000 e^- to 100 Ke^-
Pixel rate at hottest pixel	50 KHz

LGAD characterization

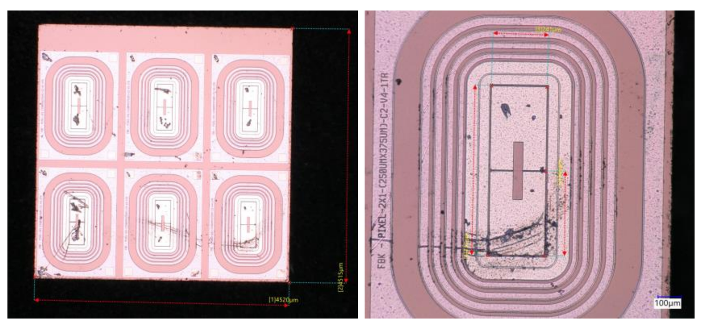
*Acknowledgements to Matias Senger from University of Zurich for the samples

❖ Type of the sensor : Ti-LGAD

Schematic structure of the sensor

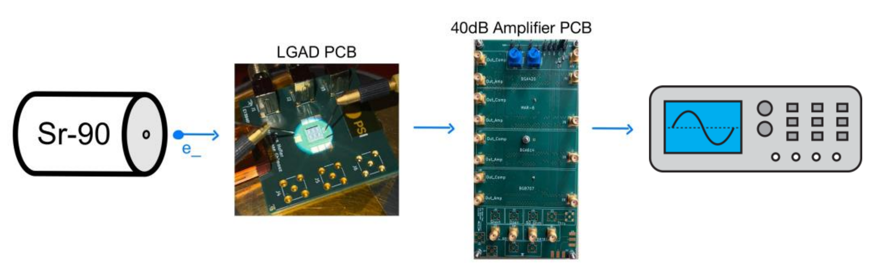


Picture of the sensor matrix sample

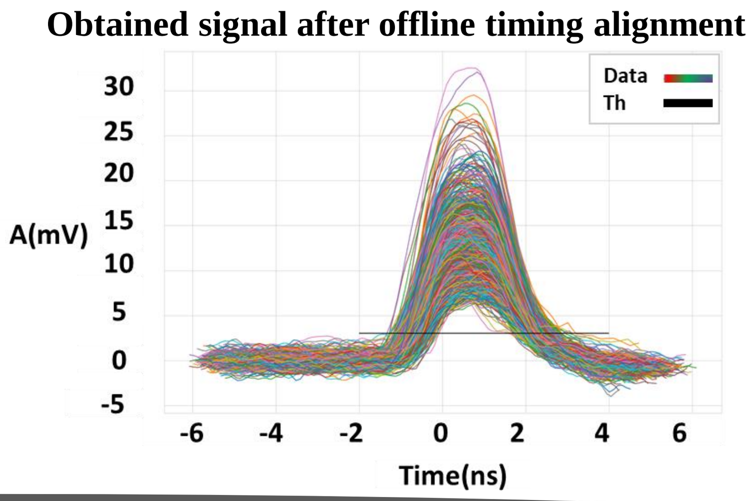


❖ Signal characterization of the sensor

Setup for the measurement of the response of the sensor



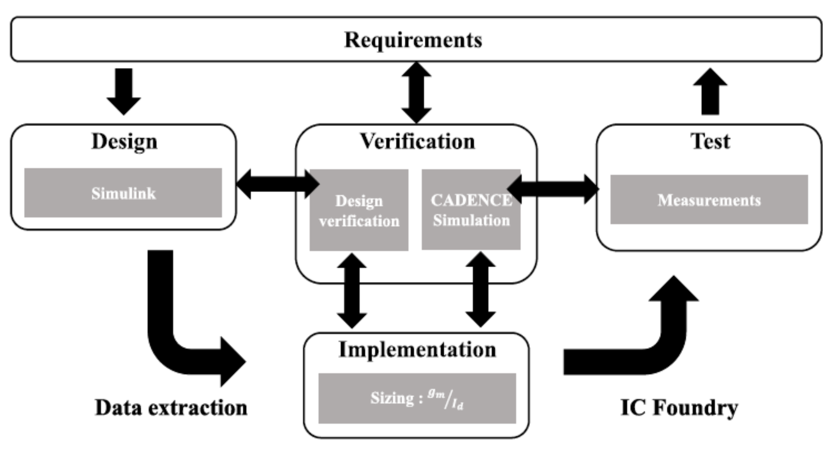
Obtained signal after offline timing alignment

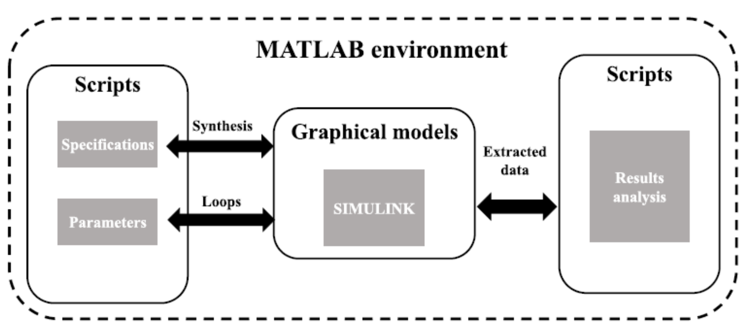


FEE modeling

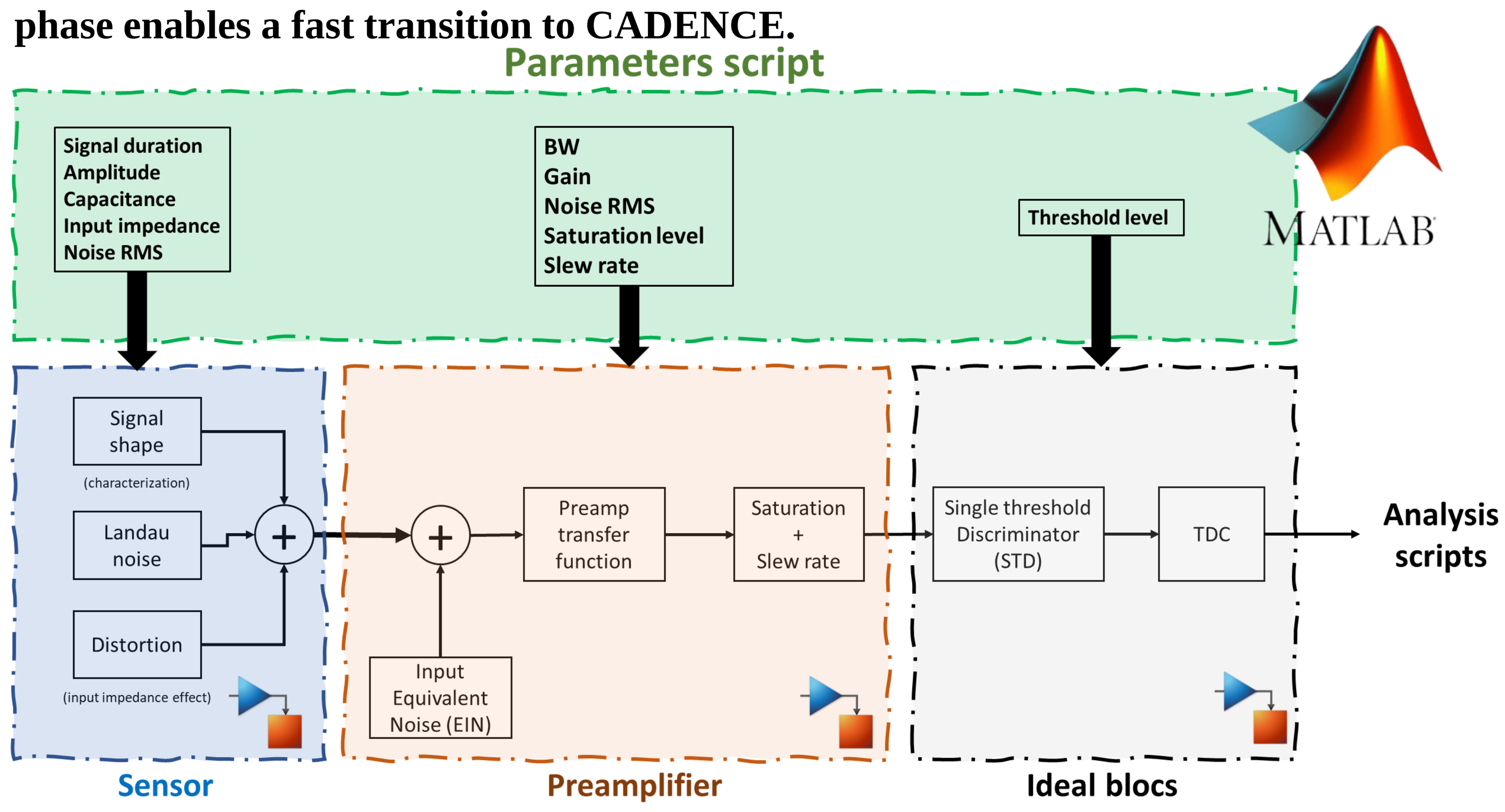
❖ The model-based design methodology

Defining the best parameters to achieve the desired specifications with efficiency





The model is designed using SIMULINK / MATLAB (script environment). The goal is to study the behavior of every bloc the system : Sensor (Obtained from the characterization) + FEE (Depends on the choice of the topology). The results from this phase enables a fast transition to CADENCE.

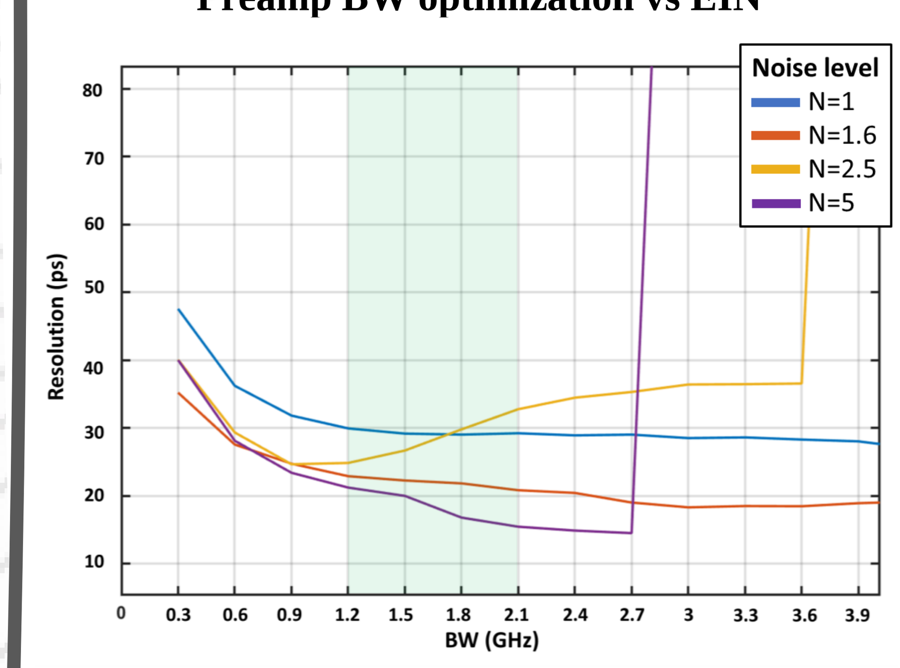


In this first step, we focus on studying the effect of the key parameters of the preamp on the timing resolution (few Ke^- signals) using an ideal STD and TDC. The integration between the sensor and the preamp is modeled as well.

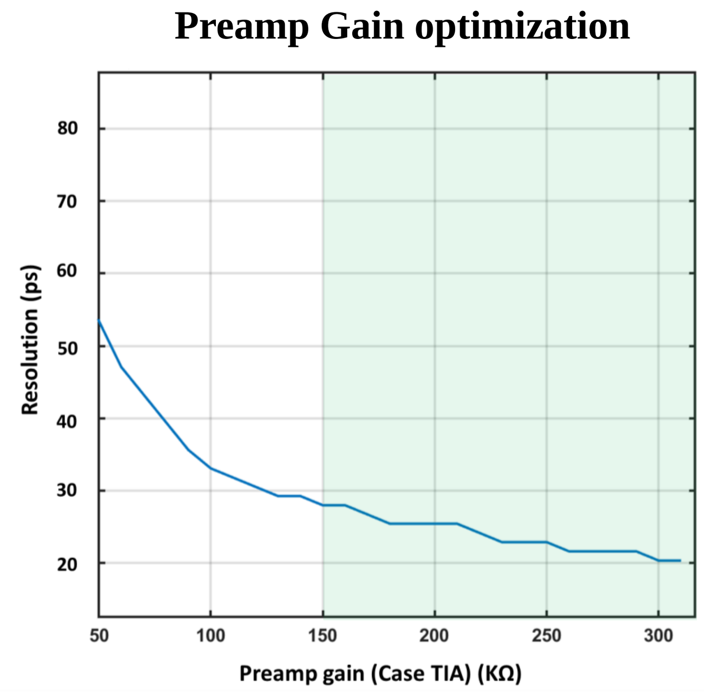
❖ Result of the modeling of sensor + preamp stage

Here, we illustrate the result of optimizing the choice for the BW and gain of the preamplifier to ensure the desired resolution (Green zone) for different scenarios of the preamp noise behavior.

Preamp BW optimization vs EIN



Preamp Gain optimization



Conclusion

- ✓ Initial system specifications are confirmed ➔ more sensor characterizations are planned ➔ New sample designs;
- ✓ Behavioral Model under development ➔ Multiple FEE solutions are investigated and optimized to reach the timing requirements ➔ multi-flavors ASIC;
- ✓ First 28nm layout in progress;

References

- CMS Collaboration, A MIP Timing Detector for the CMS Phase-2 Upgrade, Report number: CERN-LHCC-2019-003, CMS-TDR-020;
- Senger, M.; Macchiolo, A.; Kilminster, B.; Paternoster, G.; Centis Vignali, M.; Borghi, G. A Comprehensive Characterization of the TI-LGAD Technology. Sensors 2023, 23, 6225.
- Ivan Liebgott and Ascension Vizinho-Coutry. "Integration of the model-based design -Industrial approach - for teaching engineering science." In: 2016 IEEE Global Engineering Education Conference (EDUCON). 2016, pp. 697–701. DOI:10.1109/EDUCON.2016.7474626.